

Digital Circuit Lab

TA: Po-Chen Wu







Outline

- Programmable Data Generator
- Logic Analyzer
- Complete the RSA System







Programmable Data Generator







Introduction to PG

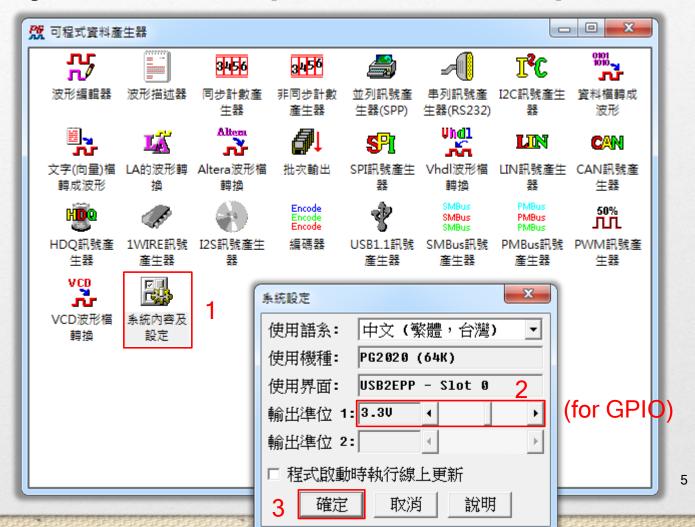
- Programmable data generator (PG in brief) is powerful of generating several kinds of digital waveforms.
- Combining logic analyzer (LA) and PG will make an auto testing system or auto verification system.







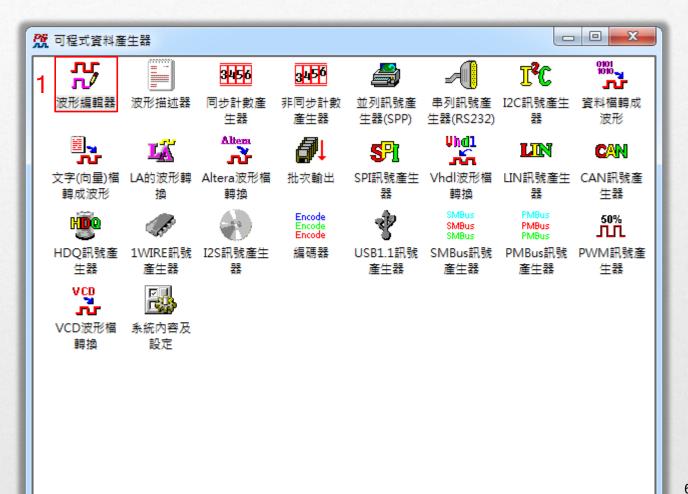
System Properties Setup







Wave Editor









Definitions

- Label (signal name)
 - Labels can be defined as numeric, alphabetic, underscore _, [, or], yet their length cannot be over 31 characteristics (bytes).
- Channel (POD order from left to right)
 - Pod A = CH-00 ~ CH-09
 - Pod B = CH-10 ~ CH-19
 - Extended Pod = Event_1, ..., Clock_Out







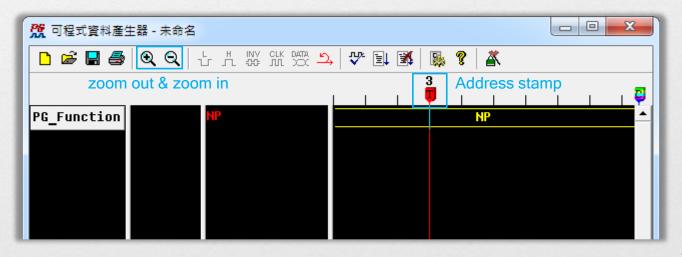






Zoom in & Zoom out

 Note! The base point is the Address Stamp of the waveform field whenever the waveform is either zoomed in or zoomed out.



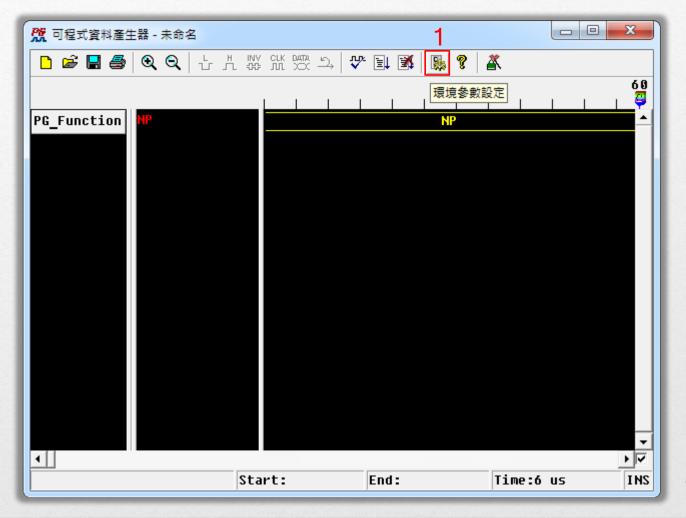








Set Parameter









PG is positive-edge-triggered.



- 1 (internal clock frequency)
- 2 (keyboard event)
- 3 (cursor change time gap, the cursor transformation depends on it)

Cursor

Drag mode When you stop the Drag cursor for a while, it will restore to Point cursor.

You just move Point cursor quickly then the Point Cursor will change to be Drag cursor automatically.

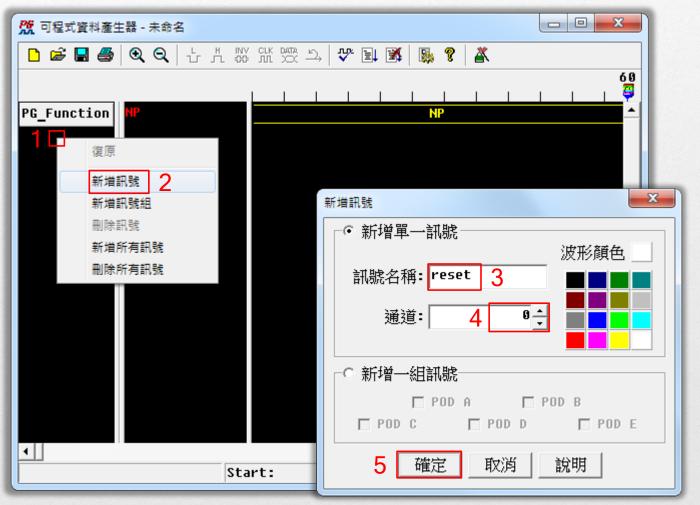








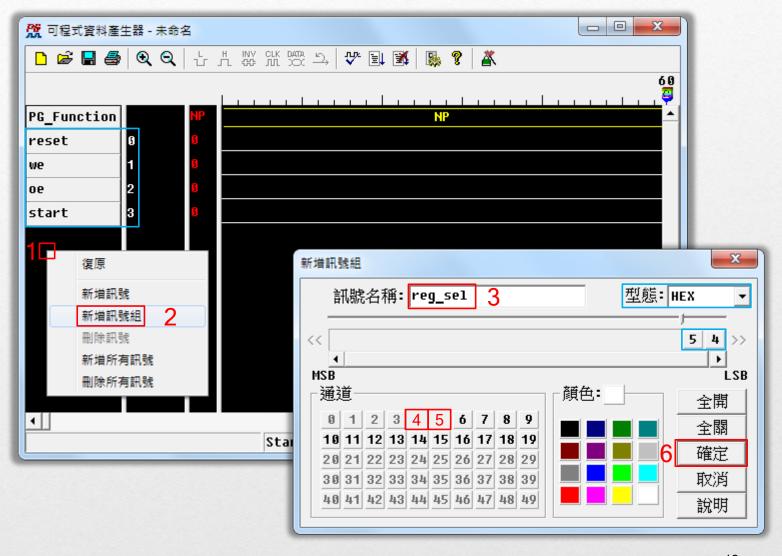
Add Label









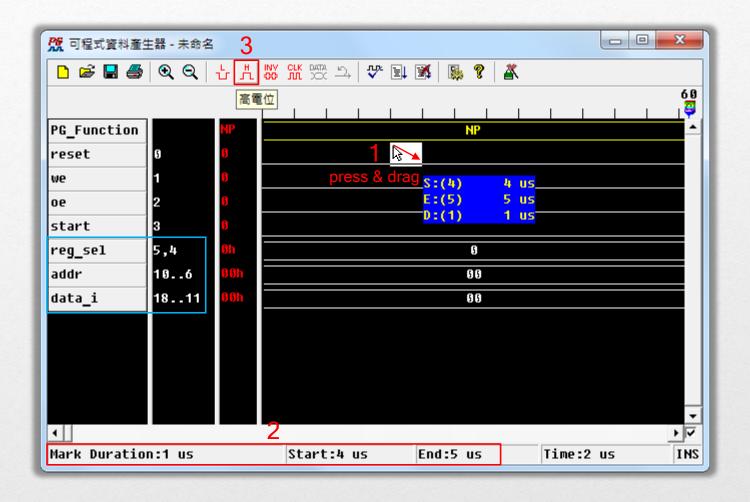






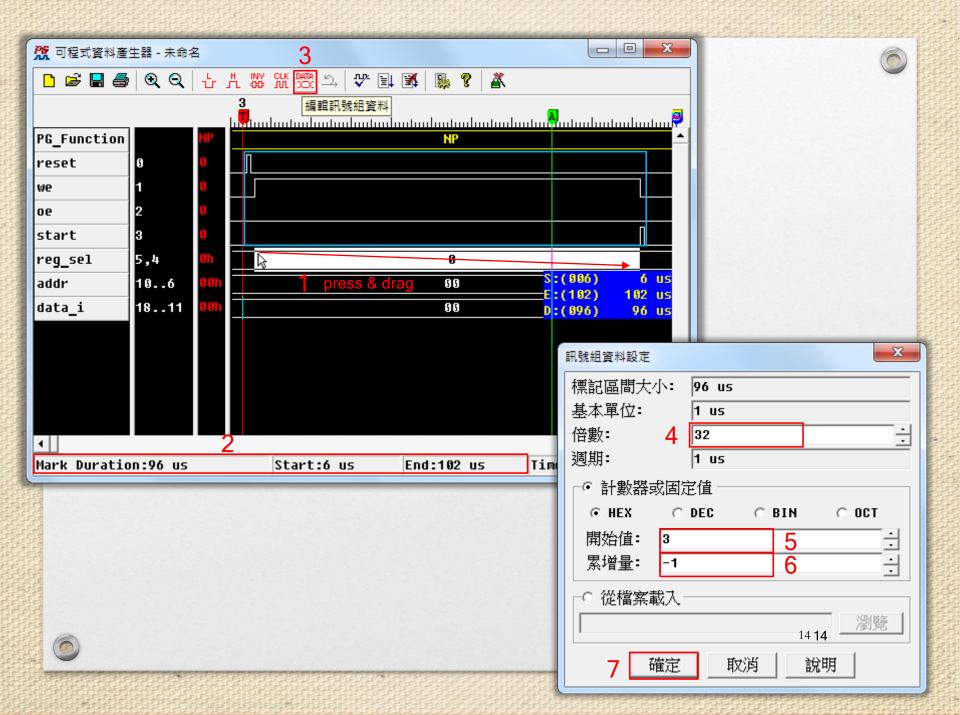






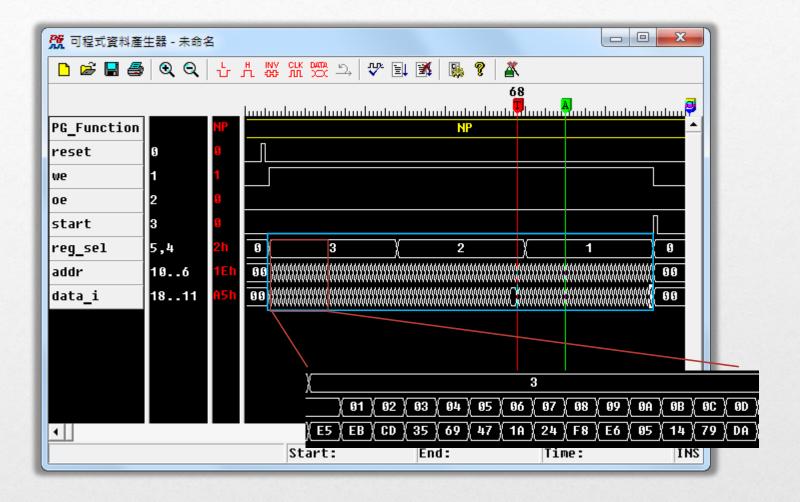


















Command Setting

 There is one label named PG_Function in waveform field cannot be deleted. You may set PG_Function command to control the waveform output flow.

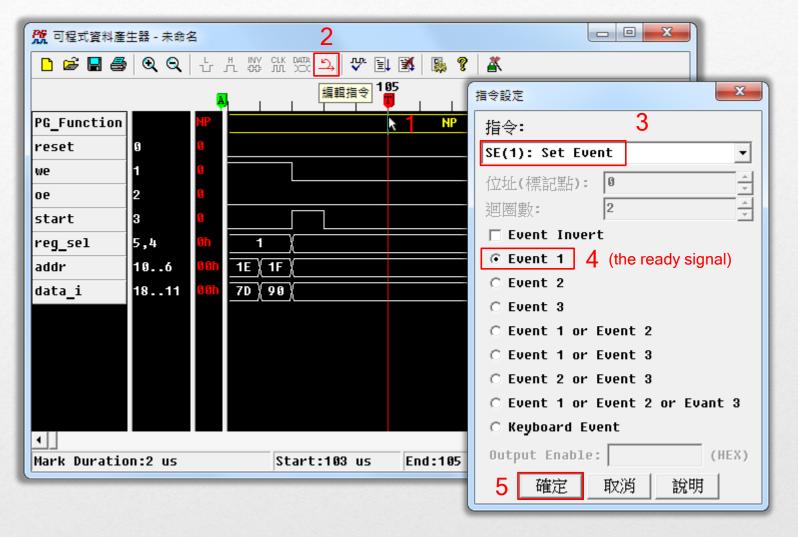
Name	Intruction	Description
NP	No Operation	No action
SE	Set Event	Set Event to be a trigger
WE	Wait Event	Stop for waiting Event received









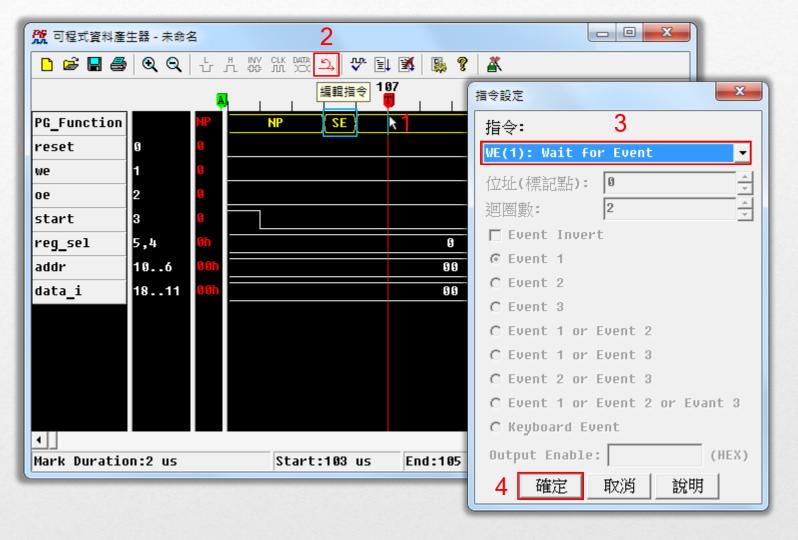










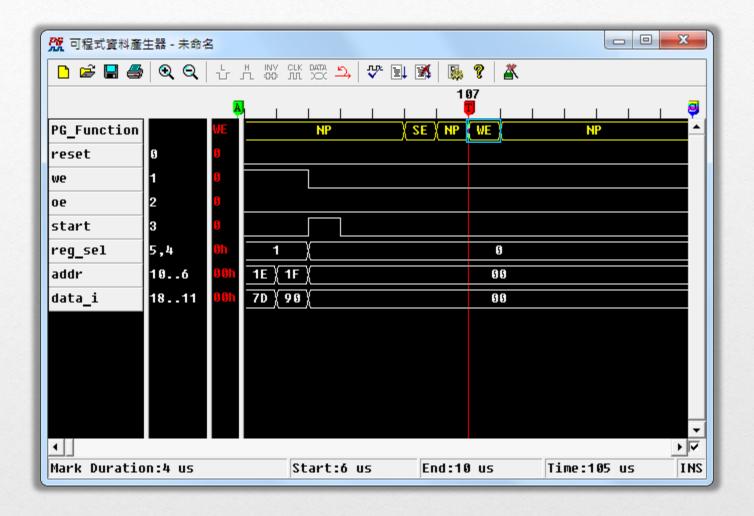






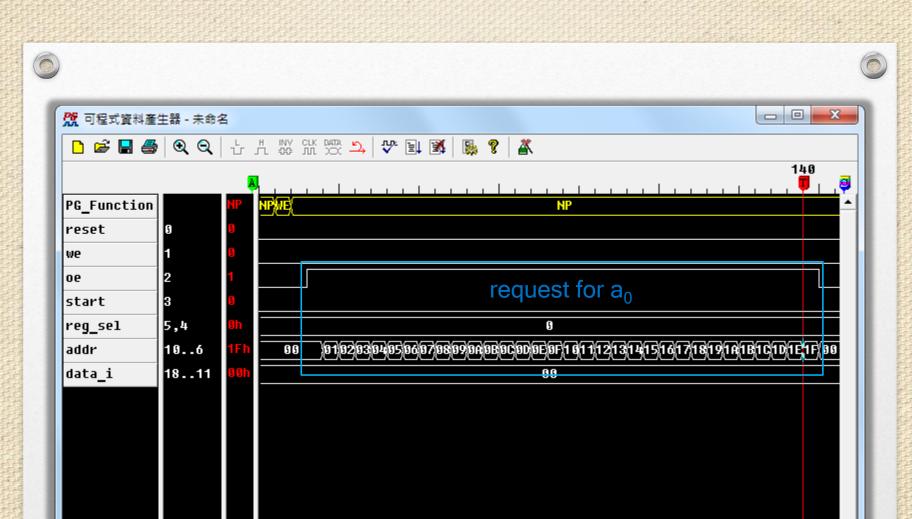














Start:

End:

Time:126 us

20



INS



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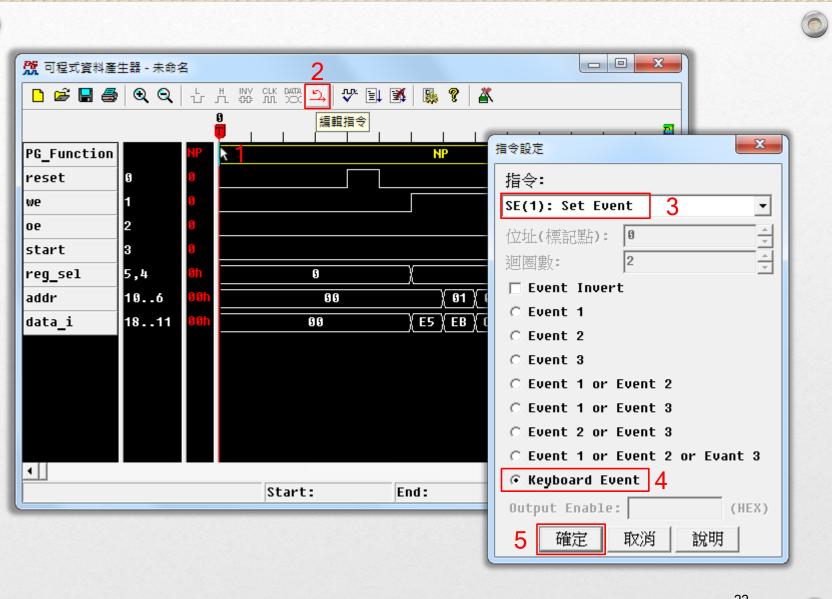


Before Running

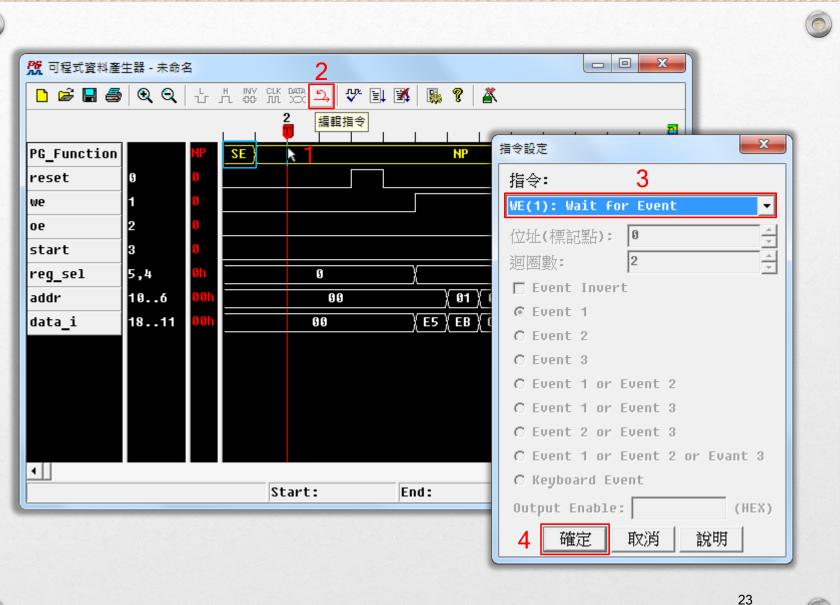
- After finished waveform check and reported no errors, you may click Run button to output these data.
 - PC will take 0.5~1 second to transform these data into PG through USB port.
 - The tip of running PG is to insert Set Keyboard Event and Wait Event command in the empty front area of waveform field.







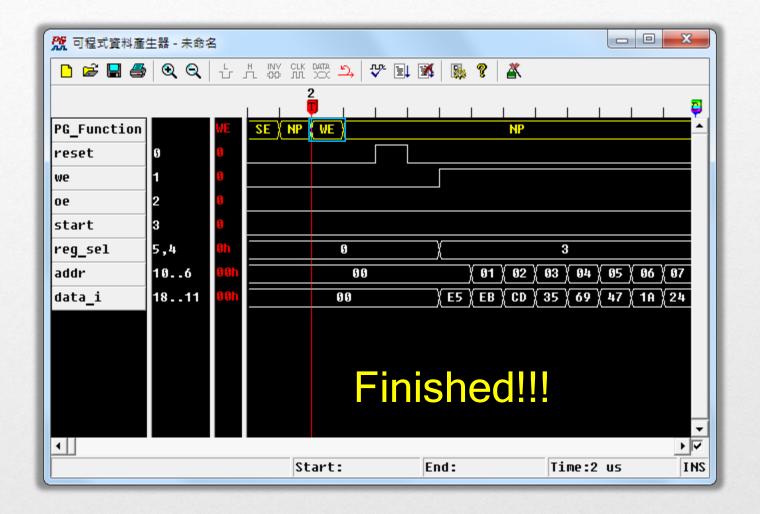












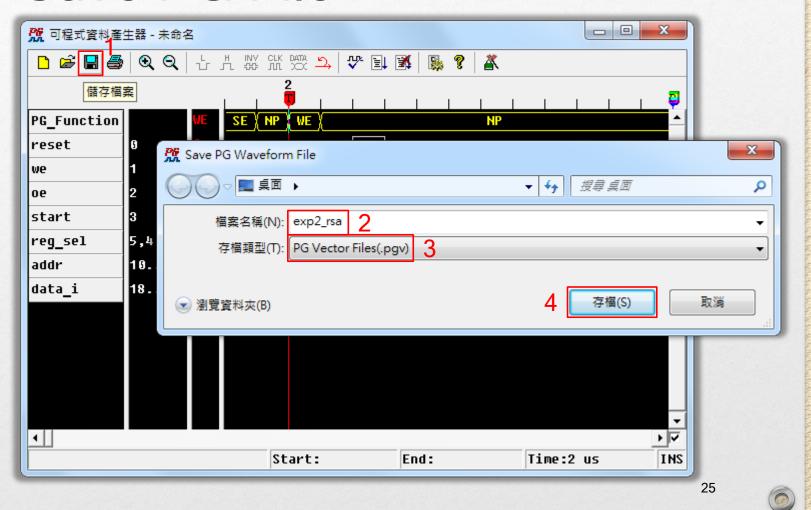








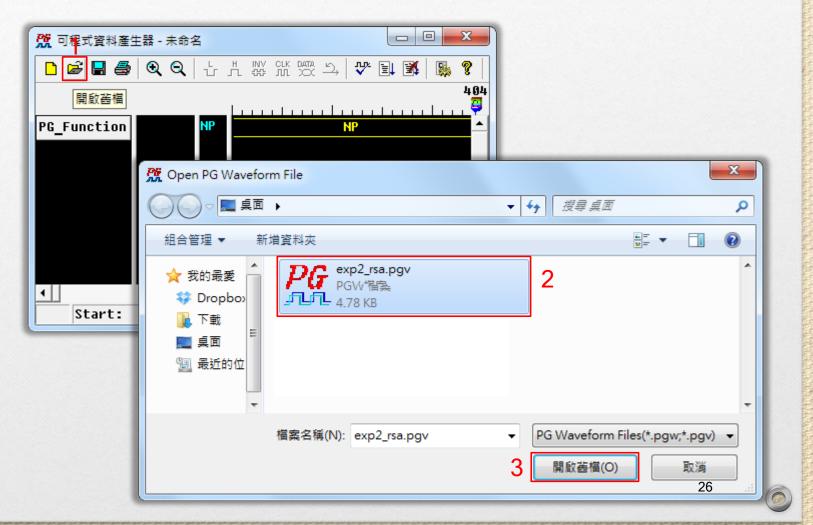
Save PG File



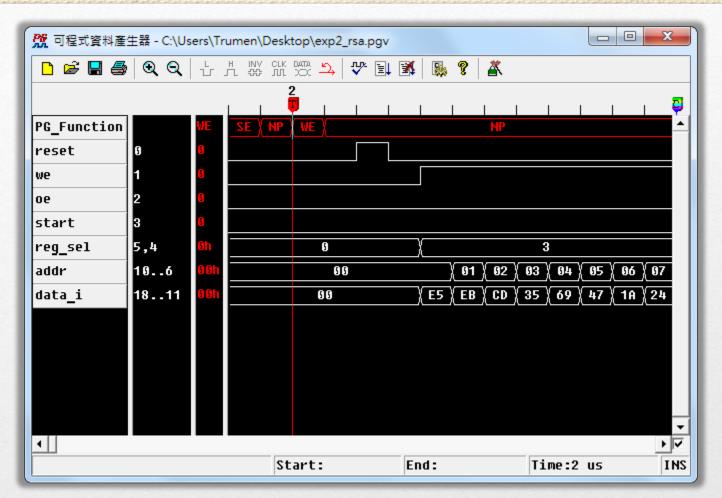




Load PG File









Double click ⇒ Doesn't work!

(It only open the PG software but does not load the waveform file. So you have to load it again.)







Logic Analyzer



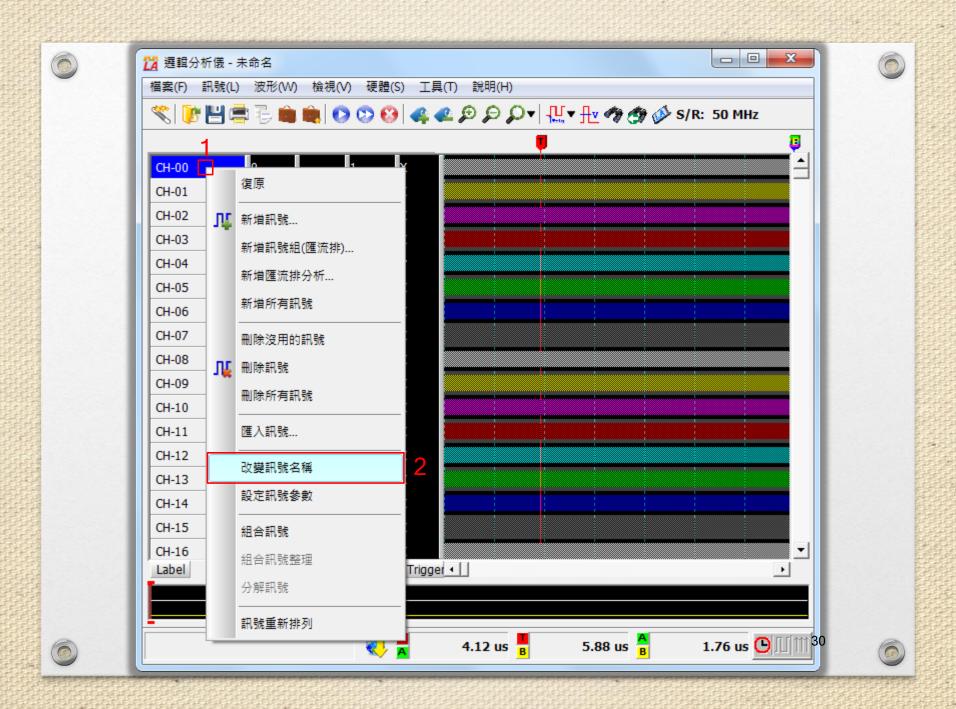


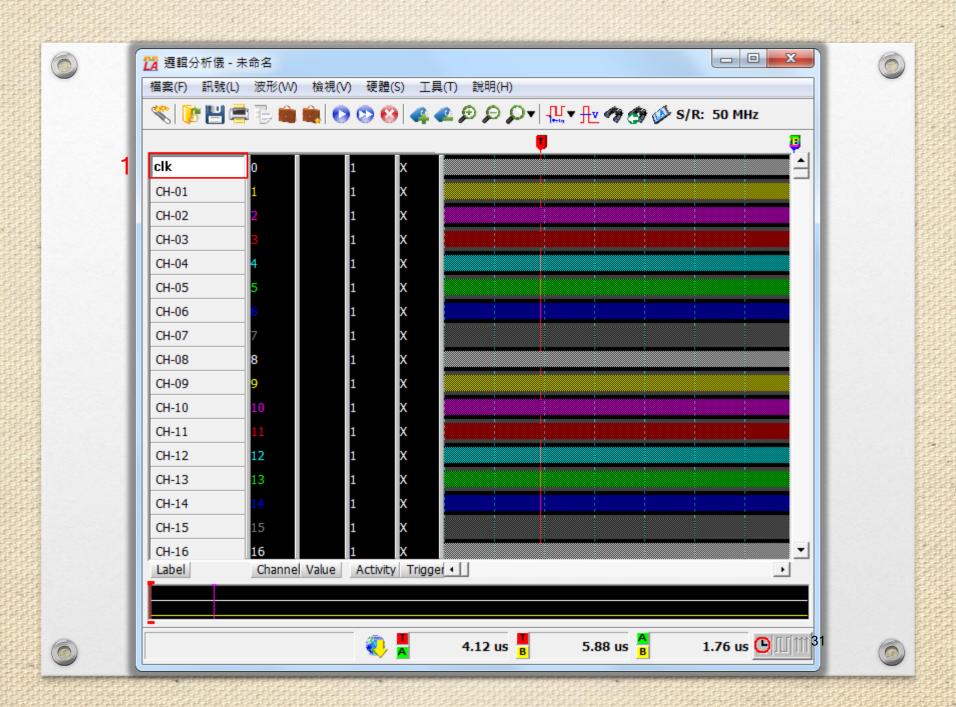


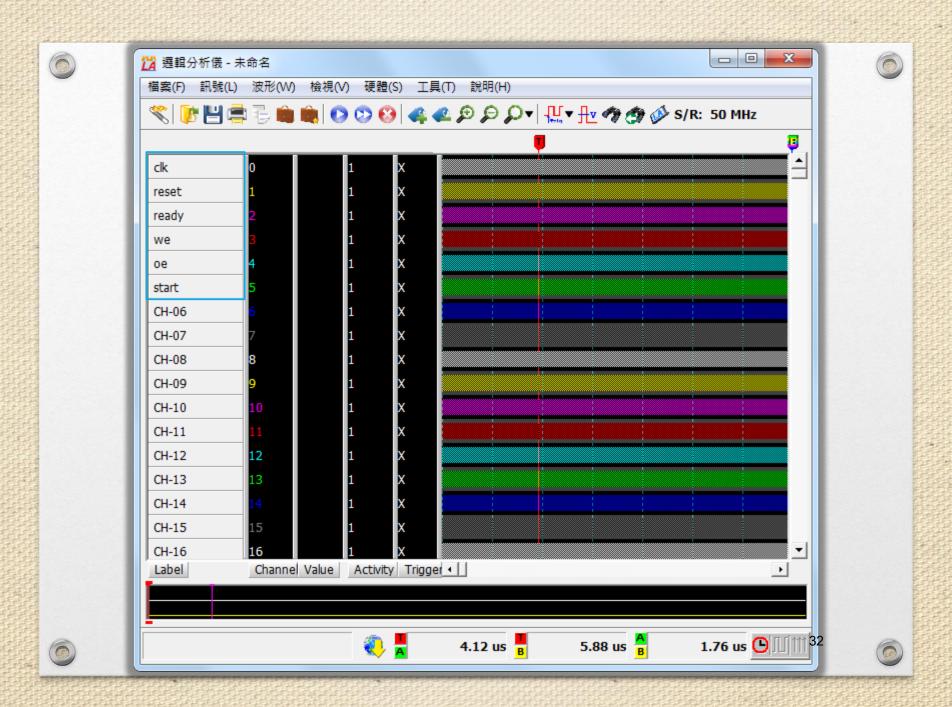
Introduction to LA

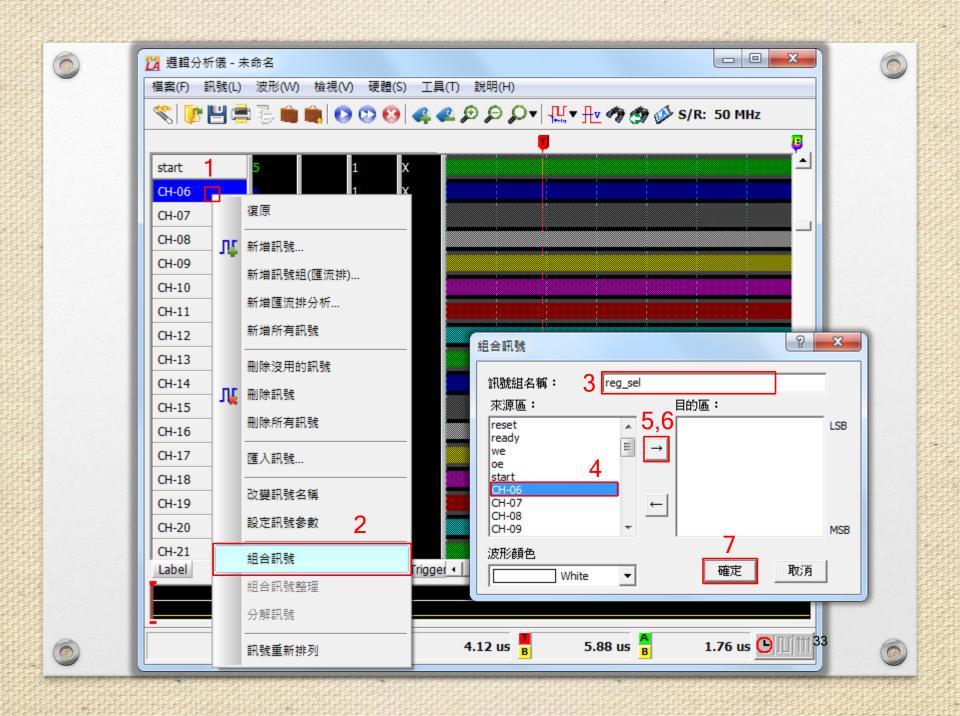
- Logic Analyzer (LA in brief) is used to observe the output signals from other devices.
- TravelLogic series (which are used in our experiments) has 36 channels.

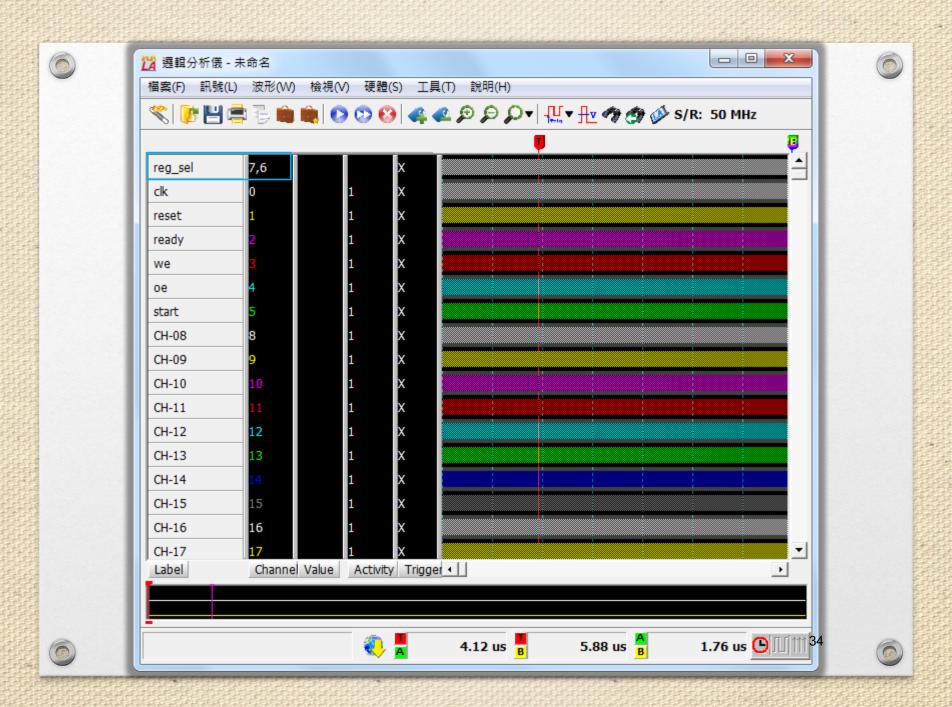


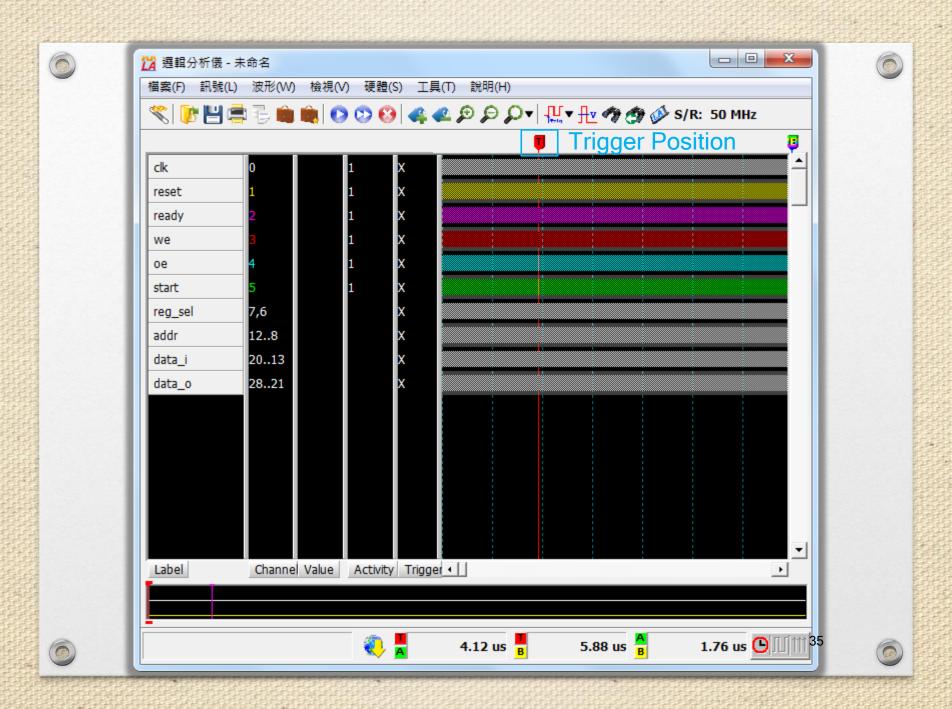






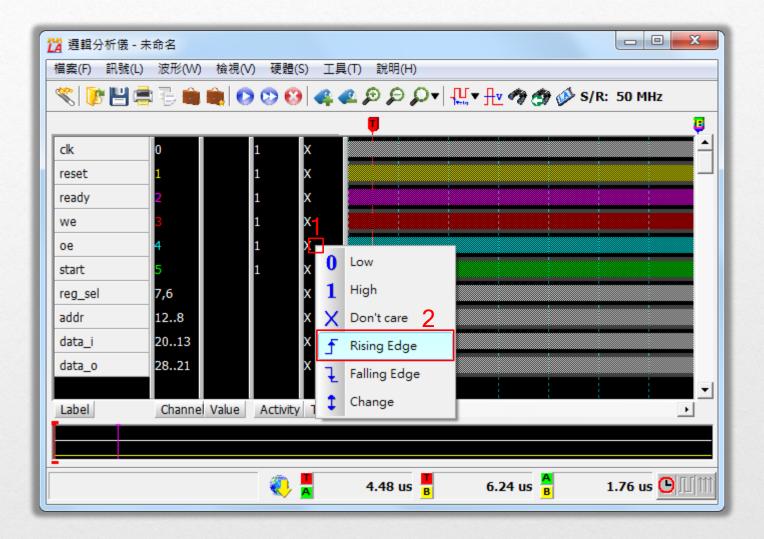










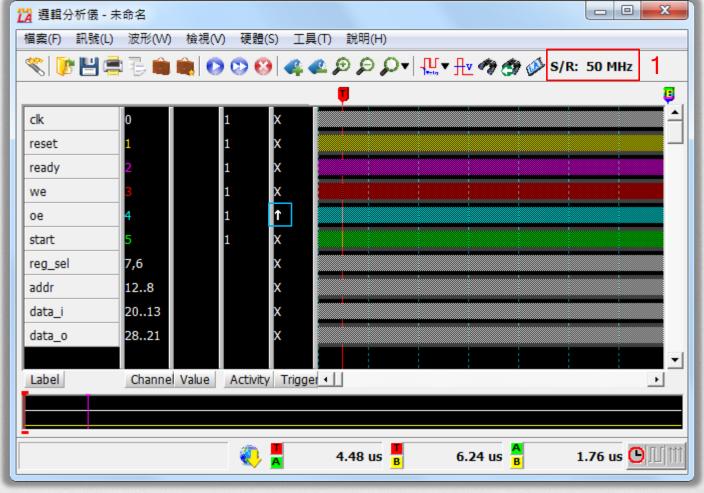










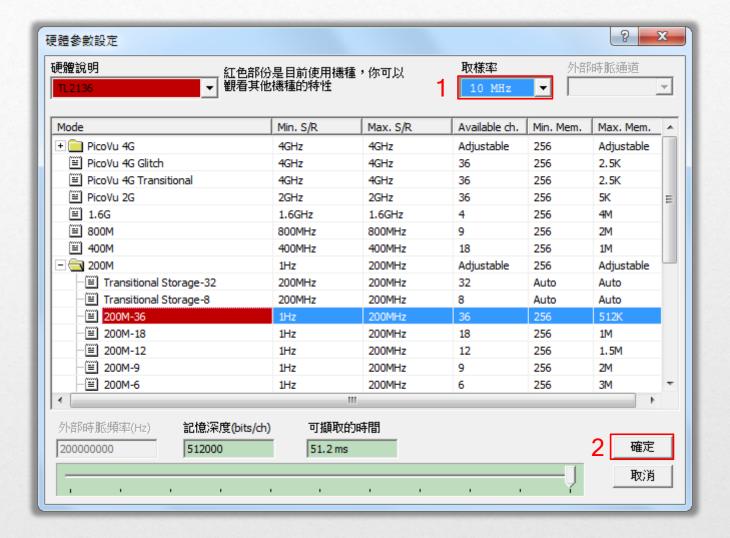










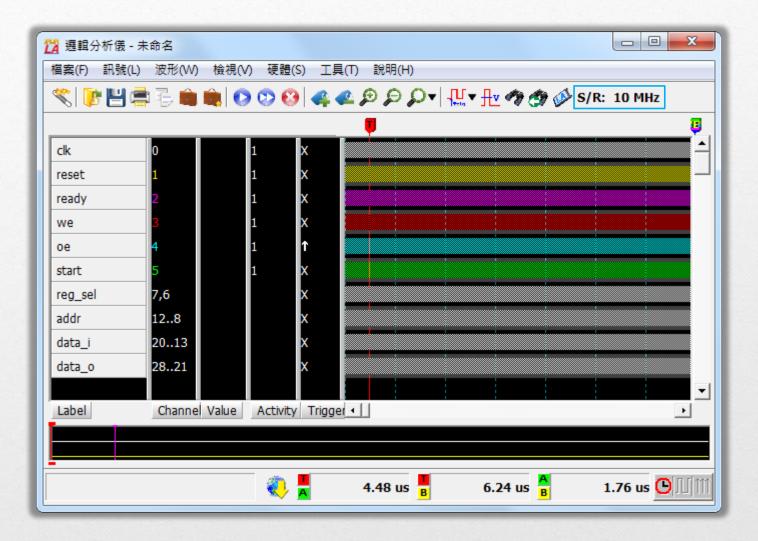




















Save LA File



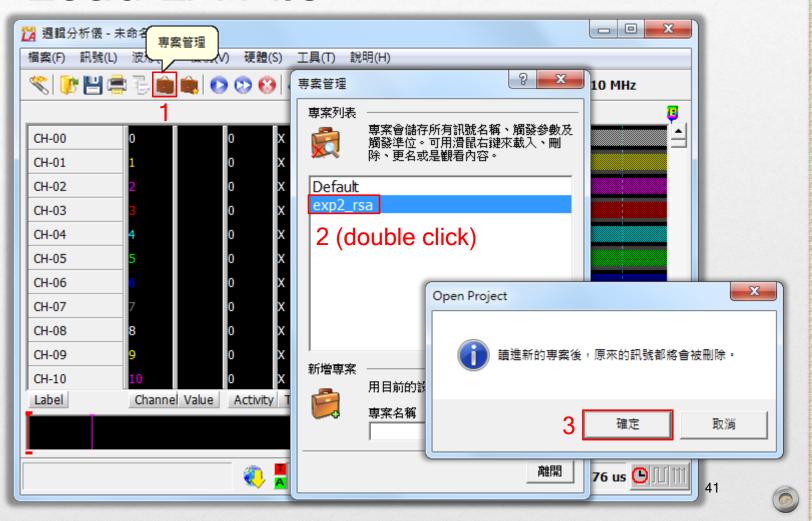








Load LA File





Complete the RSA System









System Overview

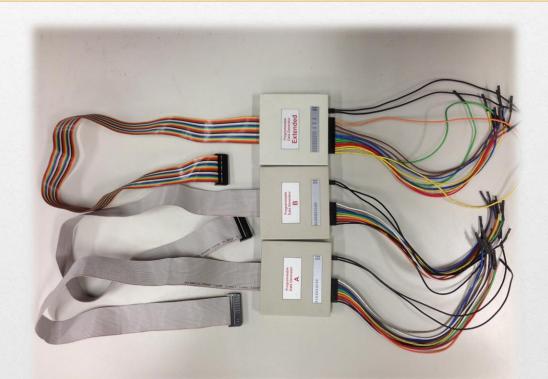








Connect PG Components (1/3)









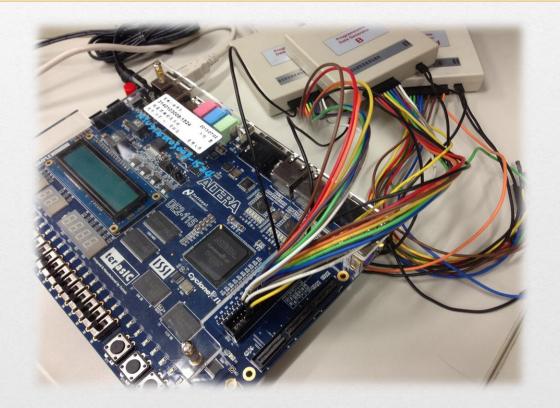
Connect PG Components (2/3)







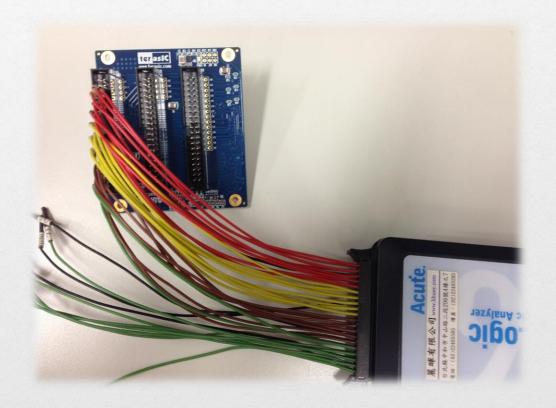
Connect PG Components (3/3)







Connect LA Components (1/2)

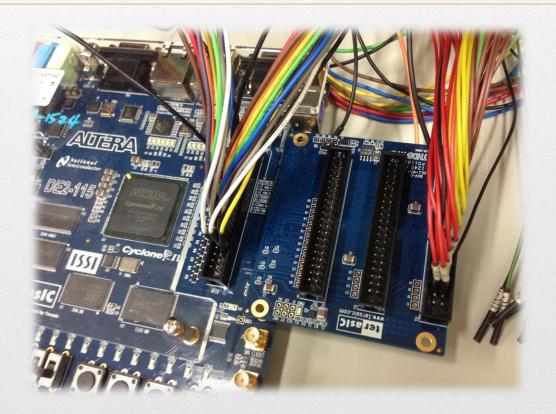








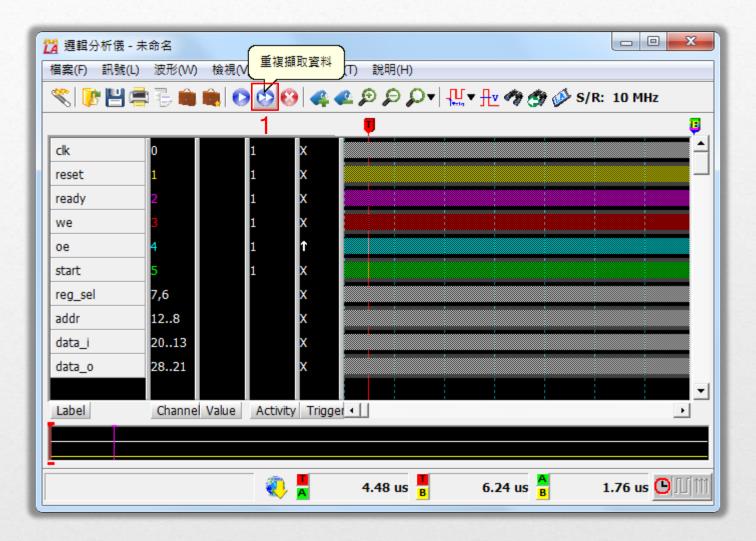
Connect LA Components (2/2)









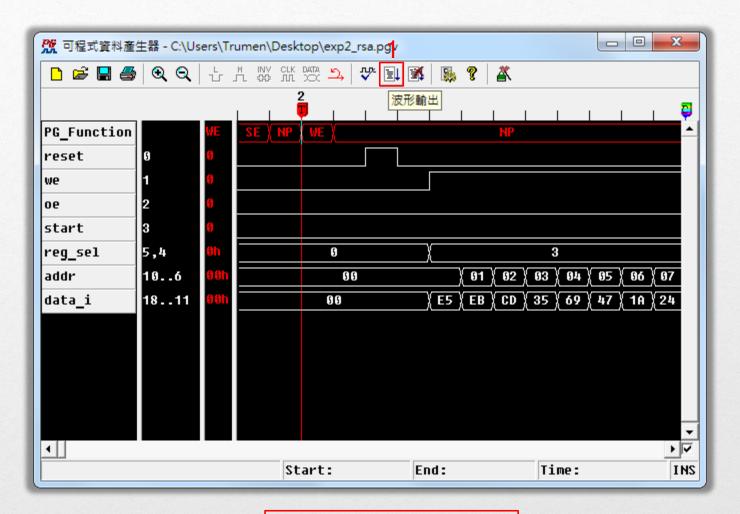












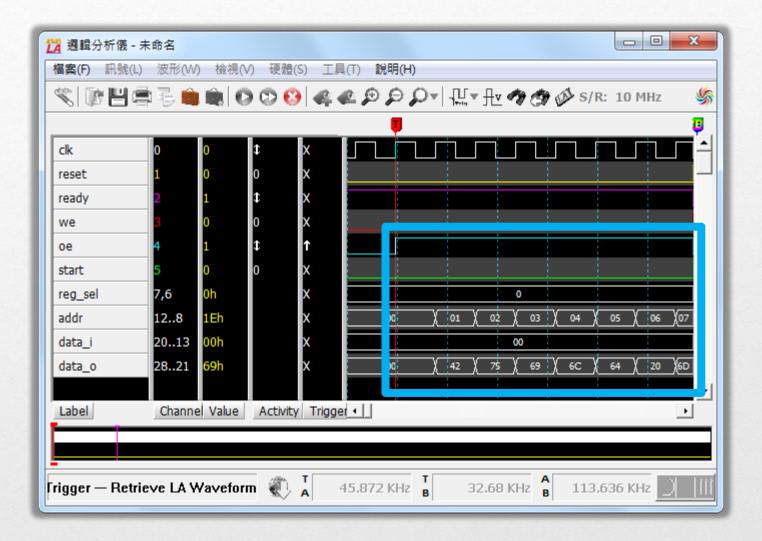
2 Push Space Key



















How to Optimize? (1/2)

- Modify the constraint file exp2_rsa.sdc and then compile again.
 - create_clock -period 500 [get_ports clk]
 derive_clock_uncertainty
 set_input_delay 0 -clock clk [all_inputs]
 set_output_delay 0 -clock clk [all_outputs]
- Change the signal frequency of PG and check if the result is still correct.
 - Don't forget to change the sampling rate of LA.
- Record the min. clock period (max freq.).









How to Optimize? (2/2)

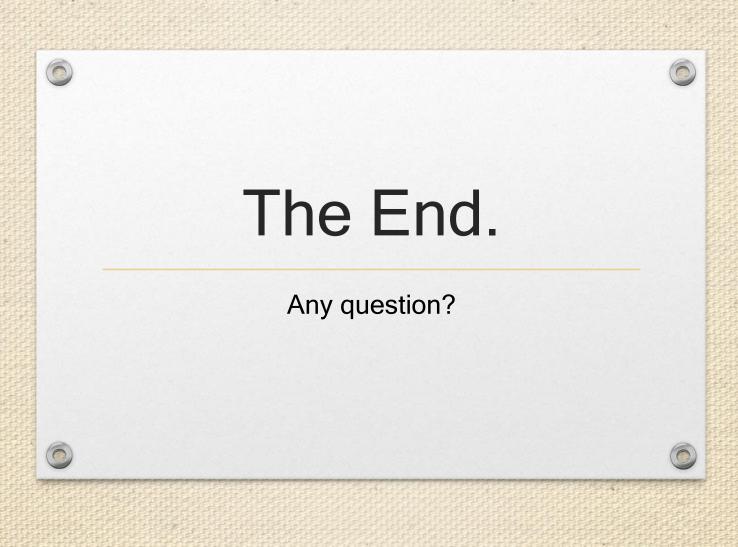
- Modify the testbench
 - clock period to min. clock period
 - TEST_DATA to 6

```
`timescale 1ns/1ps
`define CYCLE 500.0
`define End_CYCLE 1000000000
`define TOTAL_DATA 38
`define TEST_DATA 6
```

 Run the Verilog simulation to get the finish time.









Reference

- 1. "DE2-115 User Manual" by Terasic Technologies Inc.
- 2. "enPG.pdf" by Acute Technology Inc.
- 3. "enLA.pdf" by Acute Technology Inc.



