My First Nios II for Altera DE2-115 Board

0

Digital Circuit Lab

TA: Po-Chen Wu



Outline

- Hardware Design
- Nios II IDE Build Flow
- Programming the CFI Flash

Hardware Design



Introduction

 This slides provides comprehensive information that will help you understand how to create a FPGA based SOPC system implementing on your FPGA development board and run software upon it.



Required Features (1/2)

- The Nios II processor core is a soft-core central processing unit (CPU) that you could program onto an Altera field programmable gate array (FPGA).
- This chapter illustrates you to the basic flow covering hardware creation and software building.



Required Features (2/2)

- The example NIOS II standard hardware system provides the following necessary components:
 - Nios II processor core, that's where the software will be executed.
 - On-chip memory to store and run the software.
 - JTAG link for communication between the host computer and target.
 - Hardware (typically using a USB-Blaster cable).
 - LED peripheral I/O (PIO), be used as indicators.



Creation of Hardware Design



10	New	Proi	iect	Wi	zard	
23	New	PIO	ect.	VVI.	zaru	

Directory, Name, Top-Level Entity [page 1 of 5]

	What is the wo	orking directory for this project?	
1	C:/Users/Trun	men/Desktop/Project	
	What is the na	ame of this project?	
2	NiosII	same as (top-level) file name	
	What is the na	ame of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.	
	NiosII		
	Use Existing P	Project Settings	
-		3	
		< Back Next > Finish Cancel Aelp	
L			

X

🚳 New Project Wizard

Add Files [page 2 of 5]

Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project. Note: you can always add design files to the project later.

ile name:									Add
ile Name	Туре	Library	Design Entry/Synthesis Tool	HDL Vers	ion				Add All
									Remove
									Up
									Down
									Properties
ecify the p	oath nan	nes of any	y non-default libraries. User L	ibraries					
						1			
					< Back	Next >	Finish	Cancel	Help

х

🍓 New Project Wizard

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation. You can install additional device support with the Install Devices command on the Tools menu.

Device family	1	Show in 'Availa	ble devices' list
Family: Cyclone IV E	•	Package:	Any 🔹
Devices: All	-	Pin count:	Any 🔹
Target device		Speed grade:	Any 🔹
Auto device selected by the Fitter		Name filter:	
 Specific device selected in 'Available devices' list 		V Show adva	nced devices HardCopy compatible only
Other: n/a			

х

Ŧ

1 Aelp

Cancel

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit element	s PL	L ^
EP4CE115F23C9L	1.0V	114480	281	3981312	532	4	
EP4CE115F23I7	1.2V	114480	281	3981312	532	4	2
EP4CE115F23I8L	1.0V	114480	281	3981312	532 for DE2-115	4	_2
EP4CE115F29C7	1.2V	114480	529	3981312	532	4	
EP4CE115F29C8	1.2V	114480	529	3981312	532	4	
EP4CE115F29C8L	1.0V	114480	529	3981312	532	4	
EP4CE115E29C9	1 OV	114480	529	3981312	532	4	Ŧ
•						•	

Companion device

HardCopy:

Limit DSP & RAM to HardCopy device resources

< Back	

Next >

3

Finish

🚳 Quartus II 64-Bit - C:/Users/Trumen/Desktop/Proj	ject/l	NiosII - NiosII			NAC AL	
File Edit View Project Assignments Processing	Tools	s Window Help 🐬		1	Se	earch altera.com
	<u>گر</u>	Run Simulation Tool Launch Simulation Library Launch Design Space Exp	▶ v Compiler blorer	ĕ⊘ ∞ ► v≷ 10 0	⊳ ₽	" 🧞 🧼 🦥 🚣 🔹
Project Navigator						
Entit	0	TimeQuest Timing Analyz	er			
Cyclone IV E: EP4CE115F29C7 NiosTL 47		Advisors	•			
	🧼 🔁	Chip Planner Design Partition Planner Netlist Viewers	۶.			
•	n	SignalTap II Logic Analyz	er			
A Hierarchy 📄 Files 🗗 Design Units 🔆 IF		In-System Memory Conte	ent Editor			- 0
Logic Analyzer Interface Editor		Editor		Τ		
	01	In-System Sources and P	robes Editor		J	J II
Flow: Compliation	1005	SignalProbe Pins				Version 13.0
Task		Programmer			~	View Quartus II
4 > Compile Design		JTAG Chain Debugger			G	Information
Analysis & Synthesis	<u>बड</u> बाइ	External Memory Interfa	ce Toolkit		•	Documentation
		external henory interna			•	Notification Center
	1	MegaWizard Plug-In Man	ager			
All 😢 🖾 🙆 😽 🔻 < <search>></search>		Nios II Software Build To	ols for Eclipse			
7 Type ID Message		Qsys	2			
	0	Tcl Scripts				
10		Customize				
		Options				11
System / Processing / License Setup						
Starts Qsys System Integration Tool		Install Devices				0% 00:00:00 _{1.1}

4)sys								x
File	Edit System View Tools Help		1						
	New System	Ctrl+N	ct Settings	Instance Paramet	ers	System Inspector	HDL Example	Generation	n
	New Component		System C	ontents		Address Map	Clock Se	ettings	
	Open	Ctrl+O	Conn N	ame	Des	cription	Export		Clc
	Save	· /==				×			
	Save As 2	🦕 1881 7					clk		
	Refresh System	儲	字於: 🕕 Pr	oject	-	🤌 📂 🖽 📟	Double-clic	k to export	clk_
	Export System as hw.tcl Compor		🔒 db				Double-clic	k to export	
	Browse Project Directory	24							
	biolise riejeer birectory	最近的项	目						
	Exit								
	Memories and Memory Contro								
Ē	Merlin Components	泉田							
	-Microcontroller Peripherals								
)···PLL	我的文	件						
	-Qsys Interconnect								
		-	檔案名稱	稱: DE2_115_QSYS		3 儲存(S)	4		
		電腦	檔案類	딸 : Qsvs System File	s (*.asvs	。 ▼ 取消			
									•
Mes	sages								
De	scription					Path			
0.54	rore O.Warninge							10	
	rors, o warnings								
									-

& Qsys - DE2_115_QSYS.qsys (C:\Use File Edit System View Tools Help	ers\Trumen\	\Desktop\	\Project\DE	2_115_QSYS.qsys)			
Component Library	Project \$	Settings System	Insta Contents	nce Parameters	System Inspec Address Map	ctor HDL Example Clock	Generation Settings
Project	₩ Use	Conn	Name	De	scription ck Source	Export	Clc
Library 		×		Connections Filter Edit Rename 2 Duplicate Remove Details Show Arbitration S	Ctrl+E Ctrl+R Ctrl+D	clk reset Double-d Double-d	lick to export clk_ lick to export
⊕PLL Qsys Interconnect Verification New Edit Add	•		* ©	Lock Base Addres Expand All Collapse All Set Color	\$		4
Messages Description				Print	Path		
0 Errors, 0 Warnings							13



A: Qoys - DE2_115_QSYS.qoys* (C:Users\Trumen\Desktop\Project)DE2_115_QSYS.qoys) File Edit System View Tools Help Component Library Project Settings Interview	<i>\</i>								
File Edit System View Tools Help Component Library Project Wex Component Library System Contents Address Map Project Wex Component Library System Contents Address Map Project Wex Component Library System Contents Address Map Project Wex Config-Expanses Project System Contents Project Wex Config-Expanses Bridges Config-Expanses Config-Expanses Project and Reset Bridges Cock and Reset Bridges Configuration & Programming Bridges Cotor and Reset Bridges Cot	🚣 Qsys - DE2_115_QSYS.qsys* (C:\U	sers\Trume	n\Desktop\Proj	ject\D	E2_115_QSYS.qsy	5)			
Component Library Project Settings Instance Parameters System inspector HDL Example Generation System Contents Address Map Clock Settings Project System Contents Address Map Clock Settings Project New Component Use Connections Name Description Export Library Config-Bypass App Exam Clock Surce Clock Input ck, in reset Clock Output Clock Settings B- Glock and Reset Config-Bypass App Exam Image Set Input Clock Settings Clock Source Clock Input B- Clock and Reset Config-Bypass App Exam Image Set Input Clock reset Reset Input Clock Couput Double-click to Doub	File Edit System View Tools Help								
System Contents Address Map Clock Settings Project System Contents Address Map Clock Settings Project System Contents Name Description Export Bridges Clock Settings Clock Settings Clock Settings Bridges Clock and Reset Clock Settings Clock Input Clock Settings Bridges Clock and Reset Clock Settings Clock Settings Bridges Clock and Reset Clock Settings Clock Input Clock Input Bridges Clock and Reset Clock Settings Clock Input Clock Input <t< td=""><td>Component Library</td><td>Project</td><td>Settings</td><td>Inst</td><td>ance Parameters</td><td></td><td>System Inspector</td><td>HDL Examp</td><td>le Generation</td></t<>	Component Library	Project	Settings	Inst	ance Parameters		System Inspector	HDL Examp	le Generation
Image: Connections Name Description Export Image: Connections Name Description Double-click to			System Conte	nts		A	ddress Map	CI	ock Settings
Project Use Connections Name Description Export Ibrary New Component Ibrary Clock Source Cloco Source Clock Source	🔍 🗙								
Wew Component Library •• Config-Bypass App Exar •• Cridges •• Configuration & Programming •• Custom Instruction Int •• Reast Processor •• Hard Processor •• Hard Processor •• Hard Processor •• Edt •• The Processor •• Edt •• Flag Double-click to c Double-click to c	Project	Use	Connections		Name		Description		Export
Library Config-Bypass App Exar Cik_in_reset Cick input Reset Input Bridges Config-Bypass App Exar Cik_in_reset Cick input Reset Input Bridges Configuration & Programming Image: Configuration & Prog	New Component	A 🖉			⊟ clk_50		Clock Source		
• Colling-System App Examples • Double-Click to C	Library				clk_in		Clock Input Reset Input		Clk
Bridges and Adapters Cik_reset Reset Output Double-click to to to Double-click to to Double-click to to Double-click to to Double-click to Double-	H-Bridges		L — Ť		clk		Clock Output		Double-click to a
 Clock and Reset Configuration & Programming Consume instruction instruction instruction Clast master instruction_mast flag_debug_mod Custom instruction Si Custom instruction Si Custom instruction Si Floating Point Hardway Hard Processor System Hard Processor System Hard Processor System Hard Processor System Edit Custom instruction Si Floating Point Hardway Hard Processor System Edit Custom instruction Shares Collapse All Set Color Print Totom State Stave is not specified. Please select the reset slave Herrors, 0 Warnings 					clk_reset		Reset Output		Double-click to e
Configuration & Programming B-DSP E-Embedded Processors • • Bitswap • • Custom Instruction Int • • Custom Instruction Me • • Edit • • Hard Processor System • Interfere Protocols • Interfere Protocols • New Edit • Hard Processor System • Interfere Protocols • Interfere Protocols • Interfere Protocols • Edit • Custom Instruction Shares • Interfere Protocols • Interfere Protocols • Edit • Custom Instruction Shares • Lock Base Address • Expand All • Collapse All • Expand All • Set Color • Set Color • Print • Etrors, 0 Warnings	E ⊡ Clock and Reset	▼ ▼			■ nios2_qsys_0	01	Miss II Drassager		
Wessages Messages	Configuration & Programming	×		\rightarrow	Clk reset n		Connections		Double-click to e
Bits wap Custom Instruction Int Custom Instruction Mi Custom Instruction Si Floating Point Hardway Hard Processor System Nios Il Processor Nos Il Processor Messages Messages Description Add Messages Edit Collapse All Collapse All Set Color Set Color Print	Embedded Processors	· 👦			data master	8	Filter	•	Double-click to e
Image: Sect slave is not specified. Please select the reset slave	Bitswap	ш			instruction_ma	st			Double-click to e
Image: Custom Instruction Mit Image: Custom Instruction Site	····· Custom Instruction Int				jtag_debug_mo	d 🐼	Edit	Ctrl+E	Double-click to (
Image: Second state	Custom Instruction Ma Custom Instruction Ma		· ••		jtag_debug_mo	d 🦉	Rename 2	Ctrl+R	Double-click to e
Hard Processor Systi Image: New Edit Image: Add Messages Description Image: Set Color <	Custom Instruction Si Floating Point Hardwa		1	~ ``	custom_instruc		Duplicate	Ctrl+D	Double-click to e
Nos I Processor Image: New Edit Image: Messages Description Image: Image: <t< td=""><td>- Hard Processor Syste</td><td></td><td></td><td></td><td></td><td>×</td><td>Remove</td><td></td><td></td></t<>	- Hard Processor Syste					×	Remove		
Image: Interface Protocols Image: Interface Protocols New Edit Image: Interface Protocols New Edit Image: Interface Protocols	Nios Il Processor						Details	•	
New Edit Messages Lock Base Address Messages Expand All Description Collapse All News Set Color State slave is not specified. Please select the reset slave 4 Errors, 0 Warnings	Interface Protocols								
New Edit Add III Messages Expand All Description Collapse All Sectors Set Color Set Color Set Color Vertors, 0 Warnings III							Show Arbitration Share	s	
Messages Description <lu> <lu> <lu> <lu> <lu> <lu> <lu< td=""><td>New Edit</td><td>•</td><td></td><td></td><td>III</td><td>•</td><td>Lock Base Address</td><td></td><td>4</td></lu<></lu></lu></lu></lu></lu></lu>	New Edit	•			III	•	Lock Base Address		4
Messages Collapse All Description Image: Collapse All Image: Collapse All <							Expand All		
Description Image: Collapse All Image: Collapse All Image: Collapse All Image: Colla	Messages						Colleges All		
Set Color Set Color Reset slave is not specified. Please select the reset slave 4 Errors, 0 Warnings	Description					48	Collapse All		
Reset slave is not specified. Please select the reset slave Print 4 Errors, 0 Warnings 15	E 🔀 4 Errors					•	Set Color		
4 Errors, 0 Warnings 15	🛛 Reset slave is not specified. Pleas	e select the re	eset slave				Print		-
	4 Errors, 0 Warnings								15

L Osvs - DE2 115 OSVS asvs* (C·\L	Jsers\Trumen\Deskton\Project\C	E2 115 OSVS asvs)		
File Edit System View Tools Help	sers (numen besktop (noject (b	/22_113_Q313.q3y3)	/	
Component Library	Project Settings Insi	tance Parameters	System Inspector	HDL Example Generation
	System Contents		Address Map	Clock Settings
interface Protocols	Use Connections	Name	Description	Export
		Clk_in_ clk_in_reset clk clk_reset nios2_qsys clk reset_n JTAG UART Write FIFO Buffer depth IRQ threshol Constru	Clock Source Clock Input Reset Input Clock Output Reset Output Nios II Processor Clock Input Reset Input Clock Input T - jtag_uart_0 TAG UART era_avalon_jtag_uart O(Data from Avalon to JTAC h (bytes): 64 • Id: 8	clk reset Double-click to Double-click to Double-click to Double-click to
Description				
E 🔀 2 Errors				Cancel
Reset slave is not specified. Pleas 2 Errors, 0 Warnings	se select the reset slave	(System.nios2_qsys	16



Osvs - DE2 115 OSVS asvs* (C:\Users\Trumen)	Deskton/Project/DE2 115 OSVS asy	(c)	
File Edit System View Toole Help	(Deskip) (10jeer (D22_115_Q313.43)	On-Chip Memory (RAM or ROM) - onchip	×
Component Library Component Library	Project Settings Instance System Contents	On-Chip Memory (RAM or ROM) attera_avalon_onchip_memory2 Size Data width: 32 Total memory size: 3 204800 Cancel Cancel Cancel Cancel Cancel Cancel Cancel Cancel Cancel Cancel Cancel Cancel Cancel Can	eration Documente Export Clk reset Docu
Messages			
Description		Path	
Errors			^
Reset slave is not specified. Please select the res	et slave	System.nios2_qsys	10
2 chors, r warning			١٥



Component Library	Project Settings Instance Parameters System					spector	HDL Example	Gener	ation
		System C	ontents		Address Map	0	Clock	Settings	
Bridges and Adapters Clock and Reset Clock and Reset Configuration & Programming DSP Embedded Processors Interface Protocols Memories and Memory Controllers		Use Connections Na			et s ter _master g_module_re g_module struction_m g_slave emory2_0	Description LIOCK INPUT Reset Input Clock Outpu Reset Outpu Nios II Proce Clock Input Reset Input Avalon Men Avalon Men Custom Inst JTAG UART Clock Input Reset Input Avalon Men Custom Inst	n ut ut essor nory Mapped Master nory Mapped Slave ruction Master r nory Mapped Slave mory (RAM or RO)	er er er	Ex CIK res L L L L L L L L L L L L
New Edit				clk1 s1 reset1	<pre></pre>	Conner Filter	ctions	•	
Messages					G	Edit	^{ne} 2	Ctrl+E Ctrl+R	Ē
Description				Path		Duplica	ate	Ctrl+D	
Keset slave is not specified. Please select the reader of the reade	set slave			System	nios2_qsys	Remov	e	,	· •
4 Errors, 2 Warnings						Show	Arbitration Shares	19	

Nios II Processor - nios2_qsys		×		00866	100000000	相關的資源	anaananana a	oonnon C
Nios II Processor attera_nios2_qsys		Documentation	SYS.qs	ys)				
Reset Vector		-	ce Para	meters	System In:	spector	HDL Example	Generation
Reset vector memory:	onchip_memory2.s1	3 -			Address ma	P	CIDCK 30	ungs
Reset vector offset:	0x0000000		Nam	e		Description		Ex
Reset vector:	0×0000000		÷ ≺	cik_in clk_in_res clk	et	CIOCK INPUT Reset Input Clock Outpu	t	res
Exception Vector		1		clk_reset		Reset Outpu	ıt	L
Exception vector memory: Exception vector offset: Exception vector:	onchip_memory2.s1 0x00000020 0x00000020	4		clk reset_n 4 data_masi instruction jtag_debug jtag_debug custom_in tag_uart clk reset avalon_jta onchip_me	s 2(double-click) ter g_module_re g_module struction_m g_slave emory2	Clock Input Reset Input Avalon Mem Avalon Mem Reset Outpu Avalon Mem Custom Inst JTAG UART Clock Input Reset Input Avalon Mem On-Chip Mei	nory Mapped Master nory Mapped Master nory Mapped Slave ruction Master nory Mapped Slave mory Mapped Slave	
New Edit Messages Description	Add		> 	Path		Reset Input		•
EX 7 Errors								
Reset slave is not specified. 7 Errors, 1 Warning	Please select the reset sla	ve		System	.nios2_qsys		2	.0

	1						
Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\De	esktop\Project\	DE2_115_QSYS	s.qsys)				
File Edit System View Tools Help							
Component Library	Project Settings	Instance	Parameters	System Inspector	HDL Exam	nple Ger	neration
	System	o Contents		Address Map	C	lock Settings	
🔍 🔍 🕺	L						
Herlin Components	Use Conne	ections	Name	Descri	ption	_	Ex
Microcontroller Peripherals	S 🔽 🚺 📜	System ID Peri	ipheral - sysic	d gsys 0	×		
Peripherals		-				n	CIK
Altera Avalon Data Pattern Chec	s -	Sys	tem ID				l
Altera Avalon Data Pattern Gene 4		Dori	inhoral				L
Avalon-ST Test Pattern Checker	~ ~	attera	avalon eveid <i>i</i>		ocumentation		
Avalon-ST Test Pattern Generat Gonduit splitter		altera_	_avalon_sysia_	daya			4
Gondal spinter Frequency Counter	2	* Parameters			•	ister	Ĺ
Performance Counter Unit	·	32 bit System ID	: 0x00000000			ister	∠ ≡
System ID Peripheral							L
Herein Controller Peripherals (double-click)		* Description				ave	2
		Please use hexa	adecimal numbe	rs only in System ID.			
Gys Interconnect							L
Window Bridge							L
						- IOM)	L
					2		L
New Edit						IVE	•
				Cancel	Finish		
Messages							
Description			Path				
S Errors							*
Sonchip_memory2.s1 (0x00x3fff) overlaps jtag	uart.avalon_jtag	j_slave (0x00x7	7) System.	nios2_qsys.data_mas	ter		-
5 Errors, 1 Warning						21	



Component Library	Project Settings Instance Parameters Sy				System I	nspector	HDL Exa	mple	Generation
		System C	ontents		Address M	ар		Clock Settin	gs
Merlin Components Microcontroller Peripherals Debug and Performance Altera Avalon Data Pattern Checker Avalon-ST Test Pattern Generat Conduit splitter Frequency Counter Performance Counter Unit System ID Peripheral Display Microcontroller Peripherals Osystanterconnect Window Bridge New Edit	Use Use Use V V V V V V V V	Connect	ions Na	me nios2_qsys clk reset_n data_master instruction_m jtag_debug_r jtag_debug_r custom_instr jtag_uart clk reset avalon_jtag_i onchip_mem clk1 s1 reset1 sysid_qsys_ clk reset control_slave	naster module_re module ruction_m slave nory2	Description NIOS II Proce Clock Input Reset Input Avalon Mem Avalon Mem Custom Inst JTAG UART Clock Input Reset Input Avalon Mem On-Chip Me Clock Input Avalon Mem Reset Input System ID P Connections Filter Edit	nory Mapped nory Mapped ut nory Mapped ruction Master mory Mapped mory (RAM of nory Mapped Peripheral	Master Master Slave er Slave or ROM) Slave	
Messages						Rename	2	Ctrl+R	
Description				Path		Duplicate		Ctrl+D	
🗆 😢 7 Errors					×	Remove			^
onchip_memory2.s1 (0x00x3ffff) overlaps jt	tag_uart.ava	lon_jtag_s	alave (0x00x7)	System.nic	os2_	Details		I	-
7 Errors, 2 Warnings						Show Arbitr	ation Shares	22	

		👃 PIO (Parallel I/O) - pio_0	×	0050000000
& Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen) File Edit System View Tools Help	\Desktop\Project\DE	PIO (Parallel		
Component Library	Project Settings System Co	I/O) altera_avalon_pio	Documentation	e Generation ck Settings Ex Ex ster t ster t ave
Memories and Memory Controllers Merlin Components Microcontroller Peripherals Debug and Performance Display Microcontroller Peripherals Microcontroller Peripherals Microcontroller Peripherals Microcontroller Peripherals Microcontroller Peripherals Vectored Interrupt Controller Vectored Interrupt Controller		S S S S S reset1 S S C k reset	Output Output Output Output Second State System ID Peripheral Clock Input Reset Input	ave d IOM) Nave d I
New Edit	↓ ↓ ↓	iii control_slave	Avalon Memory Mapped S	Slave L ▼
Messages				
Description		Path		
onchip_memory2.s1 (0x00x3ffff) overlaps jta 7 Errors, 1 Warning	ag_uart.avalon_jtag_sla	ve (0x00x7) System.nios2_qs	ys.data_master	- 23



Component Library	Project S	ettings Ins	stance Paramet	ers	System Inspector	HDL Example	Generation
		System Contents		1	Address Map	Cloc	k Settings
Contig-Bypass App Example	Use Use Use V V V V V V V V V	Connections	Name)_aeoug_n)_debug_n stom_instru _uart eet alon_itag_s hip_mem 1 set1 d asvs	Descripti nodule_re Reset Ou nodule Avalon M uction_m Custom In JTAG UA Clock Inpu Reset Inp slave Avalon M Ory2 On-Chip I Clock Inpu Avalon M Reset Inp System ID	ion tput emory Mapped Sla istruction Master RT ut emory Mapped Sla Memory (RAM or Ri ut emory Mapped Sla ut) Peripheral	ve L DM) ve L
Debug and Performance Display Microcontroller Peripherals Microcontroller Vo) PlO (Parallel VO) Vectored Interrupt Controller Vectored Interrupt Controller Rew Edit			ightarrow s1	a_qsys	Clock Inpu Reset Inpu Avalon M PIO (Para Connections Filter	Peripheral ut emory Mapped Sla liel VO)	ve
		ſ	II		Edit	Ctrl+E	4
Messages					Rename 2 Duplicate	Ctrl+R Ctrl+D	
Description				Path 🗙	Remove		
🗆 🔀 9 Errors					Details	•	A
Sonchip_memory2.s1 (0x00x3ffff) overlaps jt 9 Errors, 3 Warnings	tag_uart.aval	on_jtag_slave (0)x00x7)	Syster	Show Arbitration S	Ghares	24



Component Library	P	Project Settings Instance Paran			Parameters	System Ir	spector	HDL Example	Generation
			System Co	ontents		Address Ma	ар	Clock Se	ttings
Contig-Bypass App Example		Use V	Connecti	ions	Name Jtag_debu custom_i jtag_uart clk reset avalon_it onchip_m clk1 s1 reset1 sysid_qsy clk reset	ug_module_re ug_module nstruction_m ag_slave nemory2	Description Reset Outp Avalon Mer Custom Inst JTAG UAR Clock Input Reset Input Avalon Mer Clock Input Avalon Mer Reset Input System ID F Clock Input Reset Input	n ut nory Mapped Slave truction Master F mory Mapped Slave emory (RAM or ROM) nory Mapped Slave Peripheral	
New Edit Messages Description		 ✓ ✓ 			Control_s clk reset s1 external_	connection	Avalon Men PIO (Paralle Clock Input Reset Input Avalon Men Conduit	nory Mapped Slave	
	itaa wa	rt avel	on itaa a	lave (0x0_0	(7) System	n nins2 asvs d	ata master		-
9 Errors, 2 Warnings	jtag_0a	rcaval	on_jtag_s	nave (0x00)	(r) System		ata_master	2	5

File Edit System View Tools Help

Component Library	Project Settings	Instance Paramete	ers System Inspector	HDL Example	Generation
	System Co	ontents	Address Map	Clock Se	ttings
Contig-Bypass App Example	Name		Description	Export	lists for sum a
		itag_debug_module Avalon Memory Mapped Slave Double itag_debug_module Custom Instruction Master Double			
		_uart set alon itan slave	Clock Input Reset Input Avalon Memory Manned Slave	Double-c Double-c Double-c	lick to expc lick to expc lick to expc
Memories and Memory Controllers Merlin Components Microcontroller Peripherals	▼ □ onc ♥ → clk S1 s1	hip_memory2	On-Chip Memory (RAM or ROM) Clock Input Avalon Memory Mapped Slave	Double-c Double-c	lick to expc lick to expc
Peripherals Debug and Performance Display Microcontroller Peripherals	Clk	set1 id_qsys set	Reset Input System ID Peripheral Clock Input Reset Input	Double-c Double-c Double-c	lick to expc lick to expc lick to expc ≡
Interval Timer PIO (Parallel I/O) Vectored Interrupt Controller PLL	Co	ntrol_slave set	Avalon Memory Mapped Slave PIO (Parallel I/O) Clock Input Reset Input	Double-c Double-c Double-c	lick to expc lick to expc lick to expc
	→ s1		Avalon Memory Mapped Slave	Double-c	lick to expc
New Edit	ex	ternal_connection	Conduit	led	*
Messages					
Description			Path		
🗆 🔀 9 Errors					*
Sonchip_memory2.s1 (0x00x3ffff) overlaps jt 9 Errors, 2 Warnings	tag_uart.avalon_jtag_s	System.nios2_qsys.data_master	2	6	

L Osvs -	DE2 115 OSYS asys* (C:\User	s\Trumen\Deski	top\Proie	ct\DE2 115 OSYS asy	s)			0 X
File Edit	System View Tools Help				-,			
Compon	Upgrade IP Cores		viect Settin	ns Instance Parar	neters Sv	stem Inspector	HDI Example	Generation
		•	Sys	tem Contents	Addr	ress Map	Clock Settin	las
	Assign Base Addresses	2						.90
	Assign Interrupt Numbers		N	ame	Description		Export	
€··Bri	Assign Custom Instruction Op	codes		jtag_debug_module_r	e Reset Output		Double-clic	ck to expc 🔒
Bric	Create Global Reset Network			jtag_debug_module	Avalon Memor	y Mapped Slave	Double-clic	ck to expc
				custom_instruction_m	Custom Instruc	ction Master	Double-clic	ck to expc
	Show System With Qsys Fabr	ic Components		jtag_uart	Clock Input		Daubla ali	la tra curra
	Run SOPC Builder to Osys Un	arade	\rightarrow	reset	Reset Input		Double-clic Double-clic	ck to expc
	Run Sone Builder to days op	grade	\longrightarrow	avalon itag slave	Avalon Memor	v Mapped Slave	Double-clic	ck to expc
÷Me	Remove Dangling Connections	i	E	onchip_memory2	On-Chip Memo	ry (RAM or ROM)	Double one	
iten	in components		$ \longrightarrow $	clk1	Clock Input		Double-clic	k to expc
⊕Micn	ocontroller Peripherals	- Y -	\longrightarrow	s1	Avalon Memor	y Mapped Slave	Double-clic	ck to expc
- Perip	pherals		\rightarrow	reset1	Reset Input		Double-clic	ck to expc
	Debug and Performance			sysid_qsys	System ID Peri	ipheral		
• • • • •	Display			Clk	Clock Input		Double-clic	ck to expc
	Microcontroller Peripherals			reset	Reset input	w Mannad Slava	Double-clic	ck to expc
	Interval Timer Rio (Parallel I/O)			led	PIO (Parallel I/C		Double-clic	CK to expc
	Vectored Interrupt Controller			clk	Clock Input	- /	Double-cliv	ck to expr
		- I I	\rightarrow	reset	Reset Input		Double-clic	k to expc
			\longrightarrow	s1	Avalon Memor	y Mapped Slave	Double-clic	k to expc
New	Edit	bbd		external_connection	Conduit		led	-
			•	III				•
Messages	\$ 							
Descripti	on				Path			
🗆 🔀 9 Err	rors							
🔀 on	chip memory2.s1 (0x00x3ffff)	overlaps itaq uar	t.avalon i	tag slave (0x00x7)	System.nios2	qsys.data_master		-
9 Errors,	1 Warning						27	



Component Library	Project S	ettings	ameters	System In	specto	or	HD	HDL Example Clock Sett			eneratior	n	
		System Con	itents		Address Ma	ър			(Clock S	ettings		
Contig-Bypass App Example	🖶 Use	Connection	ns Na	me		D	E	Cl	В	End	IRQ	Орсос	٦
				clk_reset nios2_qsys	5	Re Nio	Doub						^
Configuration & Programming DSP Embedded Processors				clk reset_n data_maste instruction	er master	Clo Re Av Av	Doub Doub Doub Doub	CIK [clk] [clk] [clk]	IRQ O	IR	\leftarrow		
	X			jtag_debug jtag_debug custom_ins	_ I_module_re I_module struction_m	Re Av Cu	Doub Doub Doub	[clk] [clk]	₽.	.0x			Ш
Peripherals Debug and Performance Display				jtag_uart clk reset avalon_itar	n slave	JT Clo Re	Doub Doub	cik [cik] [cik]	-	0×		7 1	
		+ + + + + + + + + + + + + + + + + + +		onchip_me clk1 s1	mory2	On Clo Av	Doub Doub	clk [clk1]	.	.0x			
New Edit				reset1 sysid_qsys clk	\$	Re Sy Clo	Doub	[clk1]					Ŧ
	•			111								F.	
Messages													
Description				Path									
⊟ 📐 1 Warning													^
A Interrupt sender jtag_uart.irq is not connected t	o an interrupt	receiver		System.j	tag_uart						00		Ŧ
U Errors, 1 Warning											28		



Component Library	Project S	Project Settings Instance Parameters				nspect	or	HD	HDL Example Generation Clock Settings Cl B End IRQ Opcoc clk. B End IRQ Opcoc clk. IRQ 0 IR IRQ IRQ clk. IRQ 0 IR IRQ IRQ clk] IRQ 0 IRQ IRQ IRQ			eneration
		System C	ontents		Address M	ар				Clock S	Settings	
Contig-Bypass App Example	🕈 Use	Connect	ions	Name		D	E	Cl	В	End	IRQ	Орсос
				clk_res ⊡ nios2_q	et sys	Re Nio	Doub					*
Configuration & Programming Configuration & Programming Configuration & Programming Configuration Controllers Controllers				clk reset_r data_m instruct jtag_de	n aster tion_master bug_module_re	Clo Re Av Av . Re	Doub Doub Doub Doub Doub	CIK [Clk] [Clk] [Clk] [Clk]	IRQ C) IR		
Memories and memory controllers Merlin Components Microcontroller Peripherals	7	•	★ → ×→	jtag_de custom	bug_module _instruction_m t	Av Cu	Doub Doub	[clk]	•	.0x		Ξ
Peripherals Debug and Performance Display Microcontroller Peripherals		+ +	$\xrightarrow{\bullet}$	clk reset avalon	_itag_slave	Clo Re Av	Doub Doub Doub	cik [cik] [cik]	÷ .	.0x) 0	
Interval Timer PIO (Parallel I/O) Vectored Interrupt Controller ▼		+ + +	$\stackrel{\bullet}{\bullet} \xrightarrow{}$	clk1 s1 reset1	010	Clo Av Re	Doub Doub Doub	clk [clk1] [clk1]	e .	.0x		
New Edit	•			clk	ii	Clo	Doub	clk				
Messages												
Description				Pat	h							
🗆 🕕 2 Info Messages												^
O System ID is not assigned automatically. Edit the state of the st	System ID par	ameter to p	orovide a uniq	ue ID Syst	em.sysid_qsys						00	-
U Errors, U Warnings											29	

					E C
Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop)	op\Project\DE	2_115_QSYS.qsys)			
File Edit System View Tools Help					
Component Library	System Co	ontents	Address Map	Clock Se	ettings
Proj	ject Settings	Instance Parameters	System Inspecto	or HDL Example	Generation
Contig-Bypass App Example	imulati 🚣 Ge	enerate Completed			×
	e simula U Ir eate sim 0 Ir 0 Ir	nfo: rsp_xbar_demux: "I nfo: rsp_xbar_demux_0 nfo: rsp_xbar_mux: "DE2	DE2_115_QSYS" instantia D2: "DE2_115_QSYS" ins 2_115_QSYS" instantiated	ated altera_merlin_dem tantiated altera_merlin_d d altera_merlin_multiple	ultiplexer "rsp_: _ demultiplexer "ı exer "rsp_xbar_
Save changes?	stben 🕕 Ir	nfo: Reusing file C:/Users	/Trumen/Desktop/Proj "DE2_115_QSYS" instan	ject/DE2_115_QSYS/synt	thesis/submodu Iltiplexer "rsp_x
Save changes to DE2_115_QSYS.qsys?	testbe a gene te tes 1 In 1	fo: Reusing file C:/Users	/Trumen/Desktop/Proj 15_QSYS" instantiated al DE2_115_QSYS" with 2	ject/DE2_115_QSYS/synt Itera_irq_mapper "irq_n 25 modules, 73 files, 25952	thesis/submodu napper" 201 bytes
		nto: ip-generate succeede	a. design files for synth	nesis	-
Microcontroller Peripherals Interval Timer Syr	nthesis	enerate Completed. 0 Erro	rs, 47 Warnings		, , , , , , , , , , , , , , , , , , ,
PIO (Parallel VO) ····· ● Vectored Interrupt Controller ····PLL ····	eate HDI			s	Stop 4 Close
New Edit Edit Ger	nerate 2				
Messages	Gener	ate the system			
Description		Pa	th		
⊇ 🕕 2 Info Messages					^
System ID is not assigned automatically. Edit the System ID 0 Errors, 0 Warnings	D parameter to p	rovide a unique ID Sys	tem.sysid_qsys	3	÷



🛯 💱 Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII							
File Edit View Project Assignments Processing Tools Window Help 🐬 Search altera.com							
🕴 🗋 💕 🛃 🍠 🕺 🛍 🛍 🧉 🥲 [NiosII 🕞 😿 😪 🖉 🤡 🖄 🖄 🖄 🖏 😓 👘							
Project Navigator							
	1						
All Carlos Contraction of the second							
Type ID Message	32						
Ln 13 Col 10 Verilog HDL File	0% 00:00:00						

```
module NiosII (
    clk,
    rst_n,
    led,
);
input clk, rst_n;
output [7:0] led;
DE2_115_QSYS DE2_115_QSYS_inst (
    .clk_clk(clk),
    .reset_reset_n(rst_n),
    .led_export(led),
);
endmodule
```





🥜 Settings - NiosII

Category:			Device		
General	Files				
Files					
Libraries	Select the design files you want to include in the project. Click Add All to add all design files in the project				
Operating Settings and Conditions	directory to the project.				
Voltage			4		
Temperature	File name:		Add		
 Compilation Process Settings 					
Early Timing Estimate Select File			×		
Incremental Compilati					
Physical Synthesis Op	🌗 🕨 Project 🕨	•	∮ 搜尋 Project		
EDA Tool Settings					
Design Entry/Synthes 組合管理	▼ 新増資料夾		i = 🗸 🦷 🔞		
Simulation Formal Verification					
Board-Level	2.55 C	名稱	修改日期		
Analysis & Synthesis Setti					
VHDL Input	рьох	🥼 .qsys_edit	2014/2/15 上午 植		
Verilog HDL Input 🛛 🗼 下重	\$	📗 🕛 db	2014/2/15 上午 楷		
Default Parameters 🔤 🖨 🖬	T =	DE2 115 OSVS	2014/2/15 上午 - 樽		
Fitter Settings					
TimeQuest Timing Analyze 🛛 🔛 市辺	1的位置	DE2_115_QSYS.cmp	2014/2/15 <u>_</u> + C		
Assembler		DE2_115_QSYS.qsys	2 2014/2/15 上午 Q		
Design Assistant	a a a a a a a a a a a a a a a a a a a		, 		
SignalTap II Logic Analyze	8				
Logic Analyzer Interface 文作	F				
SSN Apalyzer	ŧ				
1774	`				
	i -	•	•		
	檔案名稱(N):	DE2_115_QSYS.qsys	Design Files (*.tdf *.vhd *.vhdl *.v 👻		
		3	開啟舊檔(O) 取消		

- -

35

Help

Apply

х

OK

Cancel

🥜 Settings - NiosII

Category:		Device		
General Files Libraries	Files Select the design files you want to include in the project. Click Add All to ad	d all design files in the project		
 Operating Settings and Conditions Voltage 	directory to the project.			
Compilation Process Settings	The figure. DE2_113_Q313.d\$95			
Early Timing Estimate Select File Incremental Compilati				
Physical Synthesis Op	🕌 « DE2_115_QSYS 🖡 synthesis 🖡 🔷 🗸 🐙 授霉 :	synthesis 🔎		
Design Entry/Synthes 組合管理	▼ 新増資料夾	iii 🕶 🔟 🔞		
Formal Verification Board-Level	▲ 名稱 ▲	修改日期		
 Analysis & Synthesis Setti VHDL Input 	pbox	2014/2/15 上午 0 3		
Verilog HDL Input 🔒 下통	t DE2_115_QSYS.v 3	2014/2/15 上午 0		
Fitter Settings	4 f的位置			
Assembler				
Design Assistant SignalTap II Logic Analyze 篇 媒體	Ē			
Logic Analyzer Interface 章 文作 PowerPlay Power Analyze	F			
SSN Analyzer 🚽 首等				
	横安名搿(N): DE2 115 OSVS v → Design Fil	es (* tdf * vbd * vbdl * v -		
		窗(O) 取消		
		36		
	OK Cancel	Apply Help		
🏒 Settings - NiosII

Cate	:gory:		
	General	Files	
	Files		
4	Libraries Operating Settings and Conditions	Select the directory to	design files you want to include in the project. Clic the project.
	Voltage Temperature	File name:	DE2_115_QSYS/synthesis/DE2_115_QSYS.v

A Compilation Process Settings Early Timing Estimate Incremental Compilation Physical Synthesis Optimizations

EDA Tool Settings Design Entry/Synthesis Simulation Formal Verification Board-Level Analysis & Synthesis Settings VHDL Input Verilog HDL Input Default Parameters Fitter Settings TimeQuest Timing Analyzer Assembler Design Assistant SignalTap II Logic Analyzer Logic Analyzer Interface PowerPlay Power Analyzer Settings

SSN Analyzer

k Add All to add all design files in the project

.... Add File Name Type Library Design Entry/Synthesis Tool Add All DE2_115_QSYS.qsys Qsys System File <None> Remove Up Down Properties .€ 111 Þ

Device...

X

- -

2

OK

Cancel

Apply

Help

Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII		×
File Edit View Project Assignments Processing Tools Window Help Search	n altera.com	•
🕴 🗋 💕 🗔 🥥 X 🗈 🛍 🔊 (*) [NiosII 🔹 🐨 🔀 😵 🔇 💷 🕨 🦻 (🖄 🕲 😫 🗞	»
Project Navigator 🕂 🗗 🗙 🐠 Verilog 1. v* 🖂 🚸 DE2_115_QSYS/synthesis/DE2_115_QSYS.v 🔀		
📔 🗁 Files 🛛 🔄 🖼 🖓 🖓 🛱 👫 💏 👘 🖆 🔞 🚱 🔞 🖉 🕲 😵	² ₈ ab/ │ 📩 📃	»
DE2_115_QSYS/synthesis/DE2_115_QSYS.v 1 // DE2_115_QSYS.v		-
3 // Generated using ACDS version 13.0sp1	. 232 at 2014	
4 5 `timescale 1 ps / 1 ps		
→ Hierarchy Files Design Units ↓ 6 Emodule DE2_115_QSYS (
Tasks 7 input wire clk_clk, Imput wire reset reset n,	<pre>// clk.clk // reset.res</pre>	e l
Flow: Compilation Customize 9 output wire [7:0] led_export	// led.exp	0
Task 12 wire nios2_gsys_instruction_ 4 Comple Design 13 wire [19:0] nios2_gsys_instruction_	master_waitr	e
Image: Second contraction Image: Second contraction Image: Second contraction Image: Second contraction	master read.	
* Type ID Message		
a dess		•
System / Processing /	38	
	0% 00:00:0	



🚱 Quartus II 64-Bit - C:/Users/Trumen/D	Deskt <mark>o</mark> p/Project/NiosII - NiosII							
File Edit View Project Assignments	Processing Tools Window H	elp 💎	_	Sea	rch altera.com 🔇			
i 🗋 💕 🖬 🥔 🐰 🖬 🛍 🔊 💌	Stop Processing	Ctrl+Shift+C	4	V 🚸 💷 🕨 😼 🚺	🛈 🛃 🦿 🧼 🔹			
i 💷 🕨 🖄 🗞 🧇 🤣 📸 📸 🆓 🎙	💿 🕨 🧏 🏷 🤣 📸 🎬 🆓 🖡 🔉 Start Compilation 🛛 Ctrl+L							
roject Navigator 🤡 Analyze Current File				SYS/synthesis/DE2_115_QSYS.v				
🗁 Files	Start 2	•		Start Hierarchy Elaboration	-			
DE2_115_QSYS/synthesis/DE2_115_Q	Update Memory Initialization F	File	►	Start Analysis & Elaboration	3			
DE2_115_QSYS.qsys	Compilation Report	Ctrl+R	1	Start Analysis & Synthesis	Ctrl+K			
NiosII.v	Dynamic Synthesis Report		16	Start Partition Merge				
	PowerPlay Power Analyzer To	ol	۱.	Start Fitter				
A Hierarchy	SSN Analyzer Tool		4	Start Assembler				
Tasks	₽ ₽ × 8 ⊟DE2_1	15_QSYS DE2_1	0	Start TimeQuest Timing Analyzer	r Ctrl+Shift+T			
Flow: Compilation	ustomize 10	clk_clk(clk),	M.	Start EDA Netlist Writer				
Tark	10 11	led_export(le		Start Design Assistant				
	12 L);	dula	37	Start PowerPlay Power Analyzer	Ctrl+Shift+P			
Comple Design	- T3 Elidino	dute		Start SSN Analyzer				
			2	Start SignalProbe Compilation	Ctrl+Shift+S			
🗕 🔁 🙆 🙆 🦽 🤝 💎 < <sea< td=""><td>arch>></td><td>~</td><td>≥io</td><td>Start I/O Assignment Analysis</td><td></td></sea<>	arch>>	~	≥io	Start I/O Assignment Analysis				
7 Type ID Message			≧ ô	Start Early Timing Estimate				
			V	Start Check & Save All Netlist Ch	nanges			
				Start VQM Writer				
				Start Equation Writer (Post-synt	thesis)			
				Start Equation Writer (Post-fittin	ng)			
8				Start Test Bench Template Write	er			
sz v				Start EDA Synthesis				
System / Processing /				Start EDA Physical Synthesis	40			
Analyzes and elaborates all files in the hierarchy	y of the current top-level entity	L	_		0% 00:00:00			











File	Edit View Pro	ject Proce	essing Tools W	indow Help 🐬			Search	altera.com	
	New File Close	Ctrl+N	🖸 孢 💽 🕅 eriod 20 [g	et_ports clk	67 ab/ 🔜 []				
	Save Save As	Ctrl+s	certainty 0 -clock c y 0 -clock	lk [all_inpu clk [all out	ts] puts]				
	Create / Update	•		_					
	Page Setup			另存新檔					×
	Print Preview Print	Ctrl+P		儲存於(I):	\mu Project		• + (i 💣 🎟	
			·	Ca.	名稱	*		修改日期	
				最近的位置	📗 .qsys_edit			2014/2/15	上午 03:01
			- L		📗 db			2014/2/15	上午 08:00
					BE2_115_Q	2SYS		2014/2/15	上午 05:51
				兵回 【二】 媒體櫃	incrementa output_files	s		2014/2/15	上午 06:28 上午 07:55
				MANU ALE					
				(1)	•				4
					檔案名稱(N)·	NiosII ste	3	-	存檔(S)
					存檔類型(T):	Symonsys Design (Constraints Files (* sdc)	L	取消
					I INVALE (*)			- 46	

🚱 Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII								
File Edit View Project Assignments Processing Tools Window Help Sea	rch altera.com 🔇							
🔋 🗋 💕 🗔 🥥 X 🗈 🛍 🕫 🤍 İNiosII 🔷 📝 😵 🐼 💿 🕨	🖄 🛈 🛃 😤 🛛 »							
📔 💷 🕨 🖄 🗞 🗞 🖉 📸 🕍 🥙 🖄 🖓 🖗 😽 🖄 🖄 🖄 🖓 🖗 😽 😒	ompilation							
Project Navigator 🕂 🗗 🗙 😔 Compilation Report - NiosII 🛛								
Image: Second structure Image: Second structure </th <th>Flow Summary Flow Status Quartus II 64-Bit Ver: Revision Name Top-level Entity Name Family Device Timing Models Total logic elements Total combination Dedicated logic re Total registers Total virtual pins Total memory bits Embedded Multiplier S</th>	Flow Summary Flow Status Quartus II 64-Bit Ver: Revision Name Top-level Entity Name Family Device Timing Models Total logic elements Total combination Dedicated logic re Total registers Total virtual pins Total memory bits Embedded Multiplier S							
	All 😢 🖾 🔏 🤝 < <search>> V</search>							
Type ID Message 12020 Port "jdo" on the entity instantiation of "the_DE2_115_QSYS_nios2_gsys_nios2_oci_i 12241 2 hierarchies have connectivity warnings - see the Connectivity Checks report fold 144001 Generated suppressed messages file C:/Users/Trumen/Desktop/Project/output_files/Ni Quartus II 64-Bit Analysis & Elaboration was successful. 0 errors, 55 warnings								
System Processing (413) Starts a new compilation	47 100% 00:00:44							



Edit View Pro	cessing Loois Window	Help 4/			Search alter	ra.com	
Hardware Setup	USB-Blaster [USB-0]	Mode: JTAC	3	▼ Progr	ess:		
Enable real-time ISP	to allow background progra	mming (for MAX II and	d MAX V devices)				
Mu Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check
June Stop	output_files/NiosII.sof	EP4CE115F29	008600F4	008600F4			
\mu Auto Detect							
💢 Delete							
🍐 Add File							
Ghange File							
Save File	•						4
							Â
A							
							=
↓ [™] Down							
	EP4CE115	-29					
	TDO						
							-

🔔 Hardware Setup	USB-Blaster [USB-0]	Mode: JTAC	3	▼ Progr	ess: 100%	% (Success	ful)
Enable real-time I	SP to allow background progra	amming (for MAX II and	d MAX V devices)				
Mu Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check
Ju Stop	output_files/NiosII.sof	EP4CE115F29	008600F4	008600F4	V		
X Delete	When co configure	onfiguratior ed with the	n is comp Nios II s	olete, the system, l	e FPGA out it do	is bes no	ot
Change File Save File	When co configure yet have	onfiguratior ed with the a C progra	n is comp Nios II s am in me	olete, the system, l emory to	e FPGA out it do execut	is bes no e.	ot •
Change File Add File Change File Add Device Add Device Dup Dup Down	When co configure yet have	onfiguration ed with the a C progra	n is comp Nios II s am in me	olete, the system, l emory to	e FPGA out it do execut	is bes no e.	ot •

NIOS II IDE Build Flow

This Chapter covers build flow of Nios II C coded software program.



Introduction

- The Nios II IDE build flow is an easy-to-use graphical user interface (GUI) that automates build and makefile management.
- In this section you will use the Nios II IDE to compile a simple C language example software program to run on the Nios II standard system configured onto the FPGA on your development board.





	lios II - Eclipse				
File	Edit Navigate Search Run Project	Nios II	Window Help		_
	New 2 Alt+Shift-	•N 🕨 💽	Nios II Application and BSP from Templa	ate 3	🕶 📑 💽 Nios I
	Open File	6	Y Nios II Application		E C/C++
	Close Ctrl+	w	Nios II Board Support Package		Home X -
	Close All Ctrl+Shift+	w 🖸	🕅 Nios II Library		
-	o		Project		
	Save Ctri	ີ 🛃) Other	Ctrl+N	Overview
	Save All Ctrl+Shift				Get an overview of the
الما	Revert				features
-0	Move				Tutoriala
	Rename				Go through tutorials
~	Convert Line Delimiters To	` .			
		_			
÷	Print Ctrl	+P			Samples E
	Switch Workspace	->			Try out the samples
	Restart				
2	Import				What's New
4	Export		🕅 🖉 Tasks) 🗉 Consol) 🔲 Propert		Find out what is new
	Properties Alt+En	er			
				Pasouro	
	Exit			resource -	Workbench
					Go to the workbench
					54
	0 items selected				

Nios II Application and BSP from Template	
Nios II Software Examples Create a new application and board support package based on a software example template	
Target hardware information SOPC Information File name: C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.sopcinfo CPU name: nios2_qsys	
Application project Project name: Hello_NiosII Use default location Project location: C:\Users\Trumen\Desktop\Project\software\Hello_NiosII Project template	
Templates Template description Blank Project Image: Count Binary Hello Freestanding Image: Count Binary Hello MicroC/OS-II Image: Count Binary Hello World Image: Count Binary Hello MicroC/OS-II Image: Count Binary Hello World Image: Count Binary Hello World Image: Count Binary Hello World Image: Count Binary Hello MicroC/OS-II Image: Count Binary Hello World Image: Count Binary	
Sack Next > Finish Cancel	55

Nios II Application and B	SP from Template	
Nios II Software Examples Select a board support par	s ckage for your application	
Oreate a new BSP proje	ct based on the application project template	
Project name: Hello_	NiosII_bsp	
Use default location	1	
Project location:	C:\Users\Trumen\Desktop\Project\software\Hello_Nios	I_bsp
Select an existing BSP p	roject from your workspace	E
		Create
		Import
2	< Back Next > Finis	h Cancel



Project Description

- When you create a new project, the NIOS II SBT for Eclipse creates two new projects in the NIOS II C/C++ Projects tab:
 - Hello_NiosII is your C/C++ application project. This project contains the source and header files for your application.
 - Hello_NiosII_bsp is a board support package that encapsulates the details of the Nios II system hardware.













Edit and Re-Run the Program

File Edit Source Refactor Navigate Search Run Project Nios II Window Help
$ \begin{array}{c} \hline & \bullet \\ \hline \hline & \bullet \\ \hline & \bullet \\ \hline \hline \hline \hline \hline & \bullet \\ \hline
Project Explorer 🛛 🖓 🖓 🖓 🖓 🖓 🖓 🖓 🖓
<pre>#include <stdio.h> #include <stdio.h> #include "system.h" #include "system.h" #include "altera_avalon_pio_regs.h" #includes obj int main() { printf("Hello from Nios II!\n"); int count = 0; int delay; while(1) { reate-this-app Hello_NiosILobjdump Hello_NiosILobjdump Makefile readme.txt #includes count = (count+1) % 8; // Gelay < 2000000) { return 0; // ellay = 115_QSYS // ellay = 0; // ellay = 0; // ellay < 2000000) {</stdio.h></stdio.h></pre>

```
#include <stdio.h>
#include "system.h"
#include "altera_avalon_pio_regs.h"
int main()
  printf("Hello from Nios II!\n");
  int count = 0;
  int delay;
  while(1) {
    IOWR_ALTERA_AVALON_PIO_DATA(LED_BASE, 1 << count);</pre>
    delay = 0;
    while(delay < 2000000 ) {</pre>
      delay++;
    }
    count = (count+1) \% 8;
  return ∅;
```

0

😂 Nios II - Hello_Nic	12-12-	New	۰.	
File Edit Source		Go Into		Help
		Open in New Window		• 😂 😂 🛷 • 🎿 🧼 📑 🔯 Nios I
	D	Сору	Ctrl+C	比应 C/C++
Project Explorer	Ē	Paste	Ctrl+V	
	×	Delete	Delete	A
🔺 😂 Hello_NiosII	<u>s</u>	Remove from Context	Ctrl+Alt+Shift+Down	rs.h"
⊳ 🐝 Binaries . ⊳ 🔊 Includes	(righ	Source t-click) Move	•	
⊳ 🔁 obj ⊳ 🕼 hello woi		Rename	F2	");
⊳ 🐝 Hello_Nic	2	Import		
create-th	4	Export		(LED_BASE, 1 << count);
		Build Project		
🚡 Makefile		Clean Project		
📄 readme.t	8	Refresh	F5	
🛛 🖌 😂 Hello_NiosII_		Close Project		
▷ m Includes		Close Unrelated Projects		
Arivers		Build Configurations	•	
⊳ 💽 alt_sys_ini		Make Targets	•	F
⊳ 🔥 linker.h		Index	•	Properties 🛗 Nios II Console 🛛 🛛 🔳 🕞 😭 🌄 🖓 🗖 🗖
⊳ .h system.h				: USB-Blaster on localhost [USB-0] device ID: 1 instance ID: 0 name: jtagua
📄 create-th		Show in Remote Systems view		
linker.x		Convert To		
		Run As 2	+	4 1 Lauterbach ISS
memory e		Debug As	•	C 2 Local C/C++ Application
bublic.ml		Profile As	•	🕅 3 Nios II Hardware 3
< III		Team	+	4 Nios II ModelSim 65
📑 🗘 🔁 Hell		Compare With	+	Run Configurations
		Restore from Local History		



Why the LEDs Blink? (1/2)

- The Nios II system description header file, system.h, contains the software definitions, name, locations, base addresses, and settings for all of the components in the Nios II hardware system.
- The system.h file is located in the in the Hello_NiosII_bsp directory.





Why the LED Blinks? (2/2)

- The Nios II processor controls the PIO ports (and thereby the LED) by reading and writing to the register map.
- For the PIO, there are four registers: data, direction, interrupt mask, and edge capture.
- To turn the LED on and off, the application writes to the PIO data register.



Register Map File (1/2)

- The PIO core has an associated software file altera_avalon_pio_regs.h.
 - This file defines the core's register map, providing symbolic constants to access the low-level hardware.
 - This file is located in Project\software\Hello_NiosII_bsp\drivers\inc \.



Register Map File (2/2)

- When you include this file, several useful functions that manipulate the PIO core registers are available to your program.
- In particular, the function IOWR_ALTERA_AVALON_PIO_DATA (base, data) can write to the PIO data register, turning the LED on and off.
- The PIO is just one of many SOPC peripherals that you can use in a system.



Debugging the Application

 Before you can debug a project in the NIOS II SBT for Eclipse, you need to create a debug configuration that specifies how to run the software.




😂 Nios II - Hello_Nio		New			•		- 0 X
File Edit Source		Go Into				Help	
		Open in New Window			ł	2 2 4 - 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	Nios I
	D	Сору		Ctrl+C	L		.++
Project Explorer	Ē	Paste		Ctrl+V			
	×	Delete		Delete			*
🔺 📂 Hello_NiosI	٩.	Remove from Context	C	trl+Alt+Shift+Down	5	.h"	
▷ ﷺ Binaries → ▷ 圖 Includes	(right	Source click)		I	·		
⊳ 🕞 obj		Move	Const.	Description Control	-		×
⊳ 📝 hello_wor		Rename	Contil	rm Perspective Switch	ו		
⊳ 🕸 Hello_Nic	2	Import		This kind of launch is	con	figured to open the Nios II Debug perspectiv	ve when it
📄 create-thi 📄 Hello Nic	4	Export		suspends.		5 1 51 1	
Hello_Nic		Build Project		This perspective is de	sigr	ned to support efficient development of a Ni	ios II
🚡 Makefile		Clean Project		project. It turns off a	utor	matic build and adds the Nios II Console view	v which is
📄 readme.t	8	Refresh		particularly useful.			
⊿ 😤 Hello_NiosII_		Close Project		Do you want to oper	1 this	s perspective now?	
 Includes Control des Control des 		Close Unrelated Projects				4	
Þ 📂 HAL		Build Configurations	Rem	ember my decision		4	+
⊳ 💽 alt_sys_ini		Make Targets				Yes	No
⊳ <u>h</u> linker.h		Index					
⊳ in system.n		Show in Remote System	sview		-	USB-Blaster on localhost [USB-0] device ID: 1 instan	ce ID: 0 name: jtagua
linker.x		Convert To					
🚡 Makefile		Run As		,			
🚡 mem_init.	_	Debug As 2				1 Local C/C++ Application	
memory.c		Profile As				2 Nios II Hardware	
j joblic.mk		Team					74
÷ =+>		Compare With		1	Ļ	Debug Configurations]
		Restore from Local Histo	ry			1	

Nios II Debug - Hello_NiosII/hello_world.c - Eclipse	1							
File Edit Source Refactor Navigate Search	Run	Project I	Nios II	Window	Help	_		
		Resume Suspend	2		F8	•		🖹 🏇 Nios II Debug 👋
🕸 Debug ⊠		Terminate			Ctrl+E2	Breakpoints	1111 Register	rs 📋 Memory 📃 🗖
D. 45 14 🔳 111 📲 🗱	.	Step Into			F5		約 📲 🖻	🗳 🗶 💥 🔂 🗹 🎽
ntread [1] (Suspended: Breakpoint hit	2	Step Over			F6		Value	
3 main() hello_world.c:7 0x0004021	-× &	Step Return			F7		-55903873	37
2 alt_main() alt_main.c:154 0x00043		Dura ta Lina	•		Chillip		-55903873	37
= 1_start() crt0.S:437 0x000401fc	-1	Kun to Line			Ctri+K			
<pre>terminated, exit value: 0>nios2-downloa;</pre>	З¢,	Use Step Fil	ters					<u>^</u>
✓ III	Q,	Run			Ctrl+F11			- F
i hello_world.c ⋈	*	Debug			F11		E Outline	8 -0
<pre>#include <stdio.h></stdio.h></pre>		Run History			•	•	1	🛯 🖞 😼 🖋 💿 🗰 🏹
#include "system.h" #include "altera avalon nio regs h"		Run As			•		1 s	tdio.h
#include artera_avaion_pro_regs.in		Run Confia	uration	5			🖬 s	ystem.h
int main()						= -	💾 a	Itera_avalon_pio_regs.h
<pre>i printf("Hello from Nios II!\n"):</pre>		Debug Hist	ory		•		• n	nain() : int
int count = 0;		Debug As			•			
int delay;		Debug Con	figurat	ions				
While(1) { TOWR ALTERA AVALON PTO DATA(LED BAS)	0	External To	ole					
delay = 0;	-	External TO						
						*		
📮 Console 🖉 Tasks 💏 Nios II Console 🛛						,	L	
Hello_NiosII Nios II Hardware configuration - cable: USB-Blaster	r on I	ocalhost [USB-	-0] devid	e ID: 1 insta	nce ID: 0 name	: jtaguart_0		
								75
						1		

Debugging Tips

 When debugging a project in the Nios II SBT for Eclipse, you can pause, stop or single step the program, set breakpoints, examine variables, and perform many other common debugging tasks.





Configure BSP Editor

- In this section you will learn how to configure some advanced options about the target memory or other things.
- By performing the following steps, you can charge all the available settings.



Nios II - Hello Nios II/bello world c - Ec				_ 0 _ X
File Edit Course Defector Neviceta		Сору	Ctrl+C	
File Edit Source Refactor Navigate	Ê.	Paste	Ctrl+V	
	×	Delete	Delete	🌙 😜 🛛 🖹 💽 Nios II 🛛 👋
🎦 Project Explorer 🕱 🗧 🗖	S.	Remove from Context	Ctrl+Alt+Shift+Down	
		Source	•	A
⊳ 😤 Hello_NiosI	(right-	Move		
🔺 😂 Hello_NiosII_bsp [DE2_115_QSVS]	(g	Rename	F2	
⊳ 🔊 Includes	pkg.	Import		
drivers	~~~	Export		
⊳ 🔁 HAL		Export		
▷ <u>c</u> alt_sys_init.c		Build Project		
b linker.h		Clean Project		punt);
⊳ in system.n	8	Refresh		
		Close Project		
Makefile		Close Unrelated Projects		
int.mk		Build Configurations	+	
memory.gab		Make Targets	•	
settings.bsp		Index	•	
i summary.html		Show in Remote Systems view		-
		Convert To		
		Run As	•	Console 🛛 🕸 Debug 🛛 🗖
		Debug As	•	
		Profile As	•	t [USB-0] device ID: 1 instance ID: 0 name: jtagua
		Team	+	
		Compare With	•	
		Restore from Local History		
		Nios II 2	•	Nios II Command Shello.
	*	Run C/C++ Code Analysis		Generate BSP
📑 🗘 😤 Hello_NiosII_bsp		Properties	Alt+Enter	BSP Editor 3
		riopenies	AITENIE	

🚖 Nios II BSP Editor - settings.bsp	
File Edit Tools Help	
Main Software Packages Drivers Linker Script Enable File Generation Target BSP Directory	
SOPC Information file: C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.sopcinfo CPU name: nios2_qsys Operating system: Altera HAL Version: default BSP target directory: C:\Users\Trumen\Desktop\Project\software\Hello_NiosII_bsp	
Settings Settings Image: Se	E
Information Problems Processing Setting "hal.linker.exception_stack_memory_region_name" set to "onchip_memory2".	
Loading drivers from ensemble report.	
(1) Mapped module: "nios2_gsys" to use the default driver version.	
Mapped module: "led" to use the default driver version.	
Manned module: "itaq uart" to use the default driver version.	
I Finished loading drivers from ensemble report.	-
80 Generate	Exit

÷I	Nios II BSP Editor - sett	tings.bsp						
File	Edit Tools Help							
Mai	in Software Packages D	Drivers Linker Scr	ipt Enable File G	eneration Target BSP Dire	ectory			
Lin	ker Section Mappings	·						
	A Name		Linker Region Na		Memory Device Name			Add
			linker Region va		Inemotive Device Name		F	Remove
.0	ss ntrv		reset		onchip_memory2		Destr	ore Defaults
	vcentions		onchin memory2		onchip_memory2		Kesu	De Delauits
h	ean		onchin memory2		onchin_memory2			
r r	odp odata		onchin_memory2		onchin_memory2			
. r	wdata		onchip memory2		onchip memory2			
.s	tack		onchip memory2		onchip memory2			
. t	ext		onchip_memory2		onchip_memory2			
Lin	ker Memory Regions							
Lir	nker Region Name	Address Range	*	Memory Device Name	Size (bytes)	Offset (bytes)		Add
ວກ	chip_memory2	0x00040020	- 0x00071FFF	onchip_memory2	204768	3 .	32 F	lemove
re	set	0x00040000	- 0x0004001F	onchip_memory2	32	2	0 Resto	ore Defaults
							Add Me	emory Device
							Remove	Memory Device
							Mem	nory Usage
							Me	mory Map
-								
Gra	ayed out entries are auto	omatically creat	ed at generate ti	me. They are not editabl	ie or persisted in the B	SP settings file.		
Inf	ormation Problems Proc	ressing						
	Setting "hal linker exception	on stack memory	region name" se	t to "onchin memory?"				
	Loading drivers from ense	mble report	_region_name_se	to onenp_memory2.				<u>^</u>
	Mapped modules "pige?, or	nuce the de	foult driver version	_				
	Manned module: "Ied" to use the default driver version.							
	Mapped module: "sysid os	sys" to use the de	fault driver version	1.				
	Mapped module: "itag uar	rt" to use the defi	ault driver version					01 1 -
							<u> </u>	
							Generate	Exit

Note

- If you make changes to the system properties or the Qsys properties or your hardware, you must rebuild your project
- To rebuild, right-click the Hello_NiosII_BSP->Nios II->Generate BSP and then Rebuild Hello_NiosII Project.



Programming the CFI Flash

Introduction

- With the density of FPGAs increasing, the need for larger configuration storage is also increasing.
- If your system contains a common flash interface (CFI) flash memory, you can use your system for FPGA configuration storage as well.





👃 Open System - Qsys								23
File Edit System View Tools Help								
Component Library	Project S	ettings	Instance Parame	eters	System Inspector	HDL Example	Gener	ation
		System C	ontents		Address Map	Clock S	ettings	
Project d	🕂 Use	Conn Na	ame	Descripti	on	Export		Clock
Project New Component 人 開啟			100.0	(Income lines				
i System	☆表: □□ (Project						
Config-Bypass Ap	A.G. ·	Tojoor				ick to	export	clk_0
Bridges Bridges). 📗	qsys_edit				ick to	export	
		0 F2 115 OS	YS					
● Configuration & Progra	ジリリロ 🦉 🖡 ir	cremental_c	db					
	- 🔒 o	utput_files						
Interface Protocols	■) s ≠	oftware						
	щ <u> </u>	F2 115 OS	YS asys					
E Peripherais								
-Qsys Interconnect	×1+							
	₩ R£							
Rever	02							
	▲ 檔案名	5稱: DE	2 115 QSYS.qsys		2	開設(0)		- F
Messages #	● 路 探索型	5开U: [A	Custom Files (t. saus)	• \		TICK		
Description			ty System Files (".qsys,"	sopc)	· · · · ·			
Description		-						
							86	
0 Errors, 0 Warnings								

& Qsys - DE2_115_QSYS.qsys (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)

File Edit System View Tools Help

Component Library		Project S	Settings	Instan	ce Parame	ters	Syster	HDL Example		Generation	1	
			System Co	ontents			Address	Мар	Cloc	k Settin	gs	
×	+	Use	Connectio	ns	Name			Description			Export	٦
Embedded Processors	X					0		Clock Source				
Interface Protocols						io.		Clock Source				
Memories and Memory Controllers	1.00			~ ~ ~	CIK_	in report		Clock input		0	ik	
Merlin Components	X.			<u> </u>	CIK_	in_reset		Clock Output		'	esel	
Microcontroller Peripherals					CIK	ranat		Clock Output			Double	
⊕ Peripherals						deve		Nice II Processo			Double	
I ±···PLL						c_qsys		Clock Input	1			
⊡Qsys Interconnect	X.				CIK			Clock Input			Double	
⊕ AHB	· _			- T	dete	si_n		Avalan Mamany	Mananad Mantar		Double	=
+ AXI Interface	1 1				inot	_master	otor	Avaion Memory	Mapped Master		Double	-
				\square	itea	debug m	ster adula ra	Avaion memory	mapped master		Double	
+Memory-Mapped					jtag	_debug_ma	odule_re	Avelog Momory	Mannad Clave		Double	
- Tri-State Components				T L	jtag	_debug_mo	otion m	Avaion memory	mapped Slave		Double	
Conduit Pin Divider (double-click)					L itaa	uart	cuon_m	ITAC HART	IOTI Master		Double	
Generic Tri-State Controller						uart		Clock Input				
 Tri-State Conduit Bridge 					CIK			Clock input			Double	
Tri-State Conduit Bridge Transk					rest	si Inn itan al		Avelop Momony	Mananad Clave		Doubh	-
Tri-State Conduit Pin Sharer				Y /	ava	ion_lag_si	ave m/2	Avaion memory	(DAM or DOM)		Double	
						ip_memo	nyz	Clock locut	y (RAM OF ROM)			
Window Bridge ▼					CIKI of			Clock input	Managed Clave		Double	
4 III >					S1			Avaion memory	mapped Slave		Double	
				TT	rese			Reset input	havel		Double	
New Edit Edit					🗆 sysic	ı_qsys		System ID Perip	neral			-
				1	1						P	
	,											
Messages												
Description						Path						
∃ 🕕 2 Info Messages												
Osystem ID is not assigned automatically. Edit the	Syste	m ID par	ameter to p	rovide a unic	ue ID	System.s	sysid_qsy	s		87		-
0 Errors 0 Warnings												

🚣 Generic Tri-State Controller - generic_tristate_controller_0



x

🚣 Generic Tri-State Controller - generic_tristate_controller_0



X

and Tri Chata Controllar, and site triatety controllar O 1 0

Seneric In-state controller - generic	_tristate_controller_0	
Generic Tri-State Co altera_generic_tristate_controller	ontroller	Documentation
 Block Diagram Show signals generic_tristate_controller_0 clk clock tristate_conduit tcm reset reset uas avalon altera_generic_tristate_controller 	 address waitrequest writebyteenable outputenable resetrequest irq reset output Parameters Is memory device Module Assignments Parameter 	 Project AMD 29LV128M Flash with Legacy SDK support CS8900 Interface (Ethernet) Cypress CY7C1380C SSRAM Flash Memory Interface (CFI) IDT71V416 SRAM ISSI IS61LPS25636A-200TQL1 SSRAM Intel 128P30 Flash Intel 128P30 Flash LAN91C111 Interface Legacy AMD 29LV065D Flash SST39VF20090 Flash
	embeddedsw.configuration.hwClassnameDriverS	Apply New Update Delete
Warning: generic_tristate_controller_0	: Properties (isFlash,isMemoryDevice,isNonVolatileStorage) have been	n set on interface uas - in composed mode these are ignored
		Cancel

- 32

🚣 Generic Tri-State Controller - generic_tristate_controller_0

-		J		
MegaCore'	Generic	Tri-State Controller		Documentation
T Block D	liagram	resetrequest		Presets
Show :	signals	reset output		Project
gen	eric_tristate_d			Library
		▼ Parameters		CS8900 Interface (Eth
reset	clock tristate reset	✓ Is memory device		Cypress CY7C1380C Flash Memory Interfac
uas	avalon	Module Assignments		IDT/1V416 SRAM ISSU 19611 P9256364.
	altera_generi	Parameter Value embeddedsw.configuration.hwClassnameDriverSupportList altera_avalon_lan91c111:altera_i embeddedsw.configuration.hwClassnameDriverSupportDefault altera_avalon_cfi_flash embeddedsw.CMacro.SETUP_VALUE 60 embeddedsw.CMacro.WAIT_VALUE 160 embeddedsw.CMacro.HOLD_VALUE 60	4	 Intel 128P30 Flash Intel 256P30 Flash LAN91C111 Interface Legacy AMD 29LV06 SST39VF20090 Flash
۰ III	•	Derematore III		Apply New
A Warning	g: generic_trista	ate_controller_0: Properties (isFlash,isMemoryDevice,isNonVolatileStorage) have been set on interface uas - in co	mpo	used mode these are ignored
				Cancel Finish

X

👃 Generic Tri-State Controller - generic_tristate_controller_0

Mogatore'	Generic	Tr i tris	-State Controller			Documentation
Block Di	iagram signals		reset output		^	Presets
clk reset	clock tristate_c		Parameters Is memory device Module Assignments		AMD 29LV128M Fla: CS8900 Interface (Et) Cypress CY7C1380C Flash Memory Interfa	
uas	avalon altera_generii		Parameter V embeddedsw.CMacro.HULD_VALUE bu embeddedsw.CMacro.TIMING_UNITS ms embeddedsw.CMacro.SIZE 83 embeddedsw.memoryInfo.MEM_INIT_DATA_WIDTH 8 embeddedsw.memoryInfo.HAS_BYTE_LANE 1 embeddedsw.memoryInfo.IS_ELASH 1	/alue v s 388608u 1	III	 IDT71V416 SRAM ISSI IS61LPS25636A- Intel 128P30 Flash Intel 256P30 Flash LAN91C111 Interface Legacy AMD 29LV06 SST39VF20090 Flash
۰ III	•		Parameters	4	Ŧ	Apply New
A Warning	: generic_trista	ate	_controller_0: Properties (isFlash,isMemoryDevice,isNonVolatileStorage) hav	e been set on interface uas - in co	ompo	osed mode these are ignored
						Cancel Finish

X

Generic Tri-State Controller - generic_tristate_controller_0	×
Generic Tri-State Controller attera_generic_tristate_controller	Documentation
Block Diagram Signal Selection Setup time: Setup tim	Presets Project Library AMD 29LV128M Flas CS8900 Interface (Eth Cypress CY7C1380C Flash Memory Interfac IDT71V416 SRAM ISSI IS61LPS25636A- Intel 128P30 Flash Intel 256P30 Flash LAN91C111 Interface Legacy AMD 29LV06 SST39VF20090 Flash SST39VF20090 Flash
→	Apply New
🖄 Warning: generic_tristate_controller_0: Properties (isFlash,isMemoryDevice,isNonVolatileStorage) have been set on interface uas - in comp	osed mode these are ignored
	93
	Cancel Finish

Generic Tri-State Controller - generic_tristate_controller_0	×
Generic Tri-State Controller altera_generic_tristate_controller	Documentation
Block Diagram Signal Selection Signal Timing Signal Polarities Show signals Enable active low polarity on the following signals: Image: Signal Polarity generic_tristate_c read 2 clk clock istate write write write Image: Signal Polarity bock bock istate Image: Signal Polarity istate 2 istate 2 istate 2 istate 3 istate 3 istate 3 istate 3 istate 3 istate istate istate 3 istate istate istate istate istate 3 istate istate istate istate <td< th=""><th>Presets Project Library AMD 29LV128M Flas CS8900 Interface (Eth Cypress CY7C1380C Flash Memory Interfac IDT71V416 SRAM ISSI IS61LPS25636A Intel 128P30 Flash Intel 256P30 Flash LAN91C111 Interface Legacy AMD 29LV06 SST39VF20090 Flash Apply New</th></td<>	Presets Project Library AMD 29LV128M Flas CS8900 Interface (Eth Cypress CY7C1380C Flash Memory Interfac IDT71V416 SRAM ISSI IS61LPS25636A Intel 128P30 Flash Intel 256P30 Flash LAN91C111 Interface Legacy AMD 29LV06 SST39VF20090 Flash Apply New
Warning: generic_tristate_controller_0: Properties (isFlash,isMemoryDevice,isNonVolatileStorage) have been set on interface uas - in comp	osed mode these are ignored
	94 4 Cancel Finish

- 0 X & Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys) File Edit System View Tools Help Component Library Project Settings Instance Parameters System Inspector HDL Example Generation System Contents Address Map Clock Settings × ÷ Use Connections Name Description Export d Processors V JTAG UART Protocols jtag uart -20 and Memory Controllers clk Clock Input mponents Reset Input reset troller Peripherals Avalon Memory Mapped Slave avalon itag slave 1 ls onchip memory2 On-Chip Memory (RAM or ROM) clk1 Clock Input \mathbf{v} rconnect s1 Avalon Memory Mapped Slave Y Reset Input reset1 1 Iterface 7 sysid gsys System ID Peripheral clk Clock Input upt ry-Mapped reset Reset Input ate Components control slave Avalon Memory Mapped Slave 1 Conduit Pin Divider PIO (Parallel I/O) Ξ led Generic Tri-State Controller clk Clock Input Tri-State Conduit Bridge Reset Input reset Dou = Tri-State Conduit Bridge Transla s1 Avalon Memory Mapped Slave Tri-State Conduit Pin Sharer external connection Conduit led \checkmark generic_tristate_controller_0 bn Connections clk Bridge reset ₹. 111 ь. V Filter uas tcm X-Add... New... Edit. -2 Ctrl+E Edit... ₹. 111 Þ 2 Ctrl+R Rename Messages Ctrl+D Duplicate × Remove Description Path Details 🗆 🔀 2 Errors ۰ System.generic generic_tristate_controller_0.clk must be connected to a clock output 95 Show Arbitration Shares Ŧ ß Suntam nanaria 2 Errors, 2 Warnings Ê. Lock Base Address

👗 Qsys - DE2_115_QSYS.qsys* (C:\U	 sers	Trumer	n\Desktop\Project\D	4	Tri-State Condui	it Pin Sharer - trist	tate_conduit_pin_share	er_0	×
File Edit System View Tools Help					🔁 🛛 Tri-S	tate Conduit	Pin Sharer		
Component Library		Project	Settings In:		egeCore altera_tri	istate_conduit_pin_s	harer	Documentatio	on
			System Contents	T					
A 10 10 10 10 10 10 10 10 10 10 10 10 10				۱I	Parameters				
Ided Processors		Use	Connections		Number of Interfac	ces: 1	2		
ice Protocols	×	V			Charing Accien				
ries and Memory Controllers			+		Sharing Assign	iment			-=
Components					To share a signal,	type the same signa	I name in the Shared Signa	I Name column	fc
erals					Update Interfac	ce Table			
orais -									
Interconnect	Ľ		• •		Interface		Signal Role	:	S
нв	. <u>▼</u> .		+ +						
KI Interface	8	V							
errupt					4		1		
emory-Mapped								,	
Conduit Pin Divider					[
@ Generic Tri-State Controller									
···· Tri-State Conduit Bridge			• - •				Ca	ncel Fini	sh <mark>3</mark> ∈
···· Tri-State Conduit Bridge Tra									
····· Tri-State Conduit Pin Sharer					external_conne	ction	Conduit	ŀ	ed
ation 1 (double-click)					cti_tlash		Generic Tri-State Contro	ller	
				3	reset		Reset Input		Dou
				→	uas		Avalon Memory Mapped	Slave	Dou
			×	-	tcm		Tristate Conduit Master		Dou.
		•	·	III	1				P.
Messages									
Description						Path			
🗆 🔀 2 Errors									
Scfi_flash.clk must be connected t	to a clo	ck outp	ut			System.cfi_flash		96	
2 Errore 2 Warninge						System of fleeb			*
2 chors, 2 warnings									

- O X & Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys) File Edit System View Tools Help Component Library **Project Settings** Instance Parameters System Inspector HDL Example Generation System Contents Address Map Clock Settings × ÷ Use Connections Name Description Expo Ided Processors × clk1 Clock Input ice Protocols -2 Avalon Memory Mapped Slave ries and Memory Controllers s1 Components Reset Input reset1 \mathbf{Z} 1 controller Peripherals System ID Peripheral sysid gsys clk Clock Input erals Reset Input reset \mathbf{v} Avalon Memory Mapped Slave Interconnect control slave Y 1 ΗВ Ied PIO (Parallel I/O) KI Interface 7 clk Clock Input Reset Input errupt reset emory-Mapped s1 Avalon Memory Mapped Slave i-State Components external_connection Conduit led — Onduit Pin Divider Onduit Ond V cfi flash Generic Tri-State Controller Generic Tri-State Controller clk Clock Input Tri-State Conduit Bridge Reset Input reset Tri-State Conduit Bridge Tra Avalon Memory Mapped Slave E uas Tri-State Conduit Pin Sharer ... 🔘 tcm Tristate Conduit Master \checkmark E tristate conduit pin sharer (Ti State Conduit Pin Sharer cation Connections w Bridge clk reset ₹. 111 ь Filter tcm tcs0 ÷ Add... New... Edit. ٠. Edit... Ctrl+E 111 Þ 2 2 Ctrl+R Rename Messages Duplicate Ctrl+D Description Path × Remove 🗆 🔀 4 Errors Details ۰ System.cfi_flash Cfi flash.clk must be connected to a clock output Show Arbitration Shares 97 ÷ Ω. Syntam trintata 4 Errors, 3 Warnings Lock Base Address

& Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)							
File Edit System View Tools Help							
Component Library	Project \$	La Tri-State Conduit Bridge - tristate_conduit_bridge_0	X				
Image: Control of the second secon	Use Use Use V V V V	Tri-State Conduit Bridge altera_tristate_conduit_bridge Block Diagram Show signals tristate_conduit_bridge_0 clk clk clk clk clk	Documentation				
(double-click) ● Generic Tri-State Controller ● Tri-State Conduit Bridge ● Tri-State Conduit Pin Sharer ● Tri-State Conduit Pin Sharer ● Tri-State Conduit Pin Sharer ● Bridge ● Mew Edit		uas tcm tristate_bridge_flash_pin_sha clk reset tcm tcs0 III	Cancel Finish Avalon Memory Mapped Slave Image: Conduit Master Tristate Conduit Master Image: Conduit Pin Sharer Clock Input Image: Conduit Master Tristate Conduit Master Image: Conduit Master Tristate Conduit Master Image: Conduit Master Tristate Conduit Slave Image: Conduit Slave				
Messages							
Description		Path	8				
E 🔀 4 Errors			<u>^</u>				
Cfi_flash.clk must be connected t	o a clock output	System.cfi_flash	98				
4 Errors, 3 Warnings		Svotom triototo brid	lao flooh sin ohoro				

👃 Qsys - DE2_115_QSYS.qsys* (C:\U	lsers\1	rume	n\Desktop\Pro	ject\DE2_115_	QSYS.qsys)					×
File Edit System View Tools Help										
Component Library		Project	Settings	Instance Pa	rameters	System Inspe	ector	HDL Example	Gene	ration
			System Cont	tents		Address Map		Cloc	k Settings	
Ided Processors		Use	Connections		Name			Description		E:
ice Protocols	×		+ +	>	reset			Reset Input		
ries and Memory Controllers			🔶 🕂		control_s	slave		Avalon Memory Mapp	ed Slave	
Components		1			🗆 led			PIO (Parallel I/O)		
controller Peripherals			♦	>	clk			Clock Input		
erals			+ + +	>	reset			Reset Input		
	-		🔶 🔶	>	s1			Avalon Memory Mapp	ed Slave	
Interconnect					external_	_connection		Conduit		lei
HB		V			cfi_flash			Generic Tri-State Con	troller	
KI Interface	8			>	clk			Clock Input		
terrupt		reset					Reset Input			
emory-Mapped		uas uas					Avalon Memory Mapp	ed Slave		
i-State Components		tcm					Tristate Conduit Maste	er		
····· Conduit Pin Divider		✓				share	Tri-State Conduit Pin S	Sharer		
Generic Tri-State Controller					CIK			Clock Input		
···· @ Tri-State Conduit Bridge					reset			Reset Input		
Tri-State Conduit Bridge Tra					tcm			Tristate Conduit Maste	er	=
In-State Conduit Pin Sharer				$\phi = \phi \longrightarrow \phi$	tcs0	and the balance of	_	Tristate Conduit Slave		
cation					tristate_c	conduit_bridge_u	71	TheState Conduit Bride		
w Bridge 👻					CIK			Connections	•	
4 III •					reset		0	F iller		
					out		Y	Filter	•	
New Edit		•		m	our			Edit	Ctrl+E	•
Messanes	,							Rename 2	Ctrl+R	
								Duplicate	Ctrl+D	
Description Path							×	Remove		
Errors							Details	+	-	
Cfi_flash.clk must be connected to a clock output System.cfi_flash							Show Arbitration Share	99		
6 Errors, 5 Warnings	6 Errors, 5 Warnings						-	Show Arbitration Share		-
-							A .	Lock Base Address		

👃 Qsys - DE2_115_QSYS.qsys* (C:\U	lsers\Ti	rumer	n\Desktop\F	Project\DE2_115	_QSYS.qsys)				x
File Edit System View Tools Help									
Component Library	F	Project	Settings	Instance P	arameters	System Inspector	HDL Example	Generation	n
			System C	ontents		Address Map Clock Settings			
× ×	ا هر ا								
Ided Processors		Use	Connections	3	Name		Description	E	3
ice Protocols	×		+ + +	+	→ reset		Reset Input		
ries and Memory Controllers			🔶 🕂		control_s	slave	Avalon Memory Mapped	Slave	
Components	·	1			🗆 led		PIO (Parallel I/O)		
controller Peripherals			♦		≻ <mark>clk</mark>		Clock Input		
erals			+	+	reset		Reset Input		
	-		🔶 🕂		≻ s1		Avalon Memory Mapped	Slave	
Interconnect	-			1	external	_connection	Conduit	le	31
НВ	. –	V		+•	🗆 cfi_flash		Generic Tri-State Control	ler	
KI Interface	8		♦	+	≻ clk		Clock Input		
errupt	"		+	+	> reset		Reset Input		
emory-Mapped			🔶 🔶	+	uas		Avalon Memory Mapped	Slave	
i-State Components					< tcm		Tristate Conduit Master		
Conduit Pin Divider		\checkmark			tristate_l	bridge_flash_pin_share	Tri-State Conduit Pin Sha	rer	
···· Generic Tri-State Controller			•		→ clk	2	Clock Input		
Tri-State Conduit Bridge			♦	♦	reset	(double-click)	Reset Input		
···· Tri-State Conduit Bridge Tra					< tcm		Tristate Conduit Master		
···· Tri-State Conduit Pin Sharer				++	tcs0		Tristate Conduit Slave		=
cation		V			🗆 tristate_l	bridge_flash	Tri-State Conduit Bridge		
w Bridge 👻 👻			♦ -		→ clk		Clock Input		
4 III >			∣ ∔	↓ ↓ ↓	reset		Reset Input		
				↓	→ tcs		Tristate Conduit Slave		
					out		Conduit		Ŧ
New		•							
Марралар	,								_
messayes						1			
Description						Path			
🗆 🔀 2 Errors									-
Sonchip_memory2.s1 (0x40000.	.0x7ffff) overla	aps cfi_flash	uas (0x00x7ffff	;)	System.nios2_qsys.data_	_master 10	00	
					n	Svotom pipo?	untion montor		

👃 Tri-State Conduit Pin Sharer - tristate_bridge_flash_pin_share

1	Tri-State Con	nduit Pin Sharer						
MegaCore'	altera_tristate_conduit	t_pin_sharer					Docume	ntation
- Block I	Diagram	Parameters						
Chow		Number of Interfaces: 1						
Show	signais							
	triototo bridgo floch	Sharing Assignment						
	instate_bridge_ilash	To share a signal, type the sa	me signal name in the S	hared Signal Name c	column for all control	ers that share that signa		
clk	alaali tiir							
reset	CIOCK UIS	Update Interface Table	1				_	
10001	reset	Interface	Signal Role	Signal Type	Signal Width	Shared Signal Name		
tcsu	tristate_conduit	cfi flash.tcm	address	Output	23	fs addr		
	altera_trist	cfi flash.tcm	outputenable n	Output	1	fl read n	2	
L		cfi_flash.tcm	write_n	Output	1	fl_we_n	14	
		cfi_flash.tcm	data	Bidirectional	8	fs_data		
		cfi_flash.tcm	chipselect_n	Output	1	fl_cs_n		
•	4 [1]	+ -		III				•
								2
							101	3
						Ca	incel	Finish
and the second			and the second second	energen en en en en en en			المصرعتي وتوالل النقرا	-

х

Component Library	Project Settings	Instance Parame	ters System Inspect	tor HDL Example	Generation
	System 0	Contents	Address Map	Clock Set	tings
 X 					
Ided Processors	Tons ons	Name	Description	Export	Clock
ice Protocols	× + +	→ reset	Reset Input	Double-click to export	[clk]
ries and Memory Controllers		→ control_slave	Avalon Memory Mapp.	Double-click to export	[clk]
Components		🖂 led	PIO (Parallel I/O)		
controller Peripherals		→ clk	Clock Input	Double-click to export	clk_50
erals		→ reset	Reset Input	Double-click to export	[clk]
	-	→ s1	Avalon Memory Mapp.	Double-click to export	[clk]
Interconnect	-	external_connec	tion Conduit	led	
HB	. –	□ cfi_flash	Generic Tri-State Cont	t	
KI Interface	8	→ clk	Clock Input	Double-click to export	clk_50
errupt	" 	→ reset	Reset Input	Double-click to export	[clk]
emory-Mapped	•	→ uas	Avalon Memory Mapp.	Double-click to export	[clk]
i-State Components		-≺ tcm	Tristate Conduit Maste	Double-click to export	[clk]
···· Conduit Pin Divider		tristate_bridge_	flash Tri-State Conduit Pin S		
@ Generic Tri-State Controller		→ clk	Clock Input	Double-click to export	clk_50
···· Tri-State Conduit Bridge		→ reset	Reset Input	Double-click to export	[clk]
····· Tri-State Conduit Bridge Tra		-≺ tcm	Tristate Conduit Maste	Double-click to export	[clk] ,
···· Tri-State Conduit Pin Sharer		→ tcs0	Tristate Conduit Slave	Double-click to export	[clk]
cation		tristate_bridge_	flash Tri-State Conduit Bridg	je	
w Bridge 👻 👻		→ clk	Clock Input	Double-click to export	clk_50
↓ Ⅲ ▶	•	→ reset	Reset Input	Double-click to export	[clk]
	○ — ♦ ——	→ tcs	Tristate Conduit Slave	Double-click to export	[clk]
New Edit		out	Conduit	tristate_bridge_flash_out	1
	•		III		•
lessages					
Description			Path		ſ
2 Errors					
Onchip memory2.s1 (0x40000.0	x7ffff) overlaps cfi_flash	uas (0x00x7fffff)	System.nios2_qsys.d	lata master	

& Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)

File Edit System View Tools Help

Component Library		Project	Settings	Instance Pa	rameters	System In	spector	or HDL Example Generatio		Generatio	n
			System Co	ontents		Address Map)		Clock Se	ttings	
Kind December 2	+	Use	Connections		Name		Description		Export		
aded Processors	X						Clock Sources				-
rise and Memory Controllers		×					Clock Input		clk		Â
Components				•	clk_in_n	eset	Reset Input		reset		
controller Peripherals					clk	4	Clock Output		Double	- click to ove	
erals					clk rese	(double-click)	Reset Output		Double	-click to exp	
		V			nios2_q	sys	Nios II Proces	sor	Double	Contra to copi	
Interconnect			•		clk		Clock Input		Double	e-click to exp	0
нв	_ ▲		♦	$\bullet \longrightarrow$	reset_n		Reset Input		Double	e-click to exp	0
KI Interface	8				data_ma	aster	Avalon Memo	гу Марр	Double	e-click to exp	0
errupt	"		c		instructi	on_master	Avalon Memo	гу Марр	Double	e-click to exp	0
emory-Mapped				≻≺	jtag_det	oug_module_reset	Reset Output		Double	a-click to exp	₀└──
i-State Components			+ + -	\rightarrow	jtag_debug_module		Avalon Memo	гу Марр	Double	a-click to exp	D
···· Conduit Pin Divider				×	custom_	_instruction_mas	. Custom Instru	ction Ma	Doubl	e-click to exp	0
Generic Tri-State Controller		\checkmark			⊟ jtag_uart		JTAG UART				
Tri-State Conduit Bridge					Clk		Clock Input		Double	a-click to exp	D
Tri-State Conduit Bridge Tra				₽ `	reset		Reset Input		Double	e-click to exp	D
etice				· · · · · · · · · · · · · · · · · · ·	avaion_	itag_slave	Avaion Memo	ry mapp	Double	e-click to exp	0
w Bridge		V		ļ		nemoryz	Clock Input	огу (ка	Devil		
w bridge				,	e1		Avalon Memo	ny Mann	Double	echick to exp	
4				<u>ن</u>	reset1		Reset Input	гу марр	Double	2-click to exp	
				Í		avs.	System ID Per	ripheral	Double	2=CITCK to expo	, ÷
New Edit		•							1	•	
							2				
Messages											
Description						Path					
🗆 🔀 2 Errors											-
Onchip_memory2.s1 (0x400000x7ffff) overlaps cfi_flash.uas (0x00x7ffff)						System.nios2_qsys.data_master 103					
2 Errors, 1 Warning	- 7///	<u> </u>	<i></i>			Evotom pipo?	ovo instruction	mantar			-

🚣 Nios II Processor - nios2_qsys

-
MegaCore

Nios II Processor

MegaCore altera_nios2_qs	ys		Documentati
🔻 Block Diagram	Hardware multiplication type:	Embedded Multipliers 👻	
Show signals	Hardware divide		
	Reset Vector		
	Reset vector memory:	cfi_flash.uas	
clk	Reset vector offset:	0×0000000 1	
reset_n	Reset vector:	0×0000000	
d_irq			
itag_debug_module	Exception Vector		
	Exception vector memory:	onchip_memory2.s1	
	Exception vector offset:	0×0000020	
	Exception vector:	0x00040020	
	MMU and MPU		
	Include MMU		
	Only include the MMU using an open	ating system that explicitly supports an MMU.	
۰ III ۲	•		

X

Documentation

Cancel Finish

🚣 Qsys	Qsys - Dt2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)									
File Edit	Syste	m View Tools Help								
Compon		Upgrade IP Cores	Instance Pa	arameters	System In	spector	HDL Example	Generation		
		Assign Base Addresses 2	em Contents		Address Map		Clock Settings			
		Assign Interrupt Numbers	ctions	Name	Name		scription Export			
ided Pro		Assign Custom Instruction Opcodes		⊟ clk 50		Clock Source				
ries and		Create Clebal Baset Network		clk in		Clock Input				
Compo		Create Global Reset Network	• • • • • • • • • • • • • • • • • • •	clk_in_re	set	Reset Input	reset			
controlle		Show System With Osys Fabric Components	clk		Clock Output	D	ouble-click to expo			
erals		Show System with asyst ablic components	' <u> </u>	clk_reset	t	Reset Output	D	ouble-click to expo		
		Run SOPC Builder to Qsys Upgrade		🗖 nios2_qs	ys	Nios II Process	sor			
Intercor		Describe Describe Constanting	;	• clk		Clock Input	D	ouble-click to expo		
HB		Remove Dangling Connections	+	reset_n		Reset Input	D	ouble-click to expo		
KI Interfa	ace			data_mas	ster	Avalon Memor	ry Mapp Do	ouble-click to expo		
errupt				instructio	on_master	Avalon Memor	y Mapp Do	ouble-click to expo		
emory-Mapped			jtag_debu	ug_module_reset	Reset Output	D	ouble-click to expo			
i-State Components jtag_de		jtag_debu	ug_module	Avalon Memor	y Mapp Do	ouble-click to expo				
© C	onduit	Pin Divider		x		Custom Instru	ction Ma Do	ouble-click to expo		
© G	enerio	Coodult Bridge				JIAG UARI				
	-Stat	e Conduit Bridge		CIK		Clock input		ouble-click to expo		
	i Stat	e Conduit Dindge Tra		avalon it		Avalon Memor	D Mann	ouble-click to expo		
nation	Folai				ay_slave	Avaion Memor	y mapp Do	DUDIE-CIICK to expo		
w Bride	•			clk1	iemory2	Clock Input	NY (NA	auble aliak ta avea		
di la contrag				s1		Avalon Memor	v Mann D	ouble-click to expo		
· ·			↓ I I ↓ ,	reset1		Reset Input	J mapp D(ouble-click to expo		
				E sysid as	vs	System ID Per	ipheral	vabre-crick to expo		
New			<u> </u>	1	,-]		4		
						2				
Message	s									
Descrip	tion				Path					
🗆 🔀 2 Er	rors							×		
Onchip_memory2.s1 (0x400000x7ffff) overlaps cfi_flash.uas (0x00x7fffff)						System.nios2_qsys.data_master 105				
0			C D 1 (0 0 0 7////	s	Svotom pipo? a	ava instruction	mantar	· · · · · · · · · · · · · · · · · · ·		
2 Errors,	1 Wa	rning								

1.85

🖕 Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)						
File Edit System View Tools Help						
Component Library	System Co	ontents		Address Map	Clock Se	ettings
	Project Settings	Instance Parame	eters	System Inspector	HDL Example	Generation
dded Processors ice Protocols ries and Memory Controllers Components controller Peripherals erals Interconnect HB KI Interface cerrupt	The testbench system Once generated, the Create testbench Q Create testbench si Synthesis Synthesis files are Create HDL design files	is a new Qsys system ave changes? Save chang 3 Save s for synthesis: Verilog	that instanti	ates the original system, adding	g bus functional models	to drive the top
emory-Mapped i-State Components 	Create block symbols Output Directory Path: Simulation: Testbench: Synthesis: Generate 2	 Info: Reusing file C: Info: Reusing file C: Info: Reusing file C: Info: irq_mapper: Info: tdt: "cfi_flash Info: tda: "cfi_flash Info: pin_sharer: " Info: arbiter: "trist Info: DE2_115_QSY Info: ip-generate su 	ted /Users/Tru /Users/Tru "DE2_115_(" instantiate " instantiate tristate_bri ate_bridge 'S: Done DE cceeded.	Imen/Desktop/Project/DE2_ Imen/Desktop/Project/DE2_ QSYS" instantiated altera_irq_ ed altera_tristate_controller ed altera_tristate_controller ridge_flash_pin_share" insta e_flash_pin_share" instantiat 2_115_QSYS" with 35 modules	115_QSYS/synthesis 115_QSYS/synthesis mapper "irq_mappe _translator "tdt" r_aggregator "tda" antiated altera_tristate ed altera_merlin_std s, 97 files, 3113638 byt	/submodi /submodi r" e_conduit I_arbitratc es
Messages		Info: Finished: Creater of the second sec	ate HDL de	sign files for synthesis		-
Description Image: Description	e,isNonVolatileStorage) h	▲ Generate Completed	1. 0 Errors, (62 Warnings	Stop 10	4 Close



	module NiosII (
	clk,	
	rst_n,	
	led,	
	// flash	S- B-
	FL_ADDR,	ALC: N
	FL_CE_N,	
	FL_DQ,	
	FL_OE_N,	
	FL_RESET_N,	
	FL_RY,	
	FL_WE_N,	
	FL_WP_N	
);	
	<pre>input clk, rst_n;</pre>	
	<pre>output [7:0] led;</pre>	Control of
	// flash	No.
	<pre>output [22:0] FL_ADDR;</pre>	1110
	output FL_CE_N;	- ANA
	<pre>inout [7:0] FL_DQ;</pre>	The second
	output FL_OE_N;	
	<pre>output FL_RESET_N;</pre>	CHICA D
	<pre>input FL_RY;</pre>	
	output FL_WE_N;	
1000	output FL_WP_N;	City of
	DE2_115_QSYS_DE2_115_QSYS_inst (ALL A
	.clk_clk(clk),	日日
	.reset_reset_n(rst_n),	ALC: N
	.led_export(led),	A.M.
	// flash	
	.tristate_bridge_flash_out_fs_addr(FL_ADDR),	
	.tristate_bridge_flash_out_fl_read_n(FL_OE_N),	Tar Ba
	.tristate bridge flash out fl cs n(FL CE N),	
	.tristate bridge flash out fs data(FL DQ),	CHUR I
	.tristate_bridge_flash_out_fl_we_n(FL_WE_N),	
);	1111
	// flash config	144
	assign FL RESET N = $1'b1;$	
	assign FL WP N = $1'b1$;	 ALC: NO
并并 并不 于于不不	endmodule	H-H
distin		Si a




NodeName	Direction	Location
FL_ADDR[0]	Output	PIN_AG12
Put FL_ADDR[1]	Output	PIN_AH7
Strain FL_ADDR[2]	Output	PIN_Y13
Put FL_ADDR[3]	Output	PIN_Y14
Put FL_ADDR[4]	Output	PIN_Y12
Put FL_ADDR[5]	Output	PIN_AA13
Put FL_ADDR[6]	Output	PIN_AA12
Put FL_ADDR[7]	Output	PIN_AB13
Put FL_ADDR[8]	Output	PIN_AB12
Put FL_ADDR[9]	Output	PIN_AB10
Put FL_ADDR[10]	Output	PIN_AE9
Put FL_ADDR[11]	Output	PIN_AF9
Price FL_ADDR[12]	Output	PIN_AA10
Put FL_ADDR[13]	Output	PIN_AD8
Put FL_ADDR[14]	Output	PIN_AC8
STL_ADDR[15]	Output	PIN_Y10
Put FL_ADDR[16]	Output	PIN_AA8
Put FL_ADDR[17]	Output	PIN_AH12
Strain FL_ADDR[18]	Output	PIN_AC12
Put FL_ADDR[19]	Output	PIN_AD12
Put FL_ADDR[20]	Output	PIN_AE10
Strain FL_ADDR[21]	Output	PIN_AD10
Set FL_ADDR[22]	Output	PIN_AD11
Set FL_CE_N	Output	PIN_AG7
FL_DQ[0]	Bidir	PIN_AH8

Node Name	Direction	Location
PUT FL_CE_N	Output	PIN_AG7
FL_DQ[0]	Bidir	PIN_AH8
FL_DQ[1]	Bidir	PIN_AF10
FL_DQ[2]	Bidir	PIN_AG10
🖳 FL_DQ[3]	Bidir	PIN_AH10
FL_DQ[4]	Bidir	PIN_AF11
FL_DQ[5]	Bidir	PIN_AG11
FL_DQ[6]	Bidir	PIN_AH11
FL_DQ[7]	Bidir	PIN_AF12
PUS FL_OE_N	Output	PIN_AG8
STATEST N	Output	PIN_AE11
EL_RY	Input	PIN_Y1
STL_WE_N	Output	PIN_AC10
ST FL_WP_N	Output	PIN_AE12
in_ clk	Input	PIN_Y2
º ^{ut} led[0]	Output	PIN_E21
º ^{ut} led[1]	Output	PIN_E22
º ^{ut} led[2]	Output	PIN_E25
º ^{ut} led[3]	Output	PIN_E24
º ^{ut} led[4]	Output	PIN_H21
º ^{ut} led[5]	Output	PIN_G20
eut led[6]	Output	PIN_G22
eut led[7]	Output	PIN_G21
in_ rst_n	Input	PIN M23
< <new node="">></new>		





Edit View Proc	essing Tools Window	Help 💎			Search altera	.com 🔇
Hardware Setup	USB-Blaster [USB-0]	Mode: JTA	3	 Progr 	ess:	
Enable real-time ISP t	o allow background program	mming (for MAX II and	d MAX V devices)			
🎾 Start	File	Device	Checksum	Usercode	Program/ Configure	Verify Blank- Check
Ju Stop	output_files/NiosII.sof	EP4CE115F29	008BF0FD	008BF0FD		
Auto Detect						
Add File						
Change File	•					۴.
Save File						<u>^</u>
Add Device						
1 ¹⁰ Up						
J [™] Down						=
	EP4CE115F	29				
	↓ TDO					
						-

🔔 Hardware Setup	USB-Blaster [USB-0]	Mode: JTAC	3	▼ Progr	ess: 100%	% (Success	ful)
Enable real-time I	SP to allow background progra	amming (for MAX II and	d MAX V devices)				
Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check
Stop	output_files/NiosII.sof	EP4CE115F29	008BF0FD	008BF0FD			
Auto Detect							
🔀 Delete							
Add File							
쌸 Change File							
Save File							
Add Device							
Dp							
Down							=
	EP4CE115	iF29					



Nios II - Hello Nios II/bello world c - Ec						
File Edit Source Refector Navigate		Сору	Ctrl+C			
The Edit Source Relactor Navigate	Ē	Paste	Ctrl+V			
	×	Delete	Delete		👻 / 🖹	🅸 Nios II Debug
抱 ▼ ね ▼ 🏷 🔶 ▼ 🔿 ▼	<u>_</u>	Remove from Context	Ctrl+Alt+Shift+Down			Nios II 🚾 C/C++
🎦 Project Explorer 🕱 📃 🗖		Source	+			- 8
	1	Move				*
⊳ 😂 Hello_NiosII	1 (***	Rename	F2	L .		
▷ 100 Hello_NiosILbsp [DE2_115_QSY	i (ng	Import		L .		
	4	Export		L .		
		Build Project		L .		
		Clean Project		L .		
	ক্লা	Refresh	F5	L		
		Close Project		lunc	.) .	
		Close Unrelated Projects				
		Puild Configurations		L .		
		Make Terrete		L .		
		Index		L .		
		Index	,	L .		
		Show in Remote Systems view				Ψ
		Convert To		⊨		4
		Run As	•	ebu	9	
		Debug As	•			
		Profile As	•		Path	Location
		Team	•	⊢		
		Compare With	•	⊢		
		Restore from Local History	[-	2	
		Nios II 2	•		Nios Comman	d Shell.
E State NC+T bar	*	Run C/C++ Code Analysis			Generate BSP	
		Properties	Alt+Enter		BSP Editor	

😂 Nios II - Hello_Ni		Go Into			
File Edit Source		Open in New Window			Help
📑 🗖 🖬 🖨	Ð	Сору	Ct	rl+C	🝷 😕 😂 👻 🌛 🤪 📑 🏇 Nios II Debug
2 ▼ 2 ▼ 10 0	Ē	Paste	Ct	rl+V	Nios II Ic C/C++
Project Explorer	×	Delete	De	elete	
	<u>_</u>	Remove from Context	Ctrl+Alt+Shift+D	own .	A
▷ 100 Hello_NiosI	1 (rig	Source ht-click)		•	şs.h"
▷ 📂 Hello_NiosII		Rename		F2	
	~	T			
	21 . 7	Import);
		Build Project 2			<pre>(LED_BASE, 1 << count);</pre>
	இ	Refresh		F5	
	~	Close Project			
		Close Unrelated Projects			
		Build Configurations		+	
		Make Targets		+	
		Index		•	4
		Show in Remote Systems view			Properties 🕸 Debug
		Convert To			
		Run As		+	<pre>imen\Desktop\Project\software\Hello_NiosII_bsp\link ^</pre>
		Debug As		+	<pre>imen\Desktop\Project\software\Hello_NiosII_bsp\IInk imen\Desktop\Project\software\Hello_NiosII_bsp\memc</pre>
		Profile As		+	<pre>imen\Desktop\Project\software\Hello_NiosII_bsp\Make s. Total time taken = 2 seconds</pre>
		Leam		•	<pre>Jsers\Trumen\Desktop\Project\software\Hello_NiosII_</pre>
		Restore from Local History		,	118
📑 🗘 🔁 Hel		Nios II		+	
		Run C/Cr + Cada Arabaia	at at at at at at at at at a d		

		Сору	Ctrl+C	
Nios II - Hello_Nic	Ê.	Paste	Ctrl+V	
File Edit Source	×	Delete	Delete	Help
i 📬 🗕 🖬 🖷 🖻	8	Remove from Context	Ctrl+Alt+Shift+Down	🝷 🤌 🔁 🥒 🥪 👘 📅 🖄 😵
½ - 🖓 - 🌤 🤇		Source	•	Nios II 🔤 C/C++
Project Explorer		Move		
		Rename	F2	
	1	Import		
	L(rig	ht/click)rt		;s.h"
	Ľ	export		
		Build Project		."):
		Clean Project		/3
	\$	Refresh	F5	
		Close Project		(LED_BASE, 1 << count);
		Close Unrelated Projects		
		Build Configurations	•	
		Make Targets	•	
		Index	+	
		Show in Remote Systems view		
		Convert To		
		Run As	•	4
		Debug As	•	Properties A Debug
		Profile As	•	
		Team	•	s free for stack + heap.
		Compare With	•	ip
		Restore from Local History		symsair-neadersource Herro_Niosir.elf
II [Nios II 2	•	BSP Editor
	*	Run C/C++ Code Analysis		Nios II Command Shell
		Update Linked Resources		Flash Programmer 3
📑 🗘 🔁 Hell		Properties	Alt+Enter	
	12-12-1	Properties	Ait+Enter	

🛃 Nios I	II Flash F	Programmer							
File Optio	ons Tools	Help							
New	v	2							
Op e Sai Sai	S Nev	v Flash Programme	er Settings File	e 200 0. W 51-			×	1	
Exi	 Get Get 	flash programmer sys flash programmer sys	tem details from tem details from	SOPC Information File				Instance ID:	Connections
Nios II		BSP Settings File	name;				3		
This too	:	SOPC Information File	name:						
lt parse		Master CPU	name:	· · ·				lash device found	i.
Each Fl		Flash m	emory:					sh device.	
Use the					OK		Cancel		
or open a	an existi	ng project using the	e File->Open n	nenu item.					
		🛓 Select SOPC I	Information D	esign File				×	
		Look in:	🔒 Project		•) 🤌 📂 🖪			
		最近的項目	.qsys_edit	t DE2_	115_QSYS.sopcinfo 4				
Informati	ion Prob		incremental incremental output_file software	al_db es					
	_	泉面	workspace	2			5		
	_	我的文件	File name:	DE2_115_QSYS.sopcin	fo		Select	Start	120
			Files of type:	SOPC Information File	(.sopcinfo)	•	Cancel		0

실 Nios II F	lash Programmer		
File Options	실 New Flash Programmer S	Settings File	
-Target hard BS SOPC Ir	 Get flash programmer system Get flash programmer system 	n details from BSP Settings File n details from SOPC Information File	
c	BSP Settings File na	me:	
F	SOPC Information File na	me: C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.sopcinfo	Connections
Flash: cfi_fla	Master CPU na	me: nios2_qsys 🔻	
Base add Master	Flash memo	ory: cfi_flash	
Files for flas		OK Cancel	2 Add
File generation	on command: ming command: Problems Processing	Select File for Flash Conversion Look in: Hello_NiosII ● ●	

🔬 Nios II Flash Programmer	
File Options Tools Help	
Target hardware information	
BSP Settings File name:	
SOPC Information File name: C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.sopcinfo	
CPU to program flash: nios2_gsys	
Hardware connection: Connection: USB-Blaster on localhost [USB-0] Device: EP3C120 [EP4CE115@1 Device ID: 1 CPU Instance ID:	Connections
Flash: cfi_flash	
Base address: 0x800000 Memory span: 0x800000	
Master CPU: nios2_qsys .zip file system offset in BSP:	
Files for flash conversion:	
File Name Conversion Type Flash Offset	Add
<pre>C:\Users\Trumen\Desktop\Project\software\Hello_NiosII\Hello_NiosII.elf ELF <no offset=""></no></pre>	Remove
File generation command:	
elf2flashinput="Hello_NiosII.elf"output="C:/Users/Trumen/Desktop/Project/flash/Hello_NiosII_cfi_flash.flash"	Properties
boot="D:/altera/13.0sp1/nios2eds/components/altera_nios2/boot_loader_cfi.srec"base=0x800000end=0x1000000	
reset=UX8UUUUUverbose	
File programming command:	
nios2-flash-programmer "C:/Users/Trumen/Desktop/Project/flash/Hello_NiosII_cfi_flash.flash"base=Ox800000	
sidp=Ox1081010id=OxOtimestamp=1392441113device=1instance=O 'cable=USB-Blaster on localhost [USB-O]'	
programveroose	
Information Problems Processing	
Start	Exit
	-122

🙆 Nios II Flash Programmer	- 0 X							
File Options Tools Help								
Target hardware information]							
BSP Settings File name:								
SOPC Information File name: C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.sopcinfo								
CPU to program flash: nios2_qsys								
Hardware connection: USB-Blaster on localhost [USB-0] Device: EP3C120 [EP4CE115@1 Device ID: 1 CPU Instance ID: Connections								
Flash: cfi_flash								
Base address: 0x800000 Memory span: 0x800000								
Master CPU: nios2_qsys .zip file system offset in BSP:								
Files for flash conversion:								
File Name Conversion Type Flash Offset	Add							
C:\Users\Trumen\Desktop\Project\software\Hello_NiosII\Hello_NiosII.elf ELF <no offset=""></no>	Remove							
File generation command:								
elf2flashinput="Hello_NiosIl.elf"output="C:/Users/Irumen/Desktop/Project/flash/Hello_NiosIl_cfl_flash.flash"	Properties							
reset=0x800000verbose								
File programming command:								
nios2-flash-programmer "C:/Users/Trumen/Desktop/Project/flash/Hello NiosII cfi flash.flash"base=0x800000								
sidp=Ox1081010id=Ox0timestamp=1392441113device=1instance=0 'cable=USB-Blaster on localhost [USB-0]'								
programverbose 🔻								
Information Problems Processing								
Leaving target processor paused	÷							
<	1 1							
Start 1.	2 Exit							
	0							

Finally...

- Restart power on the development board.
- Download NiosII.sof of your project "NiosII" to the board.
- You will see that the LEDs blink!





Reference

- 1. "My First Nios II for Altera DE2-115 Board" by Terasic Technologies Inc.
- 2. "My First Nios II for Altera DE2i-150 Board" by Terasic Technologies Inc.
- 3. "DE2-115 User Manual" by Terasic Technologies Inc.

