My First Nios II for Altera DE2-115 Board

Digital Circuit Lab

TA: Po-Chen Wu

Outline

- Hardware Design
- Nios II IDE Build Flow
- Programming the CFI Flash

Hardware Design

Introduction

- This slides provides comprehensive information that will help you understand how to create a FPGA based SOPC system implementing on your FPGA development board and run software upon it.

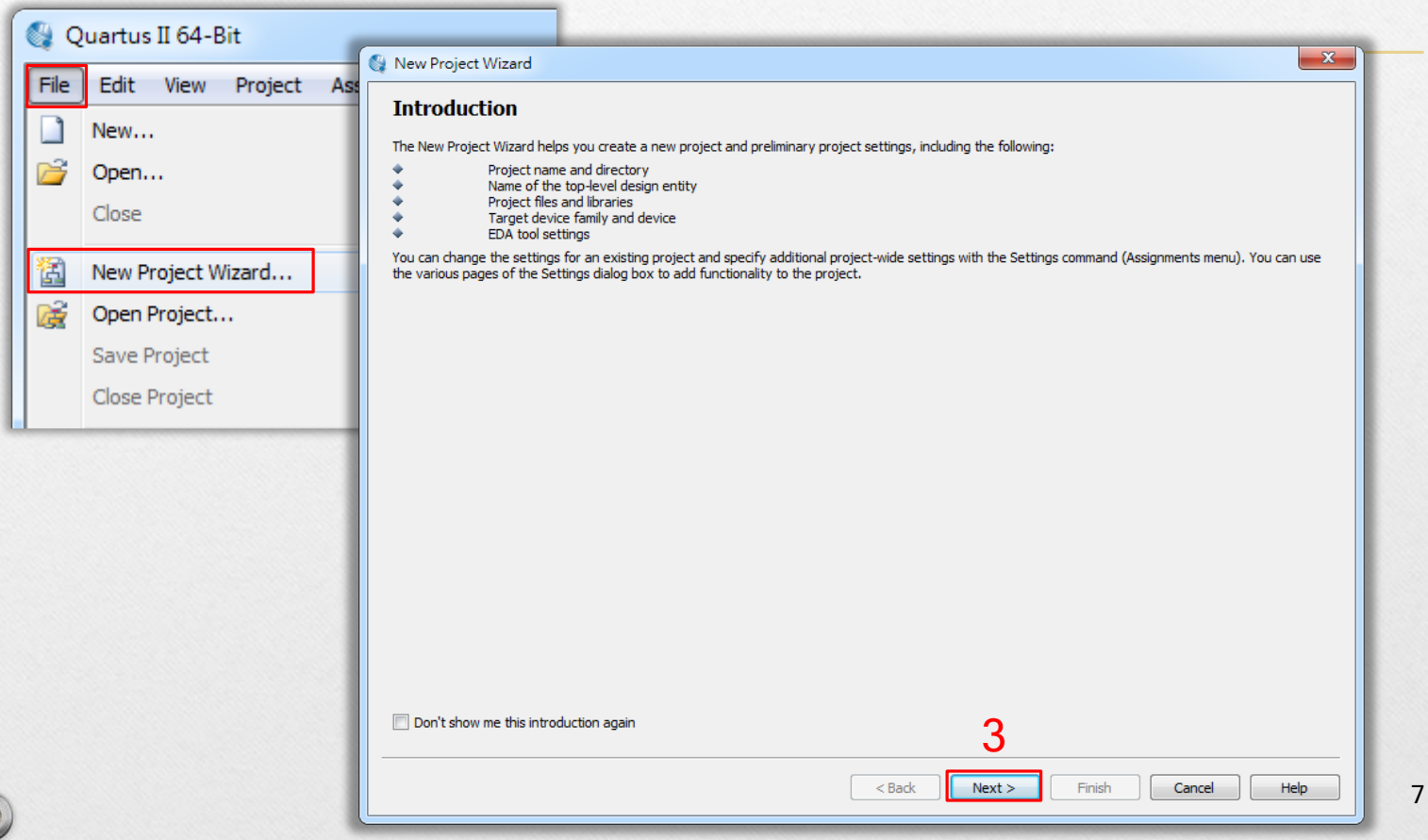
Required Features (1/2)

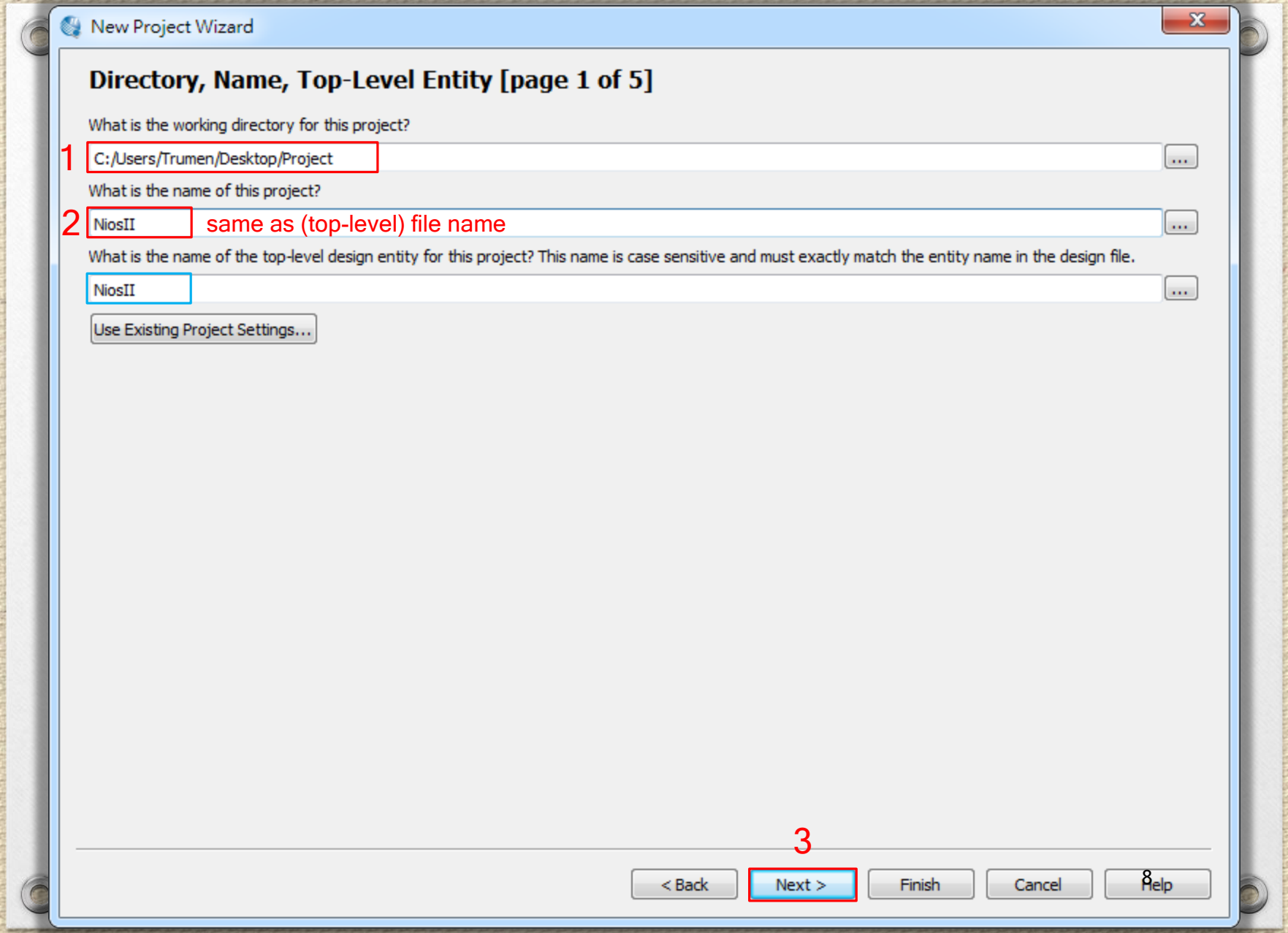
- The Nios II processor core is a soft-core central processing unit (CPU) that you could program onto an Altera field programmable gate array (FPGA).
- This chapter illustrates you to the basic flow covering hardware creation and software building.

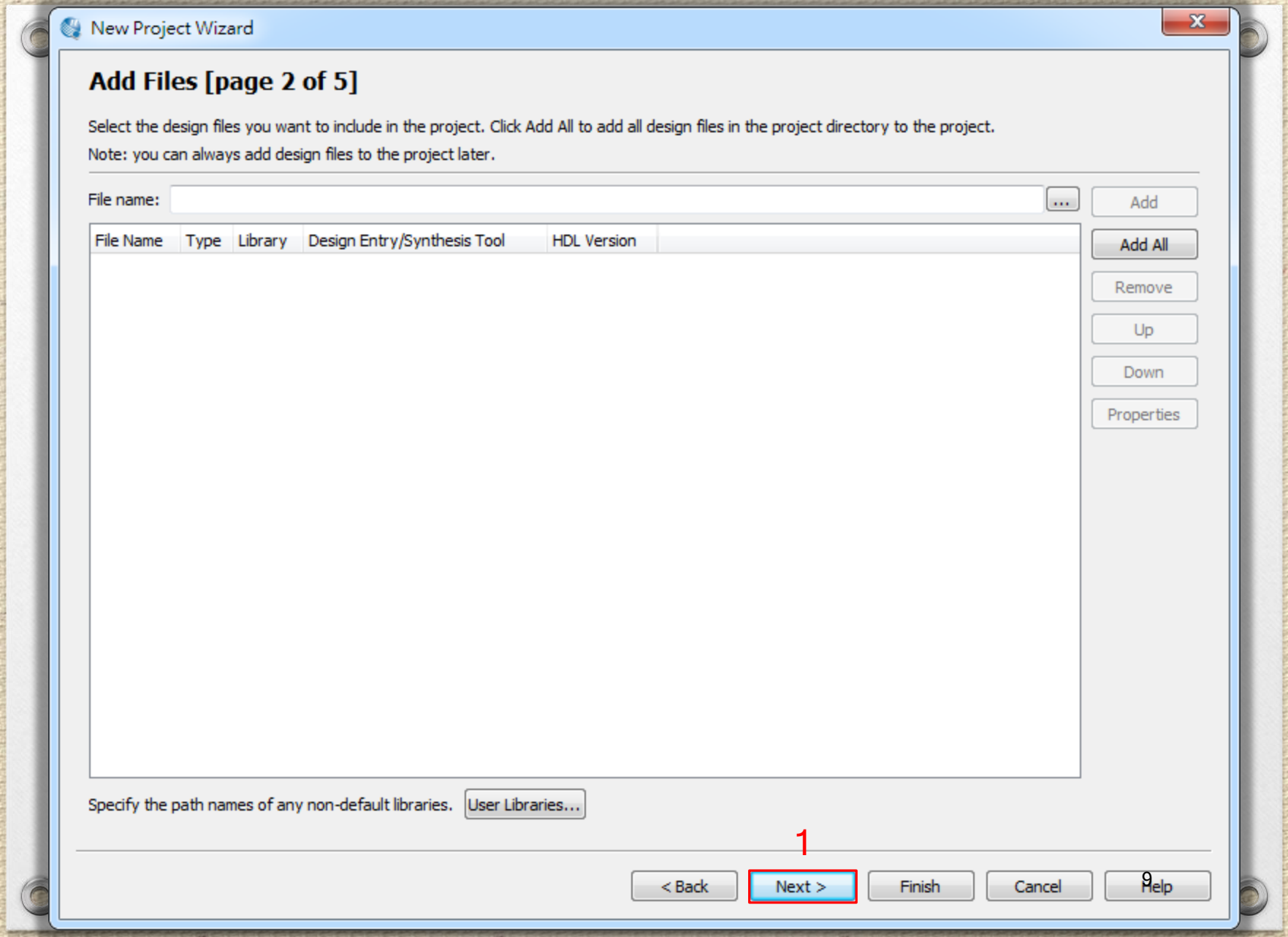
Required Features (2/2)

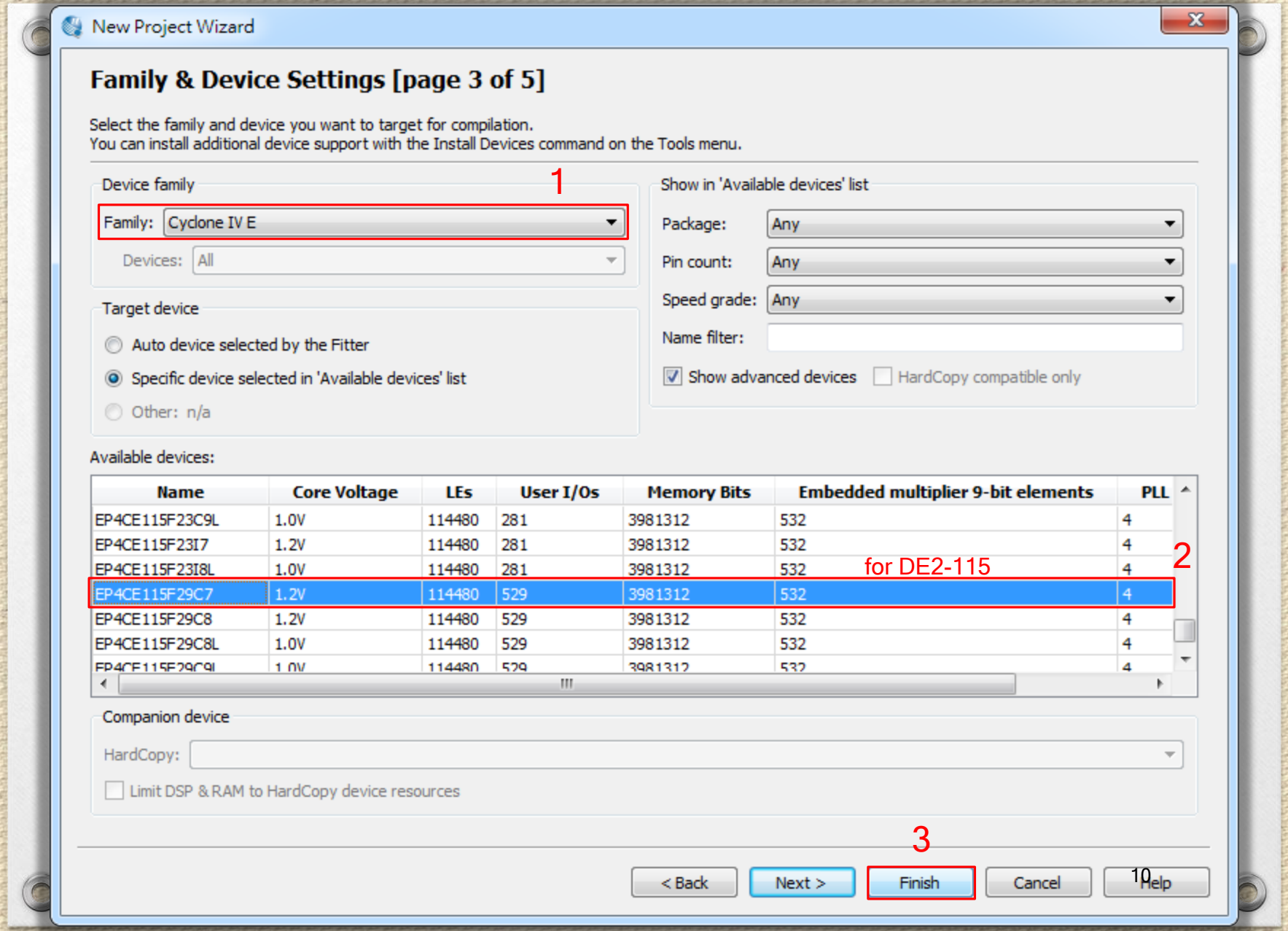
- The example NIOS II standard hardware system provides the following necessary components:
  - Nios II processor core, that's where the software will be executed.
  - On-chip memory to store and run the software.
  - JTAG link for communication between the host computer and target.
  - Hardware (typically using a USB-Blaster cable).
  - LED peripheral I/O (PIO), be used as indicators.

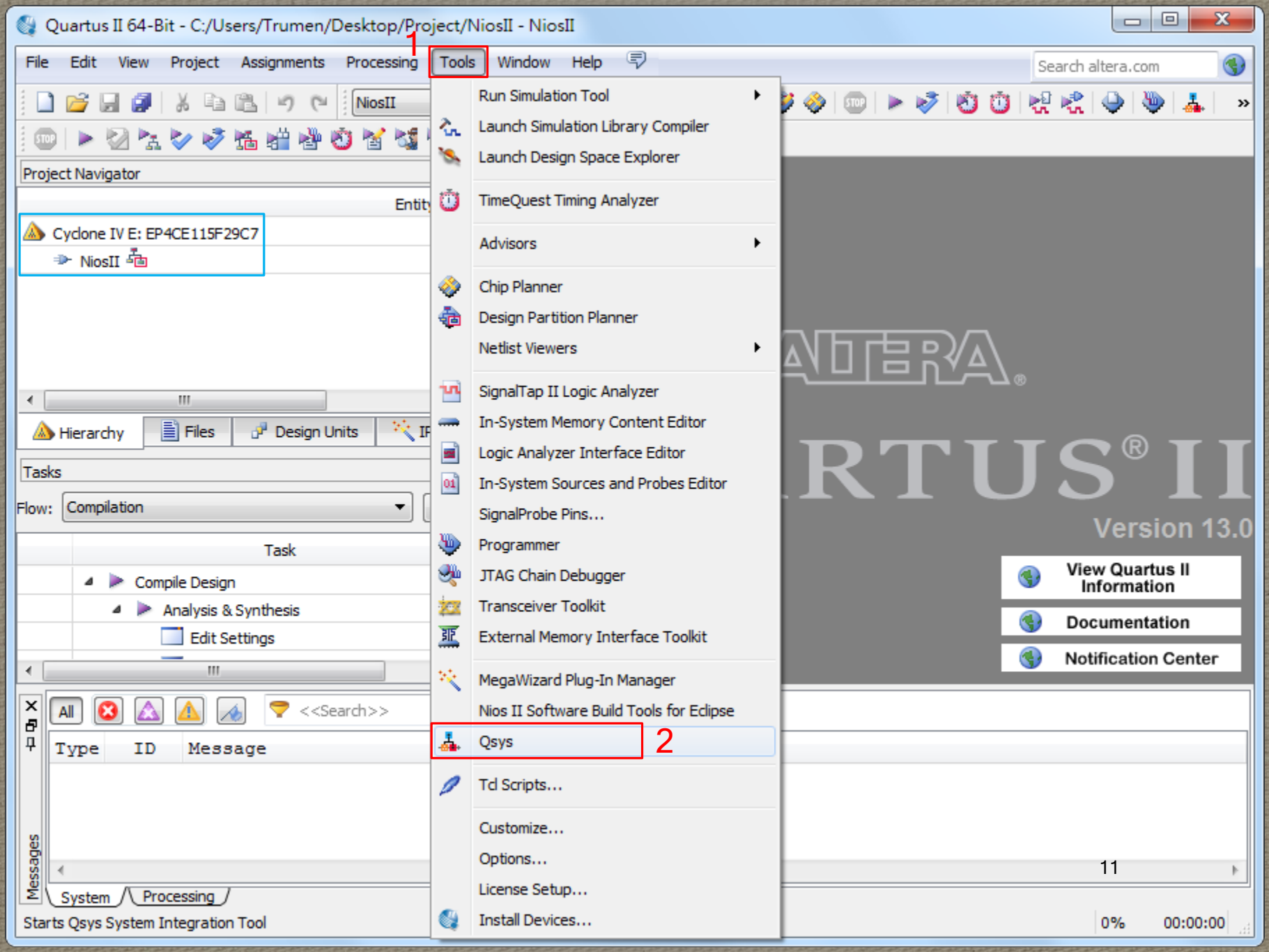
Creation of Hardware Design

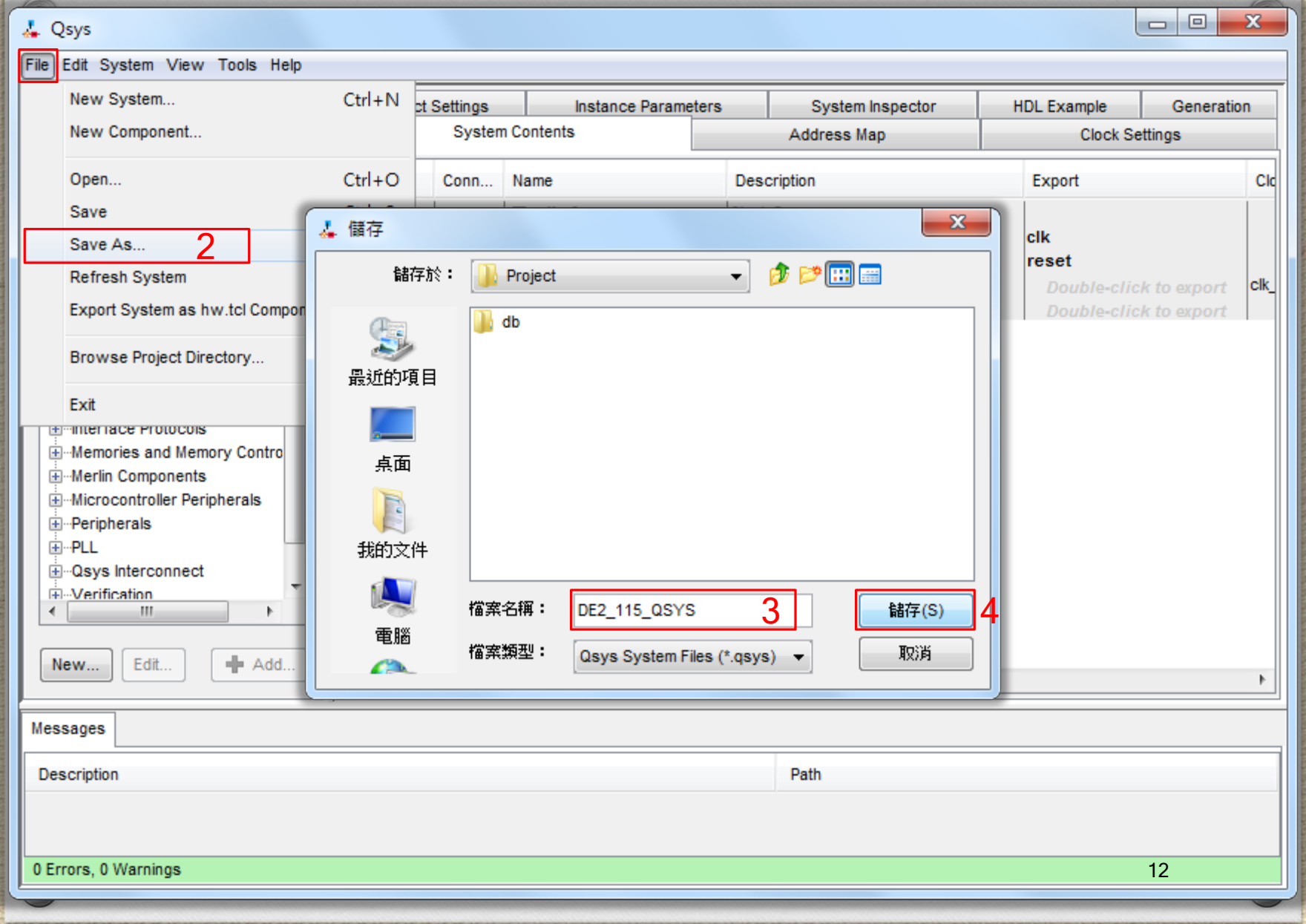


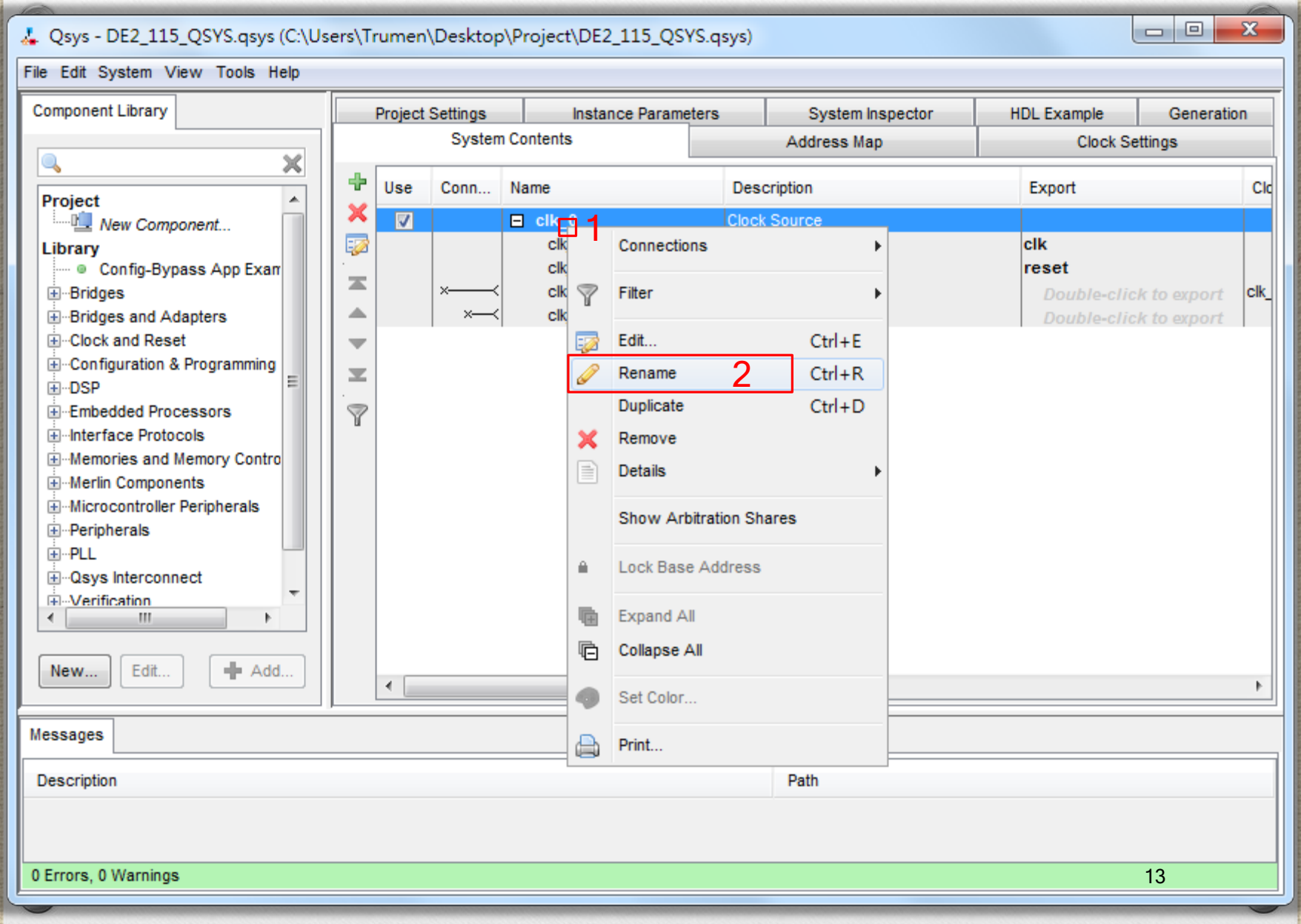

New Project Wizard
Directory, Name, Top-Level Entity [page 1 of 5]
What is the working directory for this project?
1
C:/Users/Trumen/Desktop/Project
...
What is the name of this project?
2
NiosII
same as (top-level) file name
...
What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.
NiosII
...
Use Existing Project Settings...
3
< Back
Next >
Finish
Cancel
Help

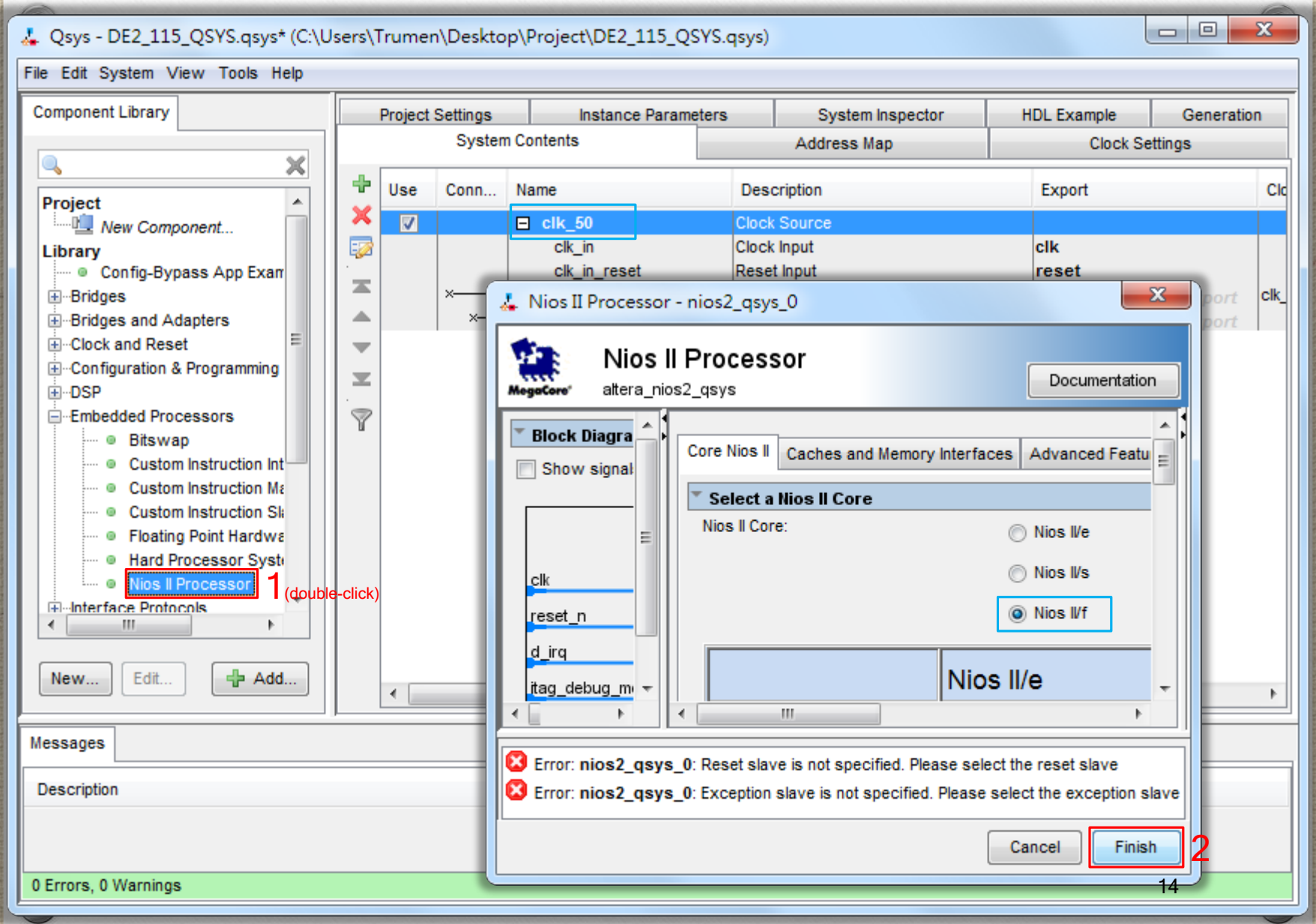

New Project Wizard
Add Files [page 2 of 5]
Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.
Note: you can always add design files to the project later.
File name:
...
Add
Add All
Remove
Up
Down
Properties
File Name
Type
Library
Design Entry/Synthesis Tool
HDL Version
Specify the path names of any non-default libraries.
User Libraries...
1
< Back
Next >
Finish
Cancel
Help


New Project Wizard
Family & Device Settings [page 3 of 5]
Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.
1
Device family
Family: Cyclone IV E
Devices: All
Target device
Auto device selected by the Fitter
Specific device selected in 'Available devices' list
Other: n/a
Show in 'Available devices' list
Package: Any
Pin count: Any
Speed grade: Any
Name filter:
Show advanced devices
HardCopy compatible only
Available devices:
Name | Core Voltage | LEs | User I/Os | Memory Bits | Embedded multiplier 9-bit elements | PLL
EP4CE115F23C9L | 1.0V | 114480 | 281 | 3981312 | 532 | 4
EP4CE115F23I7 | 1.2V | 114480 | 281 | 3981312 | 532 | 4
EP4CE115F23I8L | 1.0V | 114480 | 281 | 3981312 | 532 | 4
EP4CE115F29C7 | 1.2V | 114480 | 529 | 3981312 | 532 | 4
EP4CE115F29C8 | 1.2V | 114480 | 529 | 3981312 | 532 | 4
EP4CE115F29C8L | 1.0V | 114480 | 529 | 3981312 | 532 | 4
for DE2-115
2
Companion device
HardCopy:
Limit DSP & RAM to HardCopy device resources
3
< Back
Next >
Finish
Cancel
Help


Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
File
Edit
View
Project
Assignments
Processing
Tools
Window
Help
1
Search altera.com
NiosII
Project Navigator
Cyclone IV E: EP4CE115F29C7
NiosII
Hierarchy
Files
Design Units
Tasks
Flow:
Compilation
Task
Compile Design
Analysis & Synthesis
Edit Settings
Run Simulation Tool
Launch Simulation Library Compiler
Launch Design Space Explorer
TimeQuest Timing Analyzer
Advisors
Chip Planner
Design Partition Planner
Netlist Viewers
SignalTap II Logic Analyzer
In-System Memory Content Editor
Logic Analyzer Interface Editor
In-System Sources and Probes Editor
SignalProbe Pins...
Programmer
JTAG Chain Debugger
Transceiver Toolkit
External Memory Interface Toolkit
MegaWizard Plug-In Manager
Nios II Software Build Tools for Eclipse
Qsys
2
Tcl Scripts...
Customize...
Options...
License Setup...
Install Devices...
ALTERA
RTUS® II
Version 13.0
View Quartus II Information
Documentation
Notification Center
All
<<Search>>
Type
ID
Message
Messages
System
Processing
11
Starts Qsys System Integration Tool
0%
00:00:00


Qsys
1
File
Edit
System
View
Tools
Help
New System... Ctrl+N
New Component...
Open... Ctrl+O
Save
Save As...
2
Refresh System
Export System as hw.tcl Compor
Browse Project Directory...
Exit
Instance Parameters
System Inspector
HDL Example
Generation
System Contents
Address Map
Clock Settings
Conn...
Name
Description
Export
clk
reset
Double-click to export
Double-click to export
Memories and Memory Contro
Merlin Components
Microcontroller Peripherals
Peripherals
PLL
Qsys Interconnect
Verification
New...
Edit...
Add...
儲存
儲存於：
Project
db
最近的項目
桌面
我的文件
電腦
檔案名稱：
DE2_115_QSYS
3
儲存(S)
4
檔案類型：
Qsys System Files (*.qsys)
取消
Messages
Description
Path
0 Errors, 0 Warnings
12


Qsys - DE2_115_QSYS.qsys (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
File Edit System View Tools Help
Component Library
Project
New Component...
Library
Config-Bypass App Exan
Bridges
Bridges and Adapters
Clock and Reset
Configuration & Programming
DSP
Embedded Processors
Interface Protocols
Memories and Memory Contro
Merlin Components
Microcontroller Peripherals
Peripherals
PLL
Qsys Interconnect
Verification
New...
Edit...
Add...
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
System Contents
Address Map
Clock Settings
Use
Conn...
Name
Description
Export
Clock Source
clk
reset
Double-click to export
1
Connections
Filter
Edit... Ctrl+E
Rename Ctrl+R
2
Duplicate Ctrl+D
Remove
Details
Show Arbitration Shares
Lock Base Address
Expand All
Collapse All
Set Color...
Print...
Messages
Description
Path
0 Errors, 0 Warnings
13


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
File Edit System View Tools Help
Component Library
Project
New Component...
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Bridges
Bridges and Adapters
Clock and Reset
Configuration & Programming
DSP
Embedded Processors
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1 (double-click)
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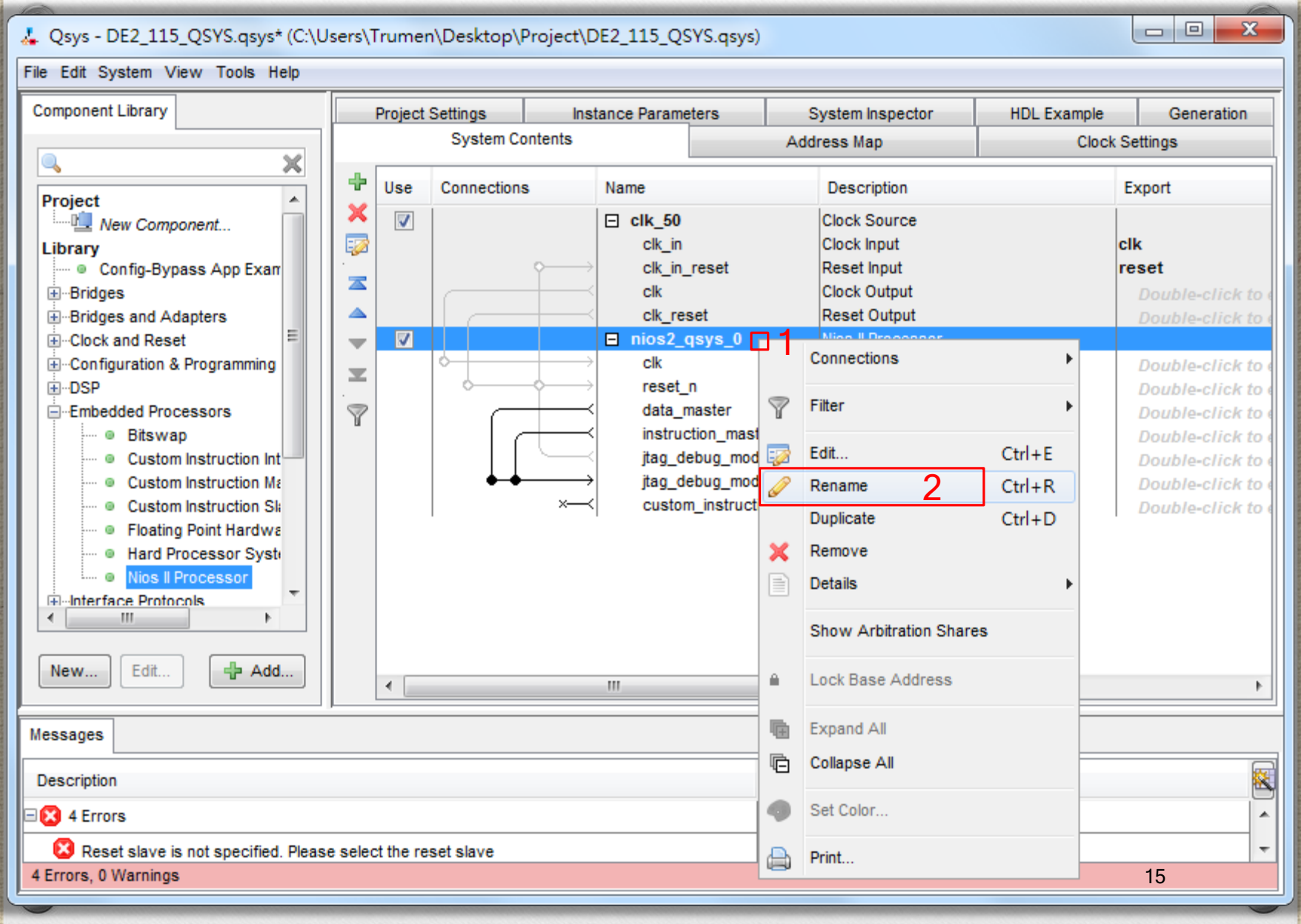
New...
Edit...
Add...
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
System Contents
Address Map
Clock Settings
Use
Conn...
Name
Description
Export
clk_50
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
reset
Nios II Processor - nios2_qsys_0
Nios II Processor
altera_nios2_qsys
Documentation
Block Diagra
Show signal
clk
reset_n
d_irq
jtag_debug_m
Core Nios II
Caches and Memory Interfaces
Advanced Featu
Select a Nios II Core
Nios II Core:
Nios II/e
Nios II/s
Nios II/f
Nios II/e
Error: nios2_qsys_0: Reset slave is not specified. Please select the reset slave
Error: nios2_qsys_0: Exception slave is not specified. Please select the exception slave
Cancel
Finish
2
Messages
Description
0 Errors, 0 Warnings


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
File Edit System View Tools Help
Component Library
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Bridges and Adapters
Clock and Reset
Configuration & Programming
DSP
Embedded Processors
Bitswap
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Project Settings
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System Inspector
HDL Example
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System Contents
Address Map
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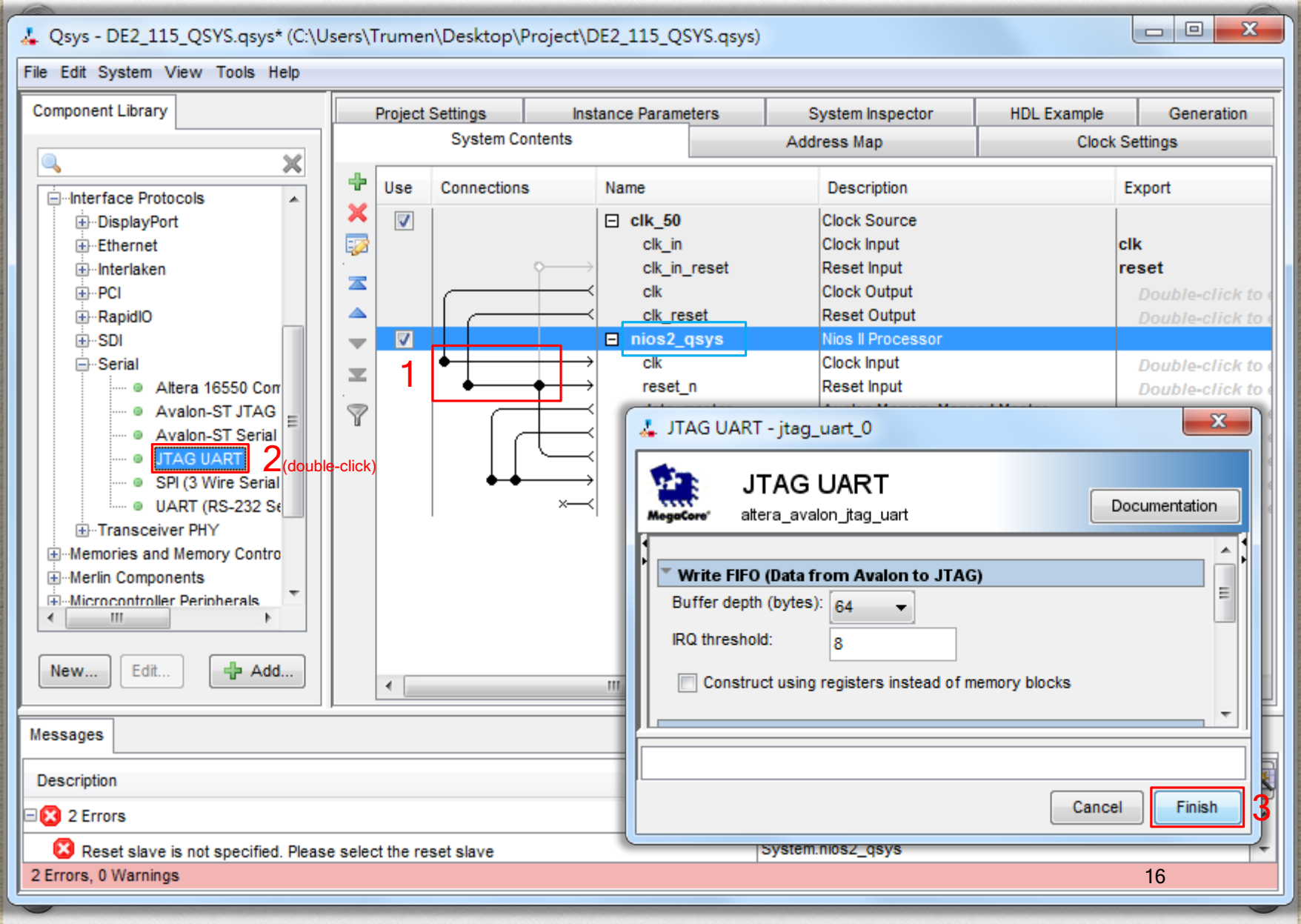
Description
Export
clk_50
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
reset
clk
Clock Output
clk_reset
Reset Output
nios2_qsys_0
1
clk
reset_n
data_master
instruction_mast
jtag_debug_mod
jtag_debug_mod
custom_instruct
Double-click to
Connections
Filter
Edit... Ctrl+E
Rename 2 Ctrl+R
Duplicate Ctrl+D
Remove
Details
Show Arbitration Shares
Lock Base Address
Expand All
Collapse All
Set Color...
Print...
Messages
Description
4 Errors
Reset slave is not specified. Please select the reset slave
4 Errors, 0 Warnings


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
File Edit System View Tools Help
Component Library
Interface Protocols
DisplayPort
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RapidIO
SDI
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Altera 16550 Con
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Avalon-ST Serial
JTAG UART
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Memories and Memory Contro
Merlin Components
Microcontroller Peripherals
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Add...
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System Inspector
HDL Example
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System Contents
Address Map
Clock Settings
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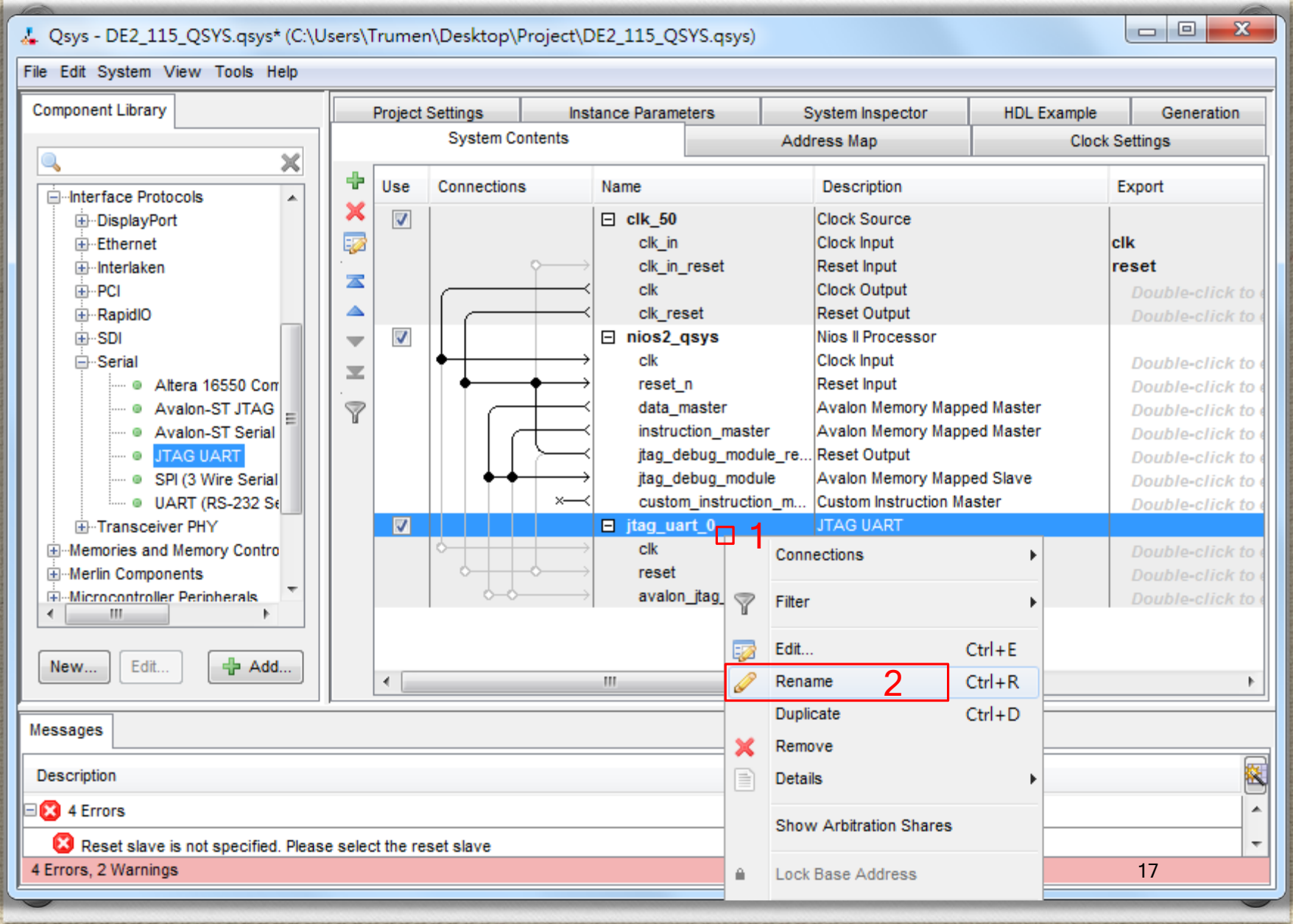
clk_50
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
reset
clk
Clock Output
clk_reset
Reset Output
nios2_qsys
Nios II Processor
clk
Clock Input
reset_n
Reset Input
1
2 (double-click)
JTAG UART - jtag_uart_0
JTAG UART
altera_avalon_jtag_uart
MegaCore
Documentation
Write FIFO (Data from Avalon to JTAG)
Buffer depth (bytes):
64
IRQ threshold:
8
Construct using registers instead of memory blocks
Cancel
Finish
3
Messages
Description
2 Errors
Reset slave is not specified. Please select the reset slave
System.nios2_qsys
2 Errors, 0 Warnings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Component Library
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DisplayPort
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Avalon-ST Serial
JTAG UART
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HDL Example
Generation
System Contents
Address Map
Clock Settings
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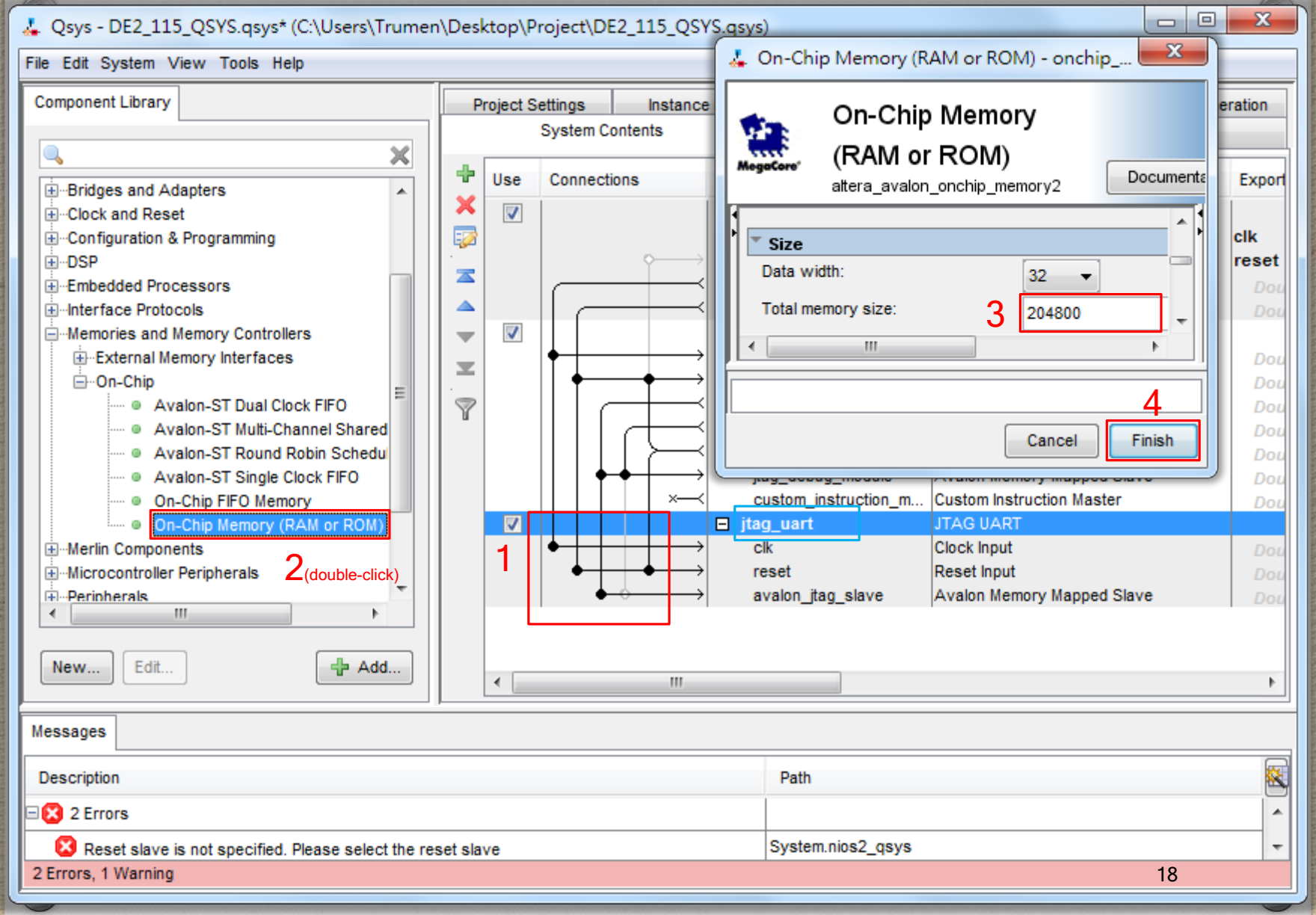
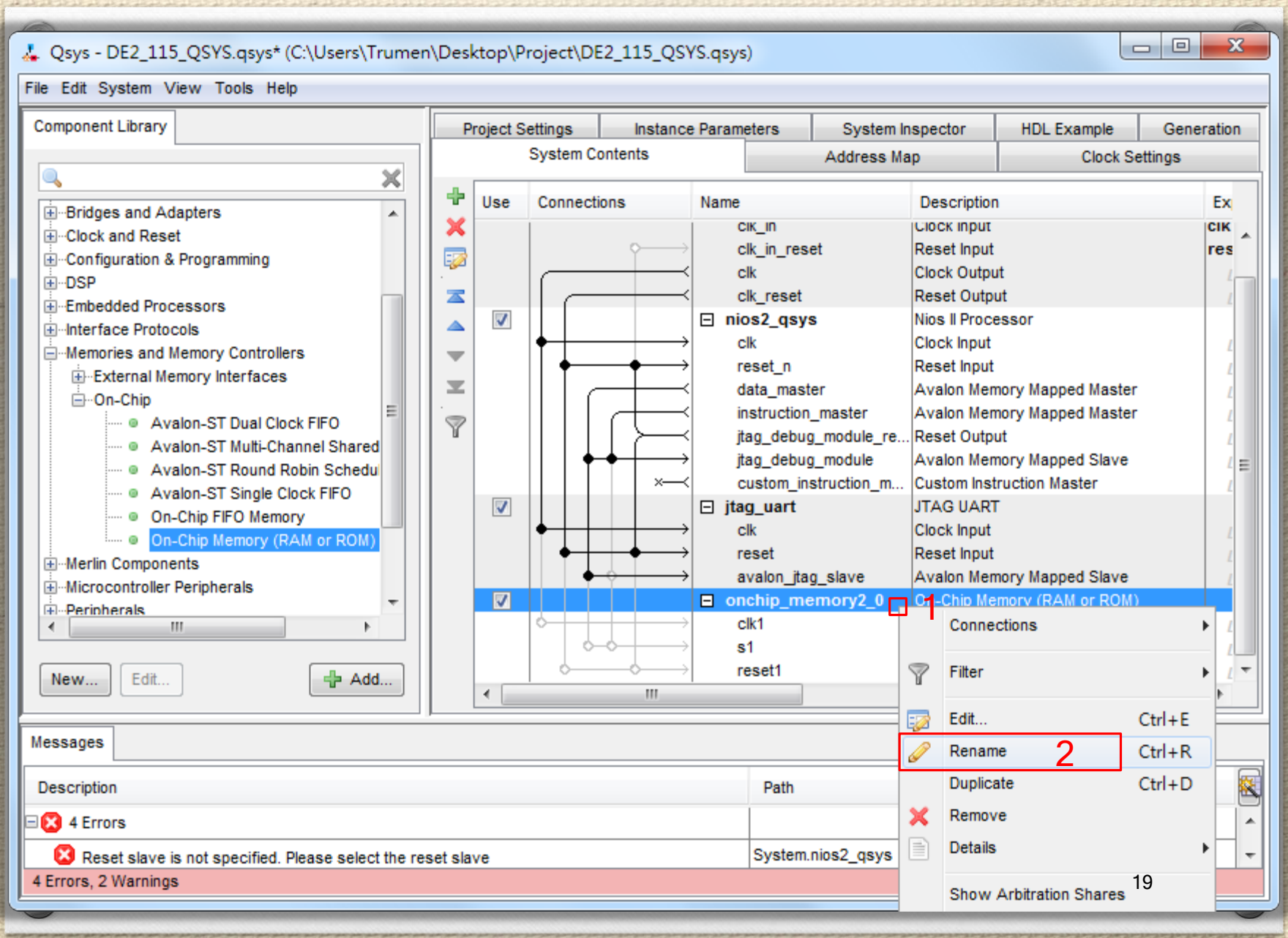
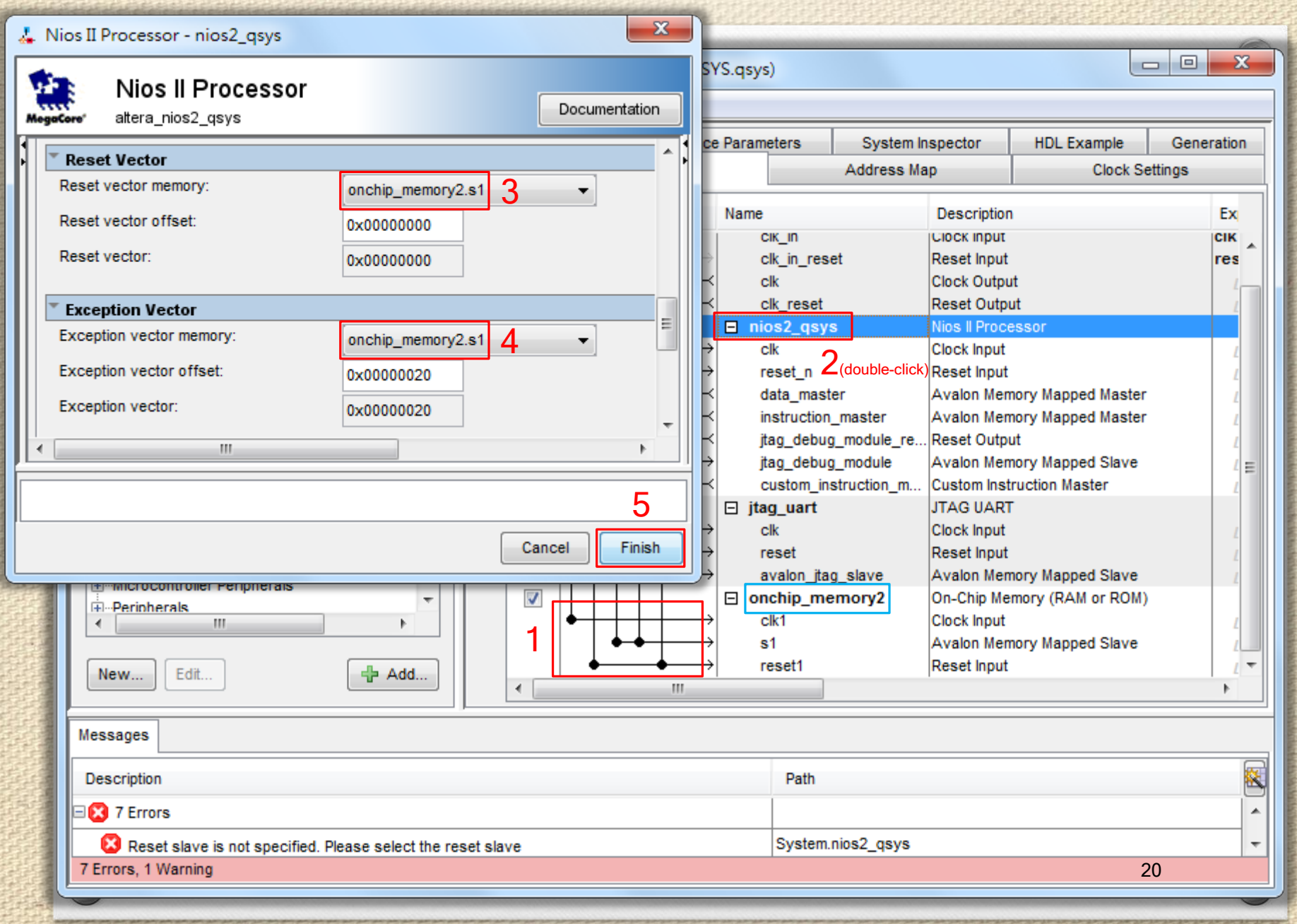
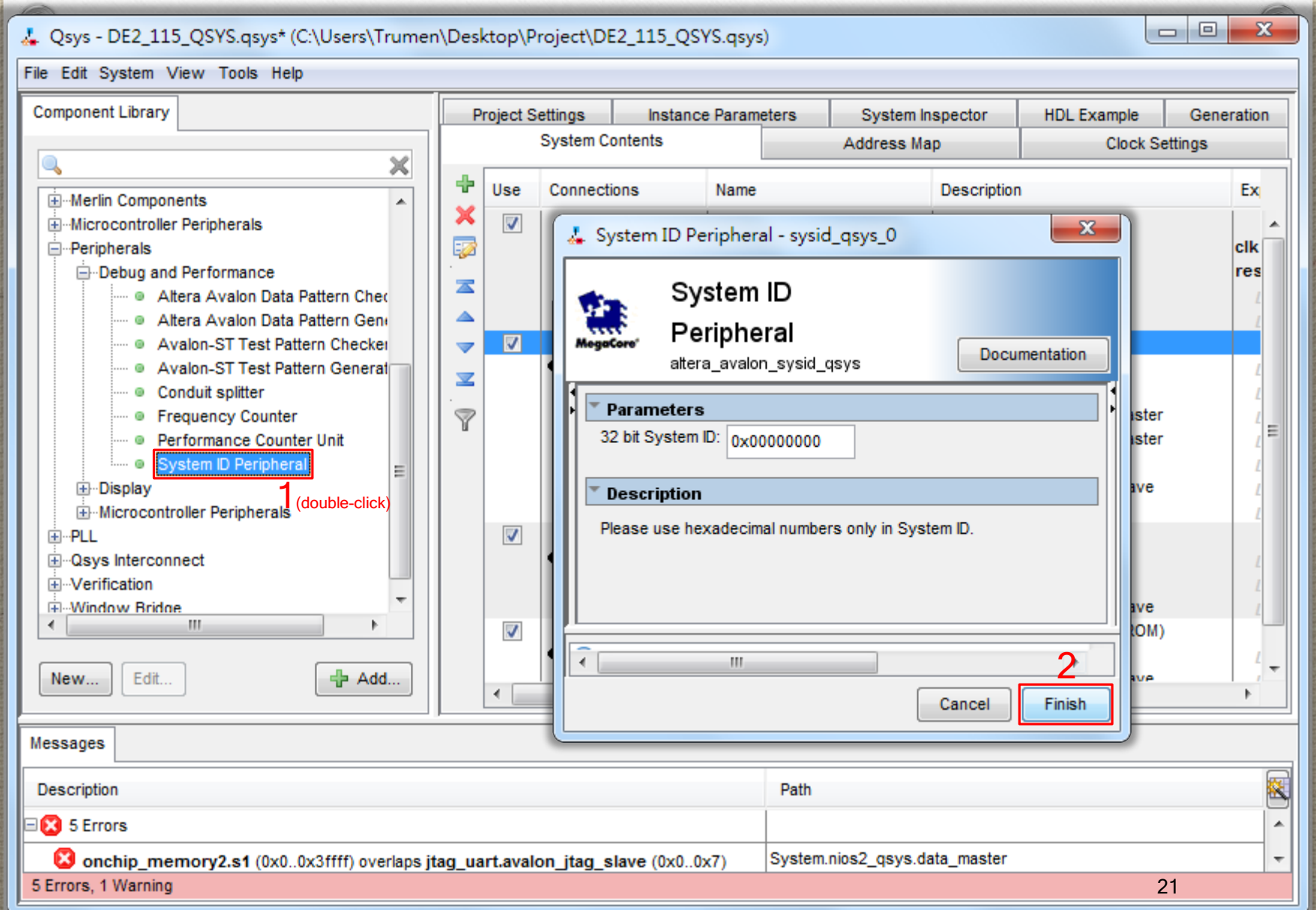
clk_50
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
reset
clk
Clock Output
clk_reset
Reset Output
nios2_qsys
Nios II Processor
clk
Clock Input
reset_n
Reset Input
data_master
Avalon Memory Mapped Master
instruction_master
Avalon Memory Mapped Master
jtag_debug_module_re...
Reset Output
jtag_debug_module
Avalon Memory Mapped Slave
custom_instruction_m...
Custom Instruction Master
jtag_uart_0
JTAG UART
clk
reset
avalon_jtag_
1
Connections
Filter
Edit...
Ctrl+E
Rename
Ctrl+R
2
Duplicate
Ctrl+D
Remove
Details
Show Arbitration Shares
Lock Base Address
Messages
Description
4 Errors
Reset slave is not specified. Please select the reset slave
4 Errors, 2 Warnings
17


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
File Edit System View Tools Help
Component Library
Bridges and Adapters
Clock and Reset
Configuration & Programming
DSP
Embedded Processors
Interface Protocols
Memories and Memory Controllers
External Memory Interfaces
On-Chip
Avalon-ST Dual Clock FIFO
Avalon-ST Multi-Channel Shared
Avalon-ST Round Robin Schedu
Avalon-ST Single Clock FIFO
On-Chip FIFO Memory
On-Chip Memory (RAM or ROM)
Merlin Components
Microcontroller Peripherals
Peripherals
2 (double-click)
New...
Edit...
Add...
Project Settings
Instance
System Contents
Use
Connections
1
custom_instruction_m...
Custom Instruction Master
jtag_uart
JTAG UART
clk
Clock Input
reset
Reset Input
avalon_jtag_slave
Avalon Memory Mapped Slave
Export
clk
reset
On-Chip Memory (RAM or ROM) - onchip_...
On-Chip Memory
(RAM or ROM)
altera_avalon_onchip_memory2
Documenta
Size
Data width:
32
Total memory size:
3
204800
4
Cancel
Finish
Messages
Description
Path
2 Errors
Reset slave is not specified. Please select the reset slave
System.nios2_qsys
2 Errors, 1 Warning
18


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
File Edit System View Tools Help
Component Library
Bridges and Adapters
Clock and Reset
Configuration & Programming
DSP
Embedded Processors
Interface Protocols
Memories and Memory Controllers
External Memory Interfaces
On-Chip
Avalon-ST Dual Clock FIFO
Avalon-ST Multi-Channel Shared
Avalon-ST Round Robin Schedu
Avalon-ST Single Clock FIFO
On-Chip FIFO Memory
On-Chip Memory (RAM or ROM)
Merlin Components
Microcontroller Peripherals
Peripherals
New...
Edit...
Add...
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
System Contents
Address Map
Clock Settings
Use
Connections
Name
Description
clk_in_reset
Reset Input
clk
Clock Output
clk_reset
Reset Output
nios2_qsys
Nios II Processor
clk
Clock Input
reset_n
Reset Input
data_master
Avalon Memory Mapped Master
instruction_master
Avalon Memory Mapped Master
jtag_debug_module_re...
Reset Output
jtag_debug_module
Avalon Memory Mapped Slave
custom_instruction_m...
Custom Instruction Master
jtag_uart
JTAG UART
clk
Clock Input
reset
Reset Input
avalon_jtag_slave
Avalon Memory Mapped Slave
onchip_memory2_0
clk1
s1
reset1
1
Connections
Filter
Edit...
Ctrl+E
Rename
2
Ctrl+R
Duplicate
Ctrl+D
Remove
Details
Show Arbitration Shares
Messages
Description
Path
4 Errors
Reset slave is not specified. Please select the reset slave
System.nios2_qsys
4 Errors, 2 Warnings
19


Nios II Processor - nios2_qsys
Nios II Processor
altera_nios2_qsys
Documentation
Reset Vector
Reset vector memory:
onchip_memory2.s1
3
Reset vector offset:
0x00000000
Reset vector:
0x00000000
Exception Vector
Exception vector memory:
onchip_memory2.s1
4
Exception vector offset:
0x00000020
Exception vector:
0x00000020
5
Cancel
Finish
SYS.qsys)
ce Parameters
System Inspector
HDL Example
Generation
Address Map
Clock Settings
Name
Description
clk_in_reset
Reset Input
clk
Clock Output
clk_reset
Reset Output
nios2_qsys
Nios II Processor
clk
Clock Input
reset_n
2 (double-click)
Reset Input
data_master
Avalon Memory Mapped Master
instruction_master
Avalon Memory Mapped Master
jtag_debug_module_re...
Reset Output
jtag_debug_module
Avalon Memory Mapped Slave
custom_instruction_m...
Custom Instruction Master
jtag_uart
JTAG UART
clk
Clock Input
reset
Reset Input
avalon_jtag_slave
Avalon Memory Mapped Slave
onchip_memory2
On-Chip Memory (RAM or ROM)
clk1
Clock Input
s1
Avalon Memory Mapped Slave
reset1
Reset Input
1
Peripherals
New...
Edit...
Add...
Messages
Description
Path
7 Errors
Reset slave is not specified. Please select the reset slave
System.nios2_qsys
7 Errors, 1 Warning
20


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
File Edit System View Tools Help
Component Library
Merlin Components
Microcontroller Peripherals
Peripherals
Debug and Performance
Altera Avalon Data Pattern Chec
Altera Avalon Data Pattern Gen
Avalon-ST Test Pattern Checke
Avalon-ST Test Pattern Generat
Conduit splitter
Frequency Counter
Performance Counter Unit
System ID Peripheral
1 (double-click)
Display
Microcontroller Peripherals
PLL
Qsys Interconnect
Verification
Window Bridge
New...
Edit...
Add...
Project Settings
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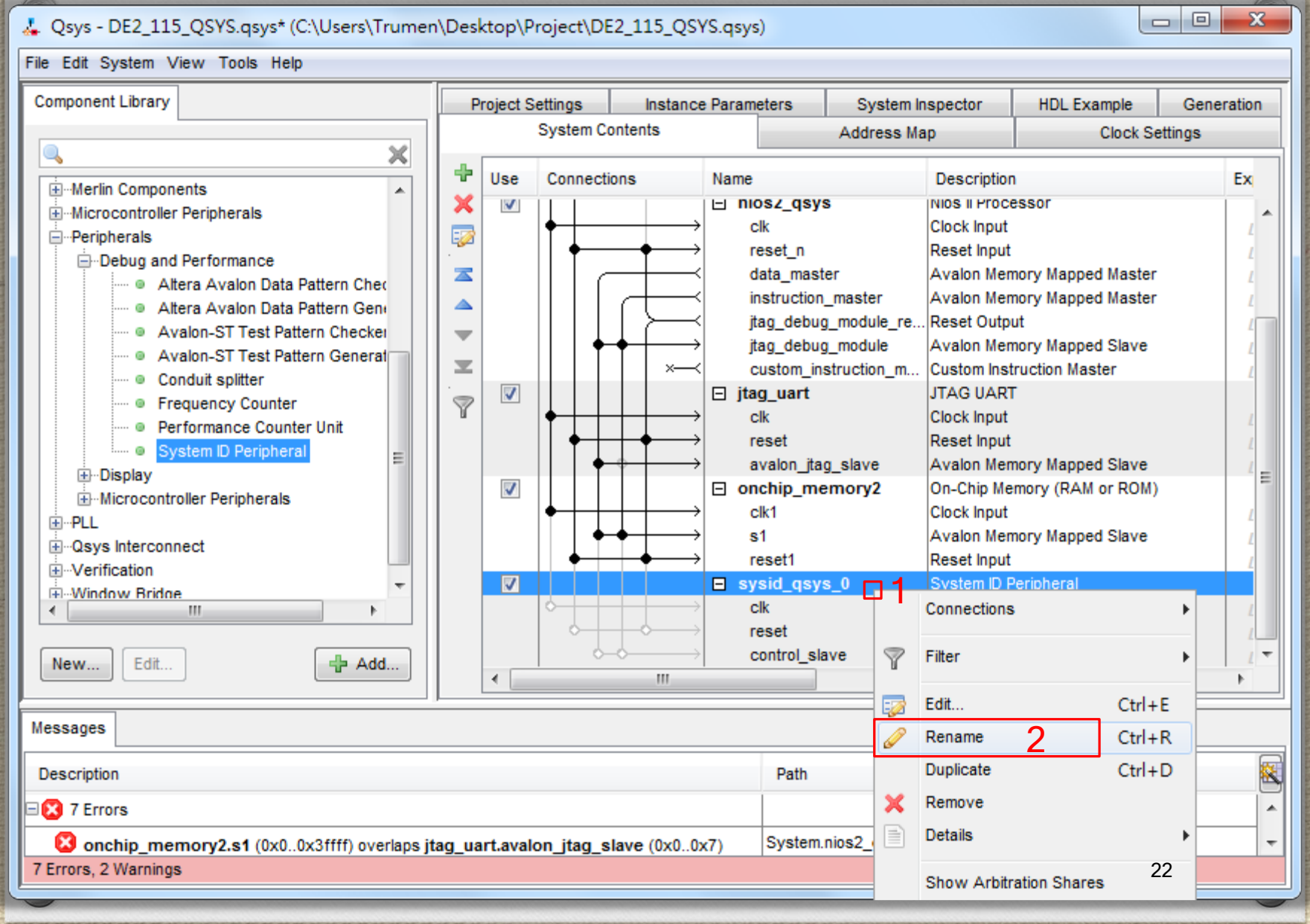
Address Map
Clock Settings
Use
Connections
Name
Description
System ID Peripheral - sysid_qsys_0
System ID Peripheral
altera_avalon_sysid_qsys
Documentation
Parameters
32 bit System ID:
0x00000000
Description
Please use hexadecimal numbers only in System ID.
2
Cancel
Finish
Messages
Description
Path
5 Errors
onchip_memory2.s1 (0x0..0x3ffff) overlaps jtag_uart.avalon_jtag_slave (0x0..0x7)
System.nios2_qsys.data_master
5 Errors, 1 Warning
21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Component Library
Merlin Components
Microcontroller Peripherals
Peripherals
Debug and Performance
Altera Avalon Data Pattern Chec
Altera Avalon Data Pattern Gen
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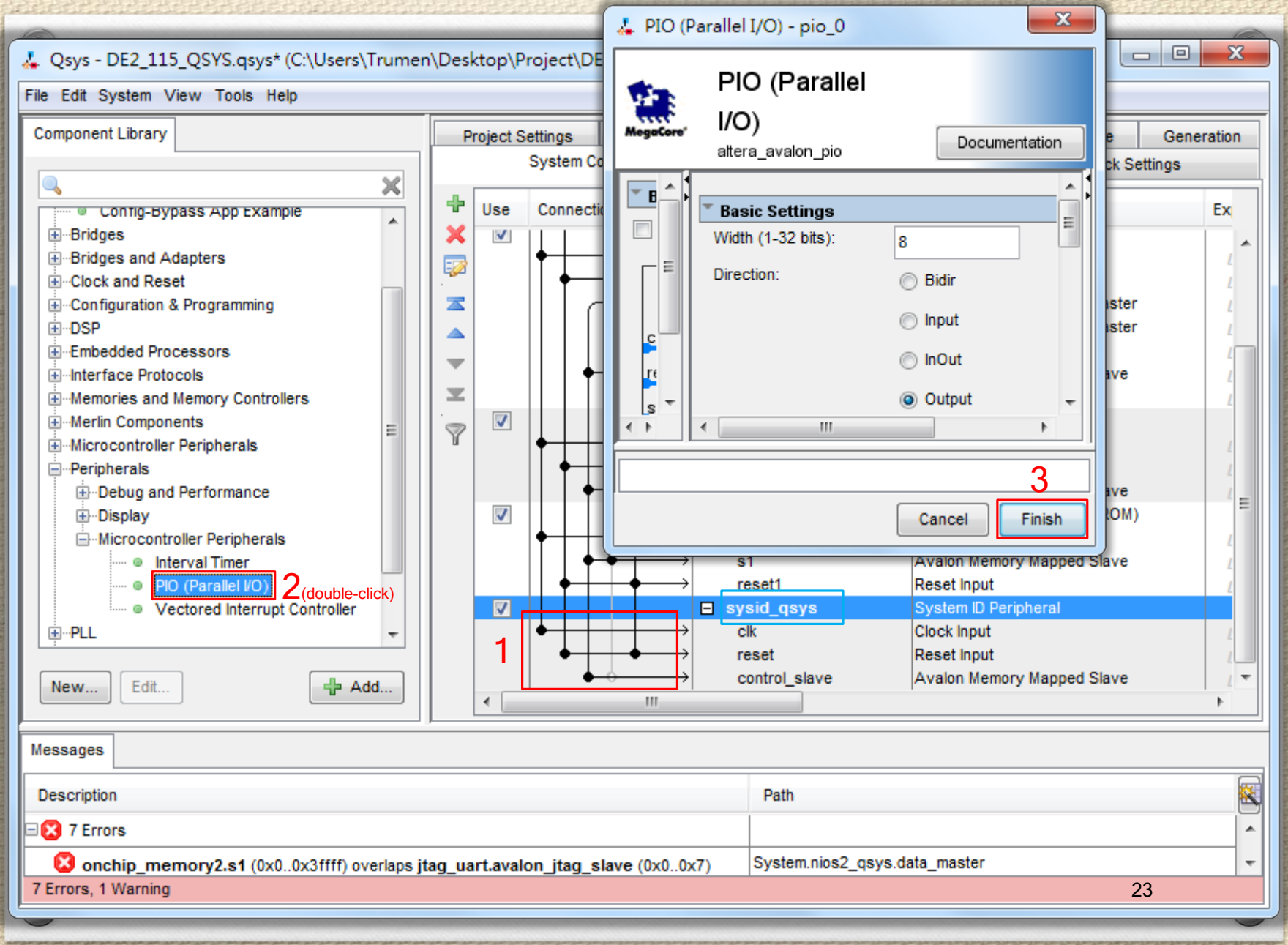
Avalon-ST Test Pattern Generat
Conduit splitter
Frequency Counter
Performance Counter Unit
System ID Peripheral
Display
Microcontroller Peripherals
PLL
Qsys Interconnect
Verification
Window Bridge
New...
Edit...
Add...
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
System Contents
Address Map
Clock Settings
Use
Connections
Name
Description
nios2_qsys
Nios II Processor
clk
Clock Input
reset_n
Reset Input
data_master
Avalon Memory Mapped Master
instruction_master
Avalon Memory Mapped Master
jtag_debug_module_re...
Reset Output
jtag_debug_module
Avalon Memory Mapped Slave
custom_instruction_m...
Custom Instruction Master
jtag_uart
JTAG UART
clk
Clock Input
reset
Reset Input
avalon_jtag_slave
Avalon Memory Mapped Slave
onchip_memory2
On-Chip Memory (RAM or ROM)
clk1
Clock Input
s1
Avalon Memory Mapped Slave
reset1
Reset Input
sysid_qsys_0
System ID Peripheral
clk
reset
control_slave
1
Connections
Filter
Edit... Ctrl+E
Rename Ctrl+R
2
Duplicate Ctrl+D
Remove
Details
Show Arbitration Shares
Messages
Description
Path
7 Errors
onchip_memory2.s1 (0x0..0x3ffff) overlaps jtag_uart.avalon_jtag_slave (0x0..0x7)
System.nios2_
7 Errors, 2 Warnings
22


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE
File Edit System View Tools Help
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PIO (Parallel I/O)
Vectored Interrupt Controller
PLL
2 (double-click)
New...
Edit...
Add...
Project Settings
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Use
Connecti
s1
Avalon Memory Mapped Slave
reset1
Reset Input
sysid_qsys
System ID Peripheral
clk
Clock Input
reset
Reset Input
control_slave
Avalon Memory Mapped Slave
1
PIO (Parallel I/O) - pio_0
PIO (Parallel I/O)
altera_avalon_pio
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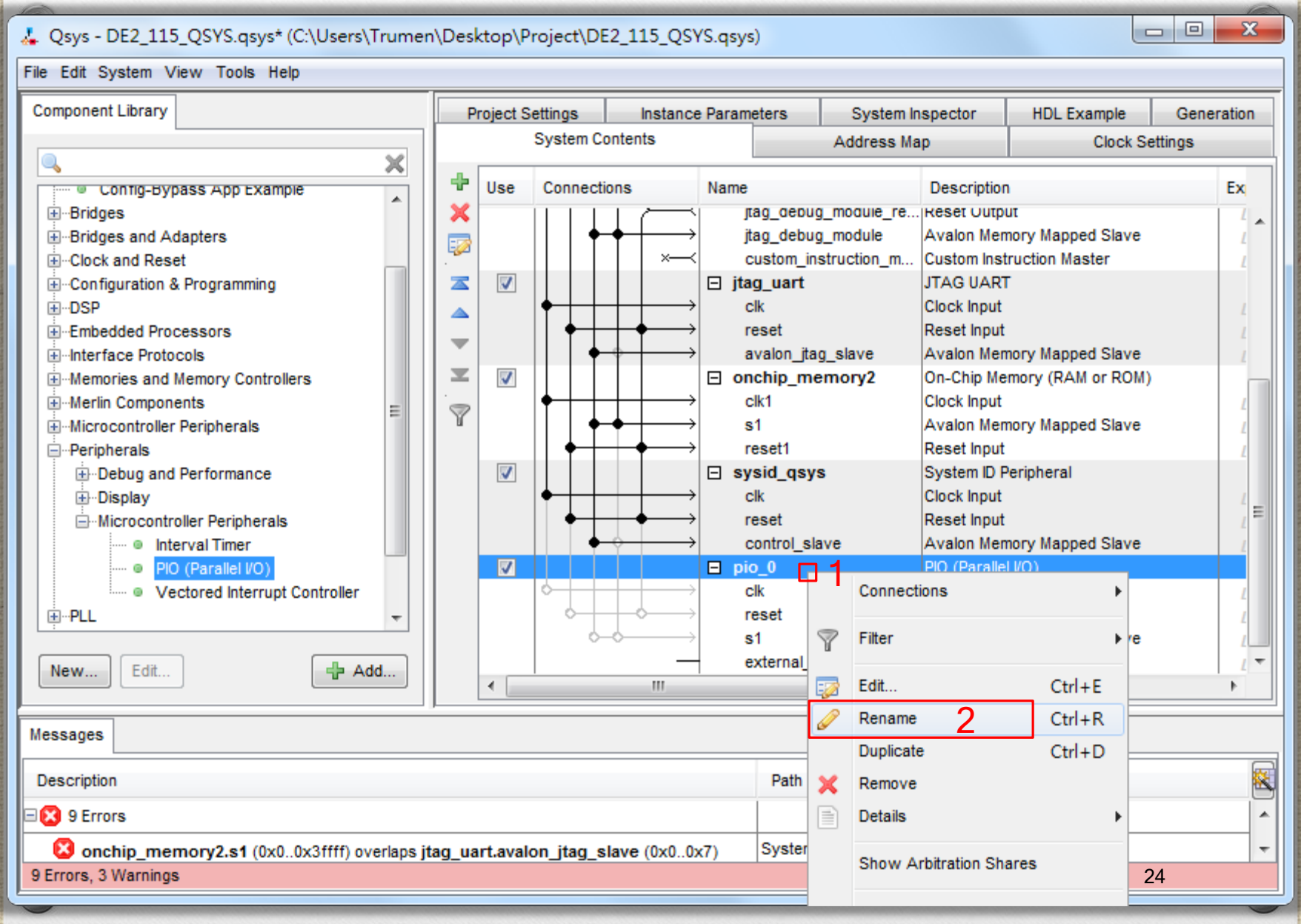
Basic Settings
Width (1-32 bits):
8
Direction:
Bidir
Input
InOut
Output
3
Cancel
Finish
Messages
Description
Path
7 Errors
onchip_memory2.s1 (0x0..0x3fff) overlaps jtag_uart.avalon_jtag_slave (0x0..0x7)
System.nios2_qsys.data_master
7 Errors, 1 Warning
23


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
File Edit System View Tools Help
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Add...
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Description
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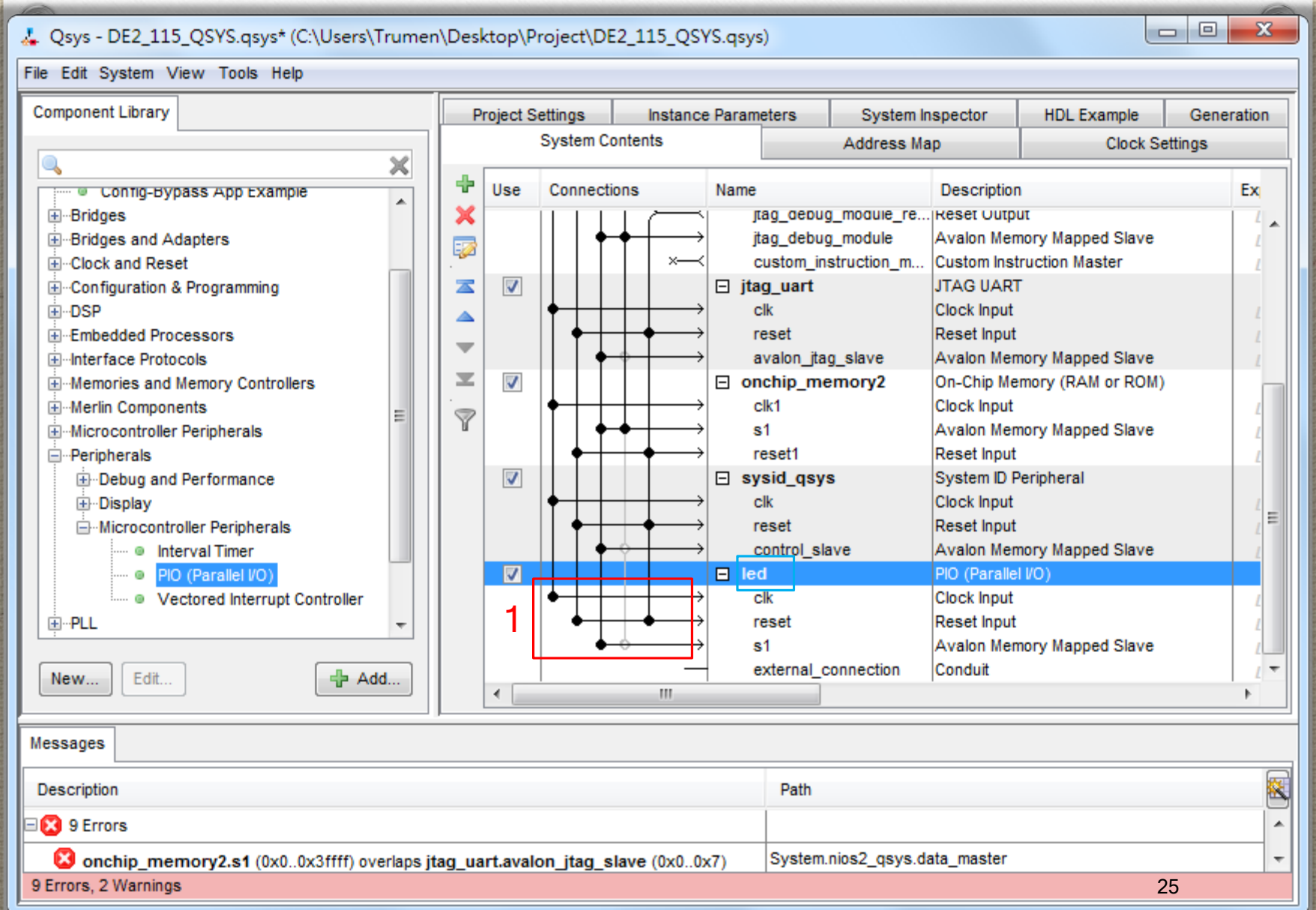
Custom Instruction Master
jtag_uart
JTAG UART
clk
Clock Input
reset
Reset Input
avalon_jtag_slave
Avalon Memory Mapped Slave
onchip_memory2
On-Chip Memory (RAM or ROM)
clk1
Clock Input
s1
Avalon Memory Mapped Slave
reset1
Reset Input
sysid_qsys
System ID Peripheral
clk
Clock Input
reset
Reset Input
control_slave
Avalon Memory Mapped Slave
pio_0
clk
reset
s1
1
Connections
Filter
Edit... Ctrl+E
Rename Ctrl+R
2
Duplicate Ctrl+D
Remove
Details
Show Arbitration Shares
Messages
Description
Path
9 Errors
onchip_memory2.s1 (0x0..0x3ffff) overlaps jtag_uart.avalon_jtag_slave (0x0..0x7)
9 Errors, 3 Warnings
24


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
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New...
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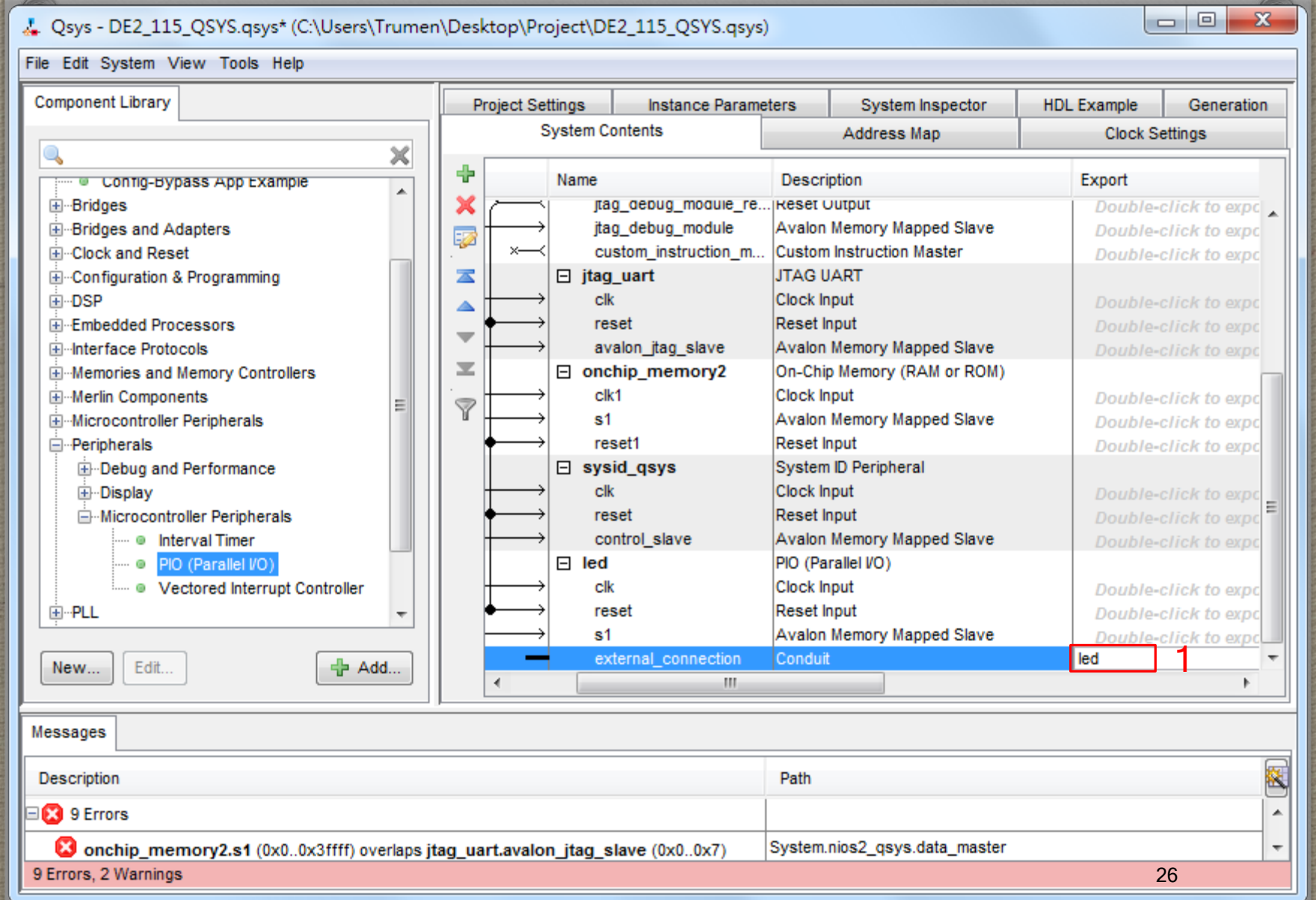
Description
jtag_debug_module
Avalon Memory Mapped Slave
custom_instruction_m...
Custom Instruction Master
jtag_uart
JTAG UART
clk
Clock Input
reset
Reset Input
avalon_jtag_slave
Avalon Memory Mapped Slave
onchip_memory2
On-Chip Memory (RAM or ROM)
clk1
Clock Input
s1
Avalon Memory Mapped Slave
reset1
Reset Input
sysid_qsys
System ID Peripheral
clk
Clock Input
reset
Reset Input
control_slave
Avalon Memory Mapped Slave
led
PIO (Parallel I/O)
clk
Clock Input
reset
Reset Input
s1
Avalon Memory Mapped Slave
external_connection
Conduit
1
Messages
Description
Path
9 Errors
onchip_memory2.s1 (0x0..0x3fff) overlaps jtag_uart.avalon_jtag_slave (0x0..0x7)
System.nios2_qsys.data_master
9 Errors, 2 Warnings
25


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
File Edit System View Tools Help
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Custom Instruction Master
jtag_uart
JTAG UART
clk
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reset
Reset Input
avalon_jtag_slave
Avalon Memory Mapped Slave
onchip_memory2
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clk1
Clock Input
s1
Avalon Memory Mapped Slave
reset1
Reset Input
sysid_qsys
System ID Peripheral
clk
Clock Input
reset
Reset Input
control_slave
Avalon Memory Mapped Slave
led
PIO (Parallel I/O)
clk
Clock Input
reset
Reset Input
s1
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led
1
Messages
Description
Path
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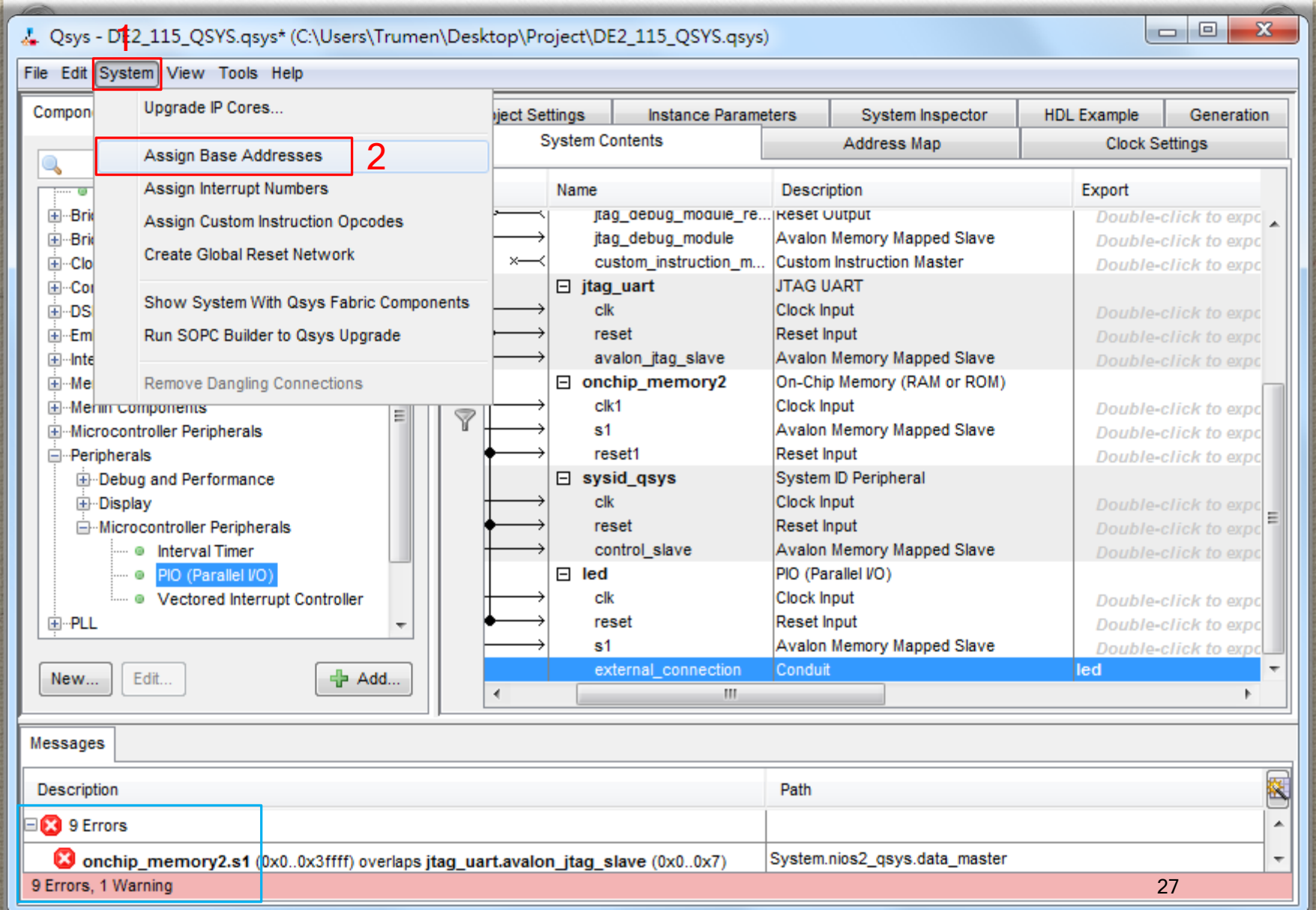
onchip_memory2.s1 (0x0..0x3ffff) overlaps jtag_uart.avalon_jtag_slave (0x0..0x7)
System.nios2_qsys.data_master
9 Errors, 2 Warnings
26


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
1
File Edit System View Tools Help
Upgrade IP Cores...
Assign Base Addresses
2
Assign Interrupt Numbers
Assign Custom Instruction Opcodes
Create Global Reset Network
Show System With Qsys Fabric Components
Run SOPC Builder to Qsys Upgrade
Remove Dangling Connections
Instance Parameters
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Custom Instruction Master
jtag_uart
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Reset Input
avalon_jtag_slave
Avalon Memory Mapped Slave
onchip_memory2
On-Chip Memory (RAM or ROM)
clk1
Clock Input
s1
Avalon Memory Mapped Slave
reset1
Reset Input
sysid_qsys
System ID Peripheral
clk
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reset
Reset Input
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led
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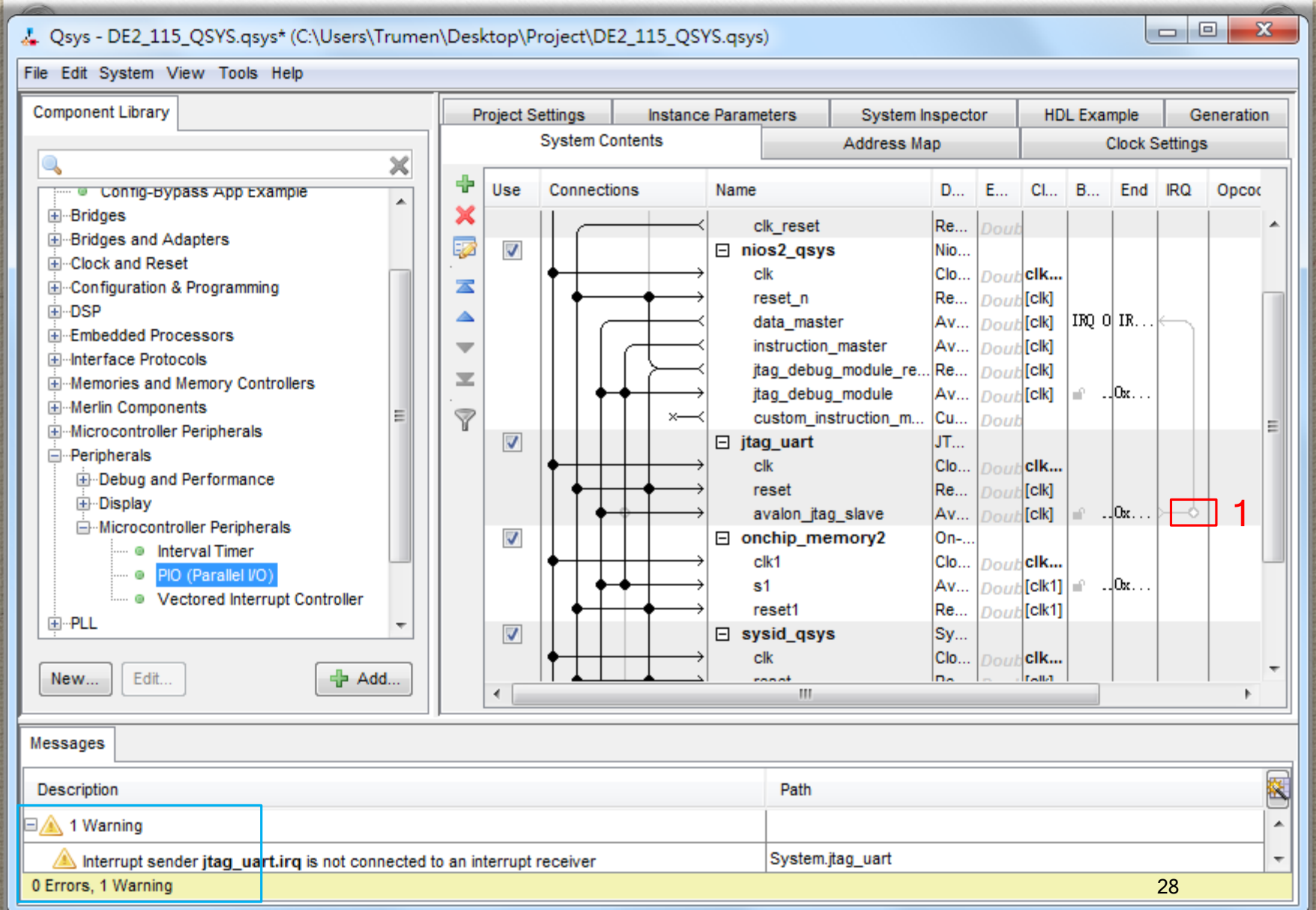
Description
Path
9 Errors
onchip_memory2.s1 (0x0..0x3ffff) overlaps jtag_uart.avalon_jtag_slave (0x0..0x7)
System.nios2_qsys.data_master
9 Errors, 1 Warning


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
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instruction_master
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jtag_debug_module
custom_instruction_m...
jtag_uart
clk
reset
avalon_jtag_slave
onchip_memory2
clk1
s1
reset1
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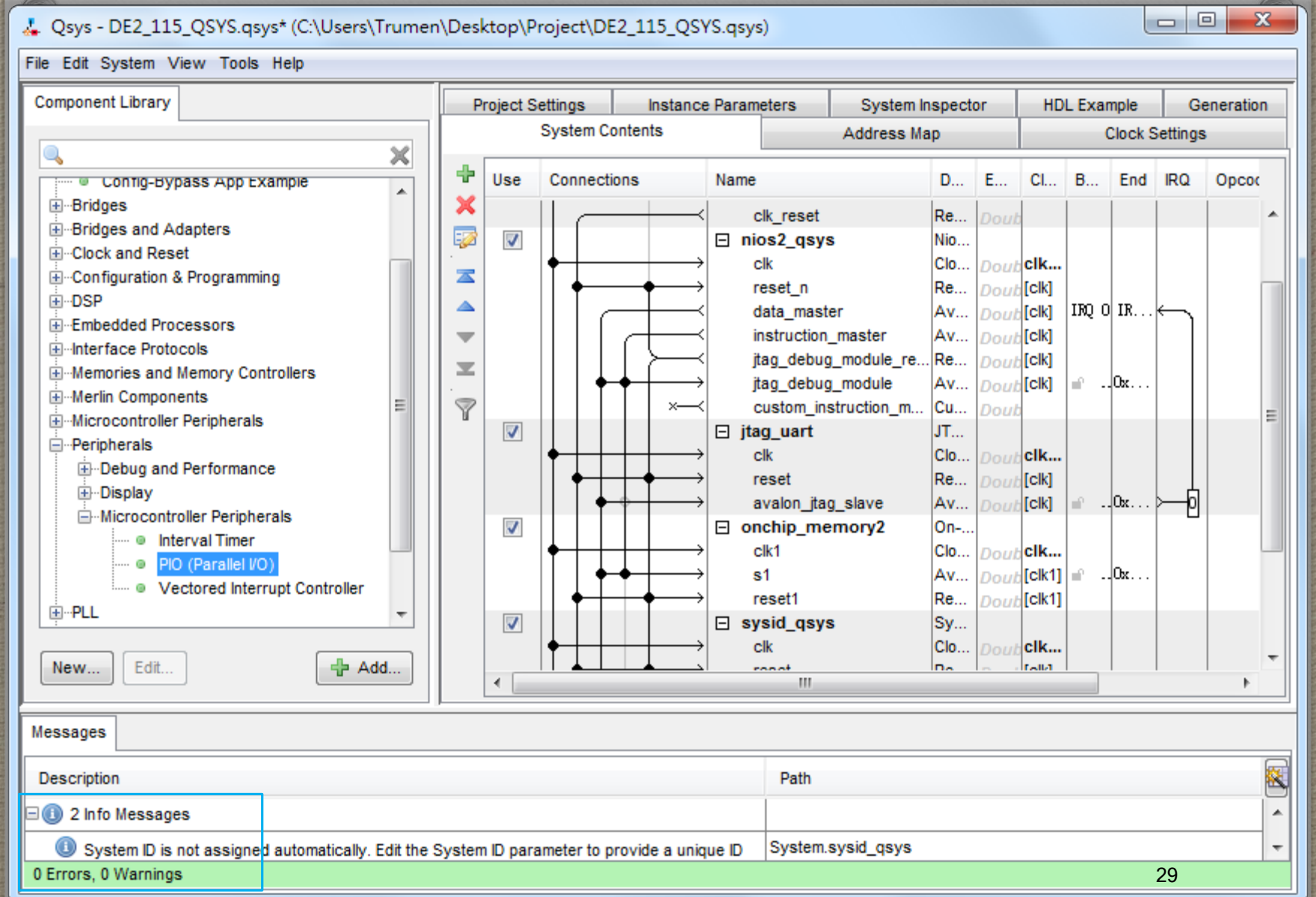
clk
IRQ
1
Messages
Description
Path
1 Warning
Interrupt sender jtag_uart.irq is not connected to an interrupt receiver
System.jtag_uart
0 Errors, 1 Warning
28


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
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nios2_qsys
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reset_n
data_master
instruction_master
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jtag_debug_module
custom_instruction_m...
jtag_uart
clk
reset
avalon_jtag_slave
onchip_memory2
clk1
s1
reset1
sysid_qsys
clk
End
IRQ
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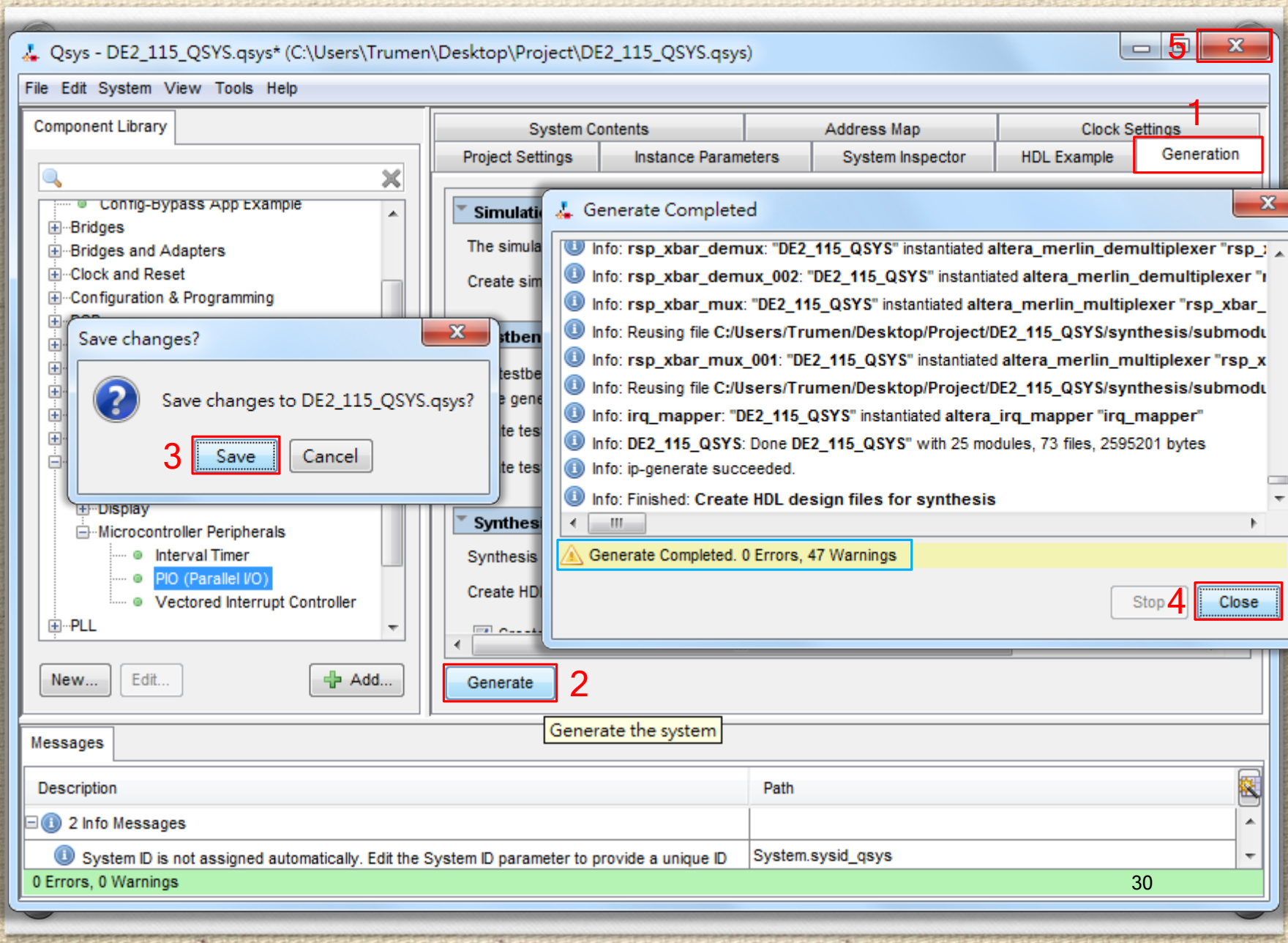
Description
Path
2 Info Messages
System ID is not assigned automatically. Edit the System ID parameter to provide a unique ID
System.sysid_qsys
0 Errors, 0 Warnings


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
File Edit System View Tools Help
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Edit...
Add...
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Project Settings
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System Inspector
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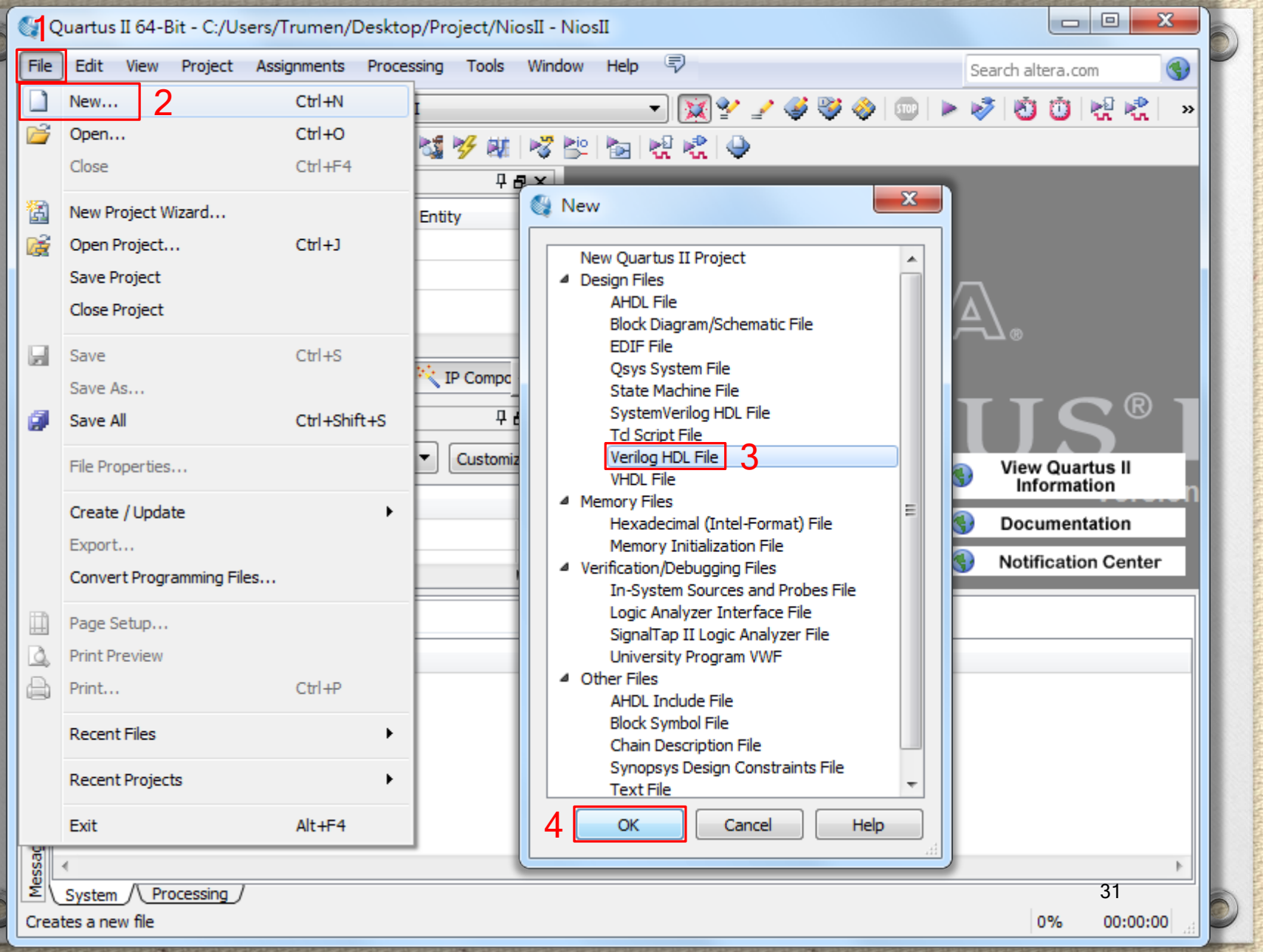
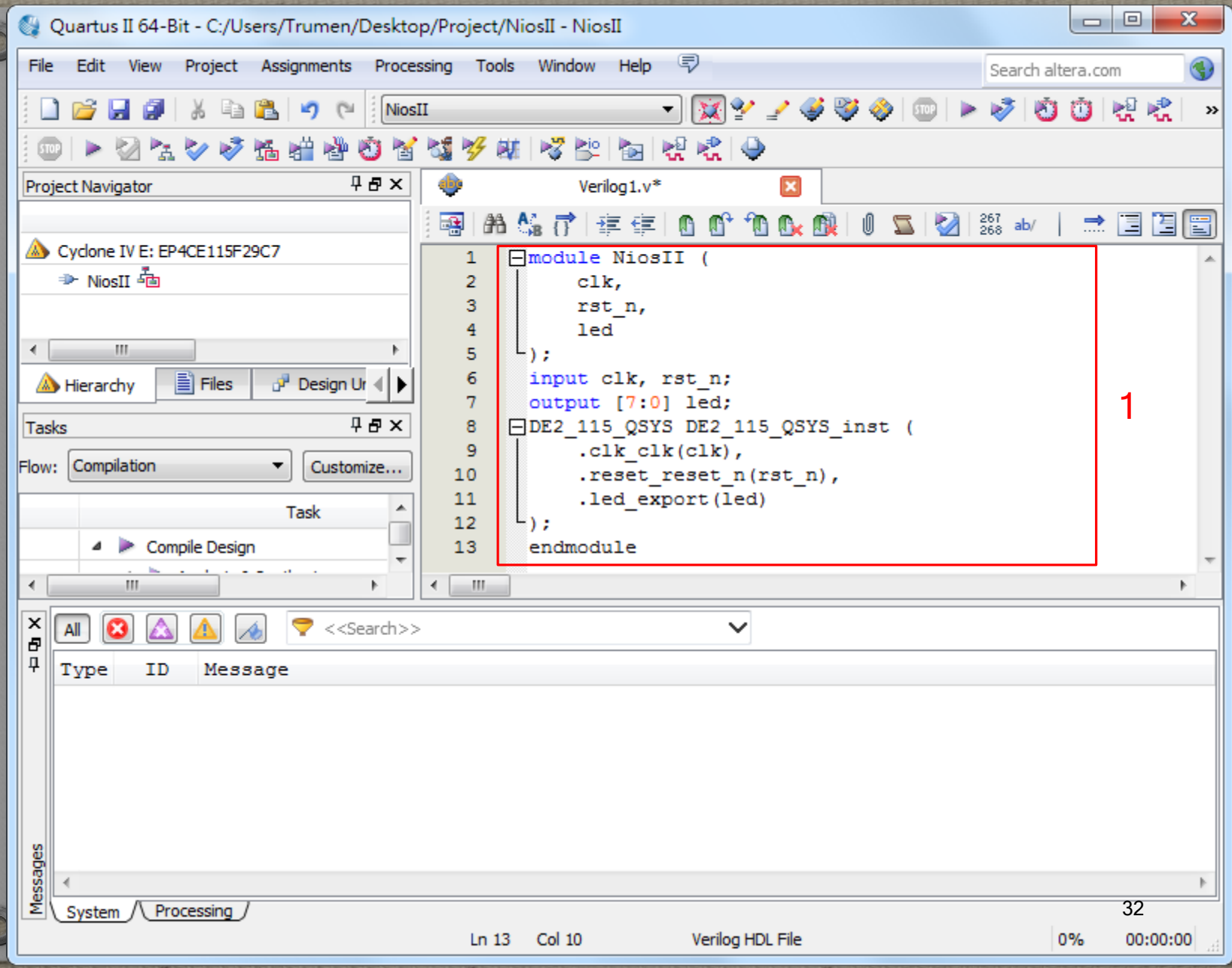
1
Generate
2
Generate the system
Save changes?
Save changes to DE2_115_QSYS.qsys?
3
Save
Cancel
Generate Completed
Info: rsp_xbar_demux: "DE2_115_QSYS" instantiated altera_merlin_demultiplexer
Info: rsp_xbar_demux_002: "DE2_115_QSYS" instantiated altera_merlin_demultiplexer
Info: rsp_xbar_mux: "DE2_115_QSYS" instantiated altera_merlin_multiplexer
Info: Reusing file C:/Users/Trumen/Desktop/Project/DE2_115_QSYS/synthesis/submodu
Info: rsp_xbar_mux_001: "DE2_115_QSYS" instantiated altera_merlin_multiplexer
Info: Reusing file C:/Users/Trumen/Desktop/Project/DE2_115_QSYS/synthesis/submodu
Info: irq_mapper: "DE2_115_QSYS" instantiated altera_irq_mapper "irq_mapper"
Info: DE2_115_QSYS: Done DE2_115_QSYS" with 25 modules, 73 files, 2595201 bytes
Info: ip-generate succeeded.
Info: Finished: Create HDL design files for synthesis
Generate Completed. 0 Errors, 47 Warnings
Stop
4
Close
5
Messages
Description
Path
2 Info Messages
System ID is not assigned automatically. Edit the System ID parameter to provide a unique ID
System.sysid_qsys
0 Errors, 0 Warnings
30


1
Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
File
Edit
View
Project
Assignments
Processing
Tools
Window
Help
Search altera.com
New... Ctrl+N
2
Open... Ctrl+O
Close Ctrl+F4
New Project Wizard...
Open Project... Ctrl+J
Save Project
Close Project
Save Ctrl+S
Save As...
Save All Ctrl+Shift+S
File Properties...
Create / Update
Export...
Convert Programming Files...
Page Setup...
Print Preview
Print... Ctrl+P
Recent Files
Recent Projects
Exit Alt+F4
New
New Quartus II Project
Design Files
AHDL File
Block Diagram/Schematic File
EDIF File
Qsys System File
State Machine File
SystemVerilog HDL File
Tcl Script File
Verilog HDL File
3
VHDL File
Memory Files
Hexadecimal (Intel-Format) File
Memory Initialization File
Verification/Debugging Files
In-System Sources and Probes File
Logic Analyzer Interface File
SignalTap II Logic Analyzer File
University Program VWF
Other Files
AHDL Include File
Block Symbol File
Chain Description File
Synopsys Design Constraints File
Text File
4
OK
Cancel
Help
Entity
IP Compc
Customiz
View Quartus II Information
Documentation
Notification Center
System
Processing
Creates a new file
0%
00:00:00


Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
File Edit View Project Assignments Processing Tools Window Help
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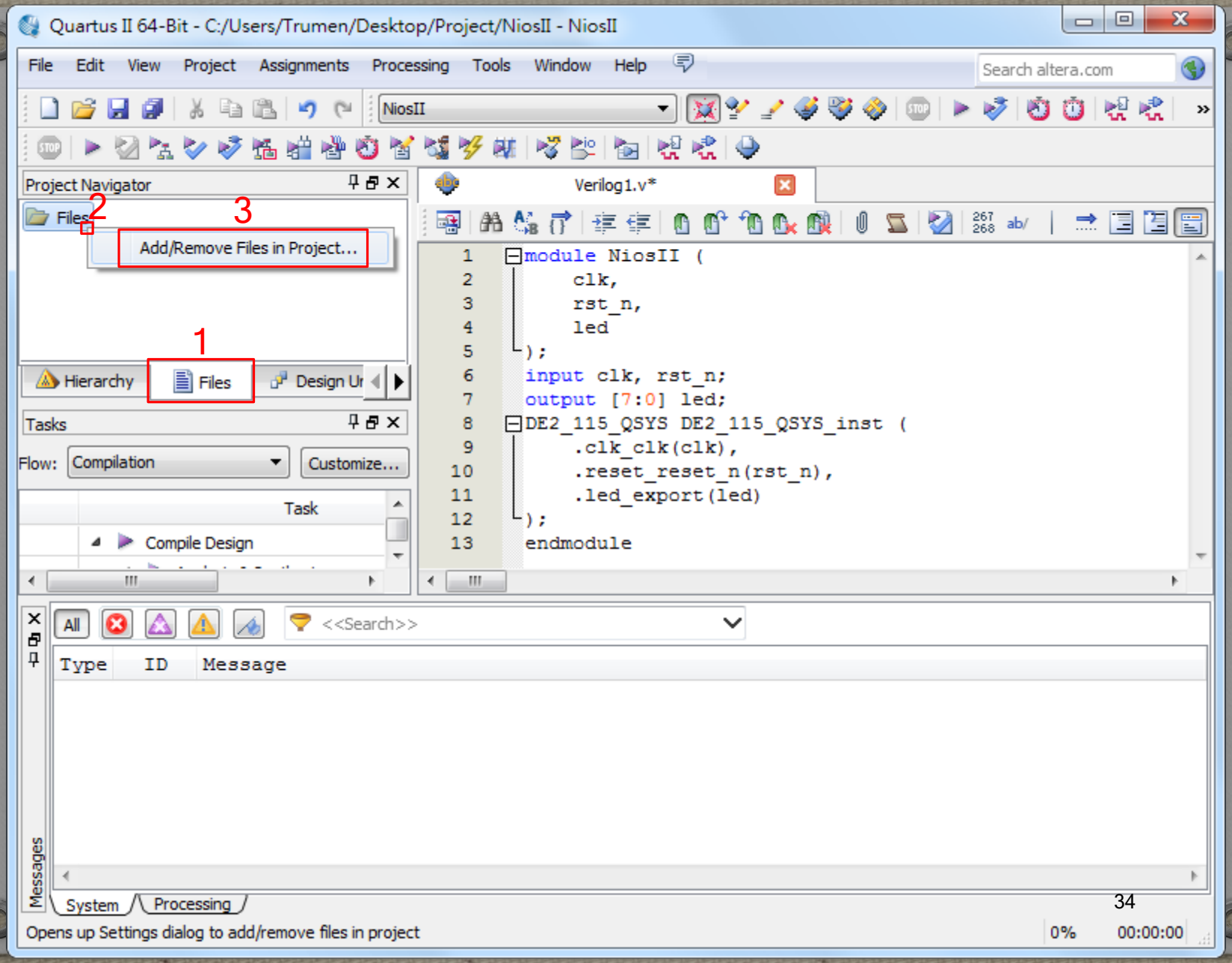
Project Navigator
Cyclone IV E: EP4CE115F29C7
NiosII
Hierarchy Files Design Ur
Tasks
Flow: Compilation Customize...
Task
Compile Design
Verilog1.v*
1 module NiosII (
2 clk,
3 rst_n,
4 led
5);
6 input clk, rst_n;
7 output [7:0] led;
8 DE2_115_QSYS DE2_115_QSYS_inst (
9 .clk_clk(clk),
10 .reset_reset_n(rst_n),
11 .led_export(led)
12);
13 endmodule
1
All
<<Search>>
Type ID Message
Messages
System Processing
Ln 13 Col 10 Verilog HDL File 0% 00:00:00

```
module NiosII (
    clk,
    rst_n,
    led,
);
input clk, rst_n;
output [7:0] led;
DE2_115_QSYS DE2_115_QSYS_inst (
    .clk_clk(clk),
    .reset_reset_n(rst_n),
    .led_export(led),
);
endmodule
```


Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
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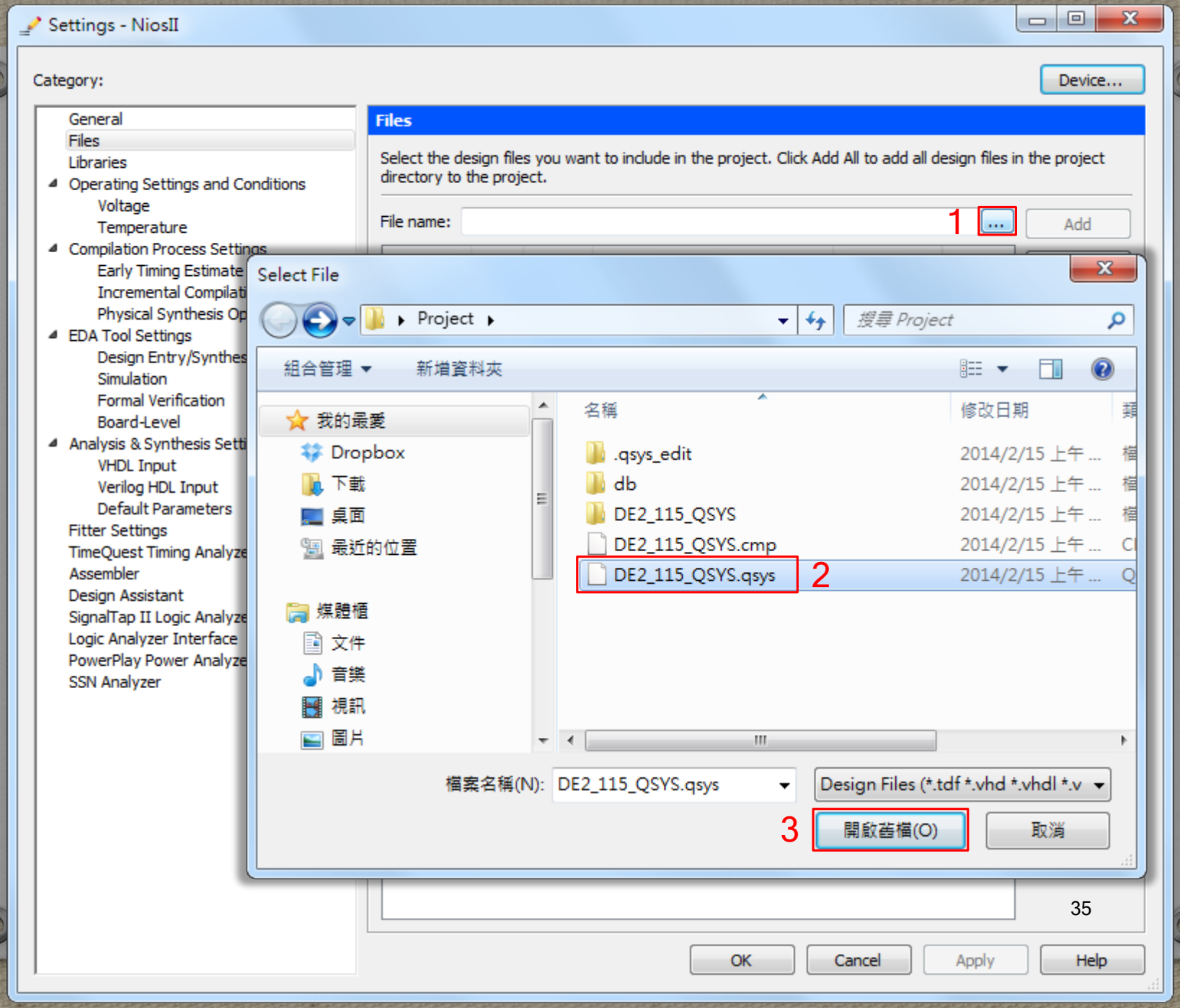
Project Navigator
Files
2
3
Add/Remove Files in Project...
1
Hierarchy
Files
Design Ur
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Verilog1.v*
1 module NiosII (
2 clk,
3 rst_n,
4 led
5);
6 input clk, rst_n;
7 output [7:0] led;
8 DE2_115_QSYS DE2_115_QSYS_inst (
9 .clk_clk(clk),
10 .reset_reset_n(rst_n),
11 .led_export(led)
12);
13 endmodule
All
<<Search>>
Type ID Message
Messages
System
Processing
Opens up Settings dialog to add/remove files in project
0%
00:00:00


Settings - NiosII
Category:
Device...
General
Files
Libraries
Operating Settings and Conditions
Voltage
Temperature
Compilation Process Settings
Early Timing Estimate
Incremental Compilati
Physical Synthesis Op
EDA Tool Settings
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VHDL Input
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Default Parameters
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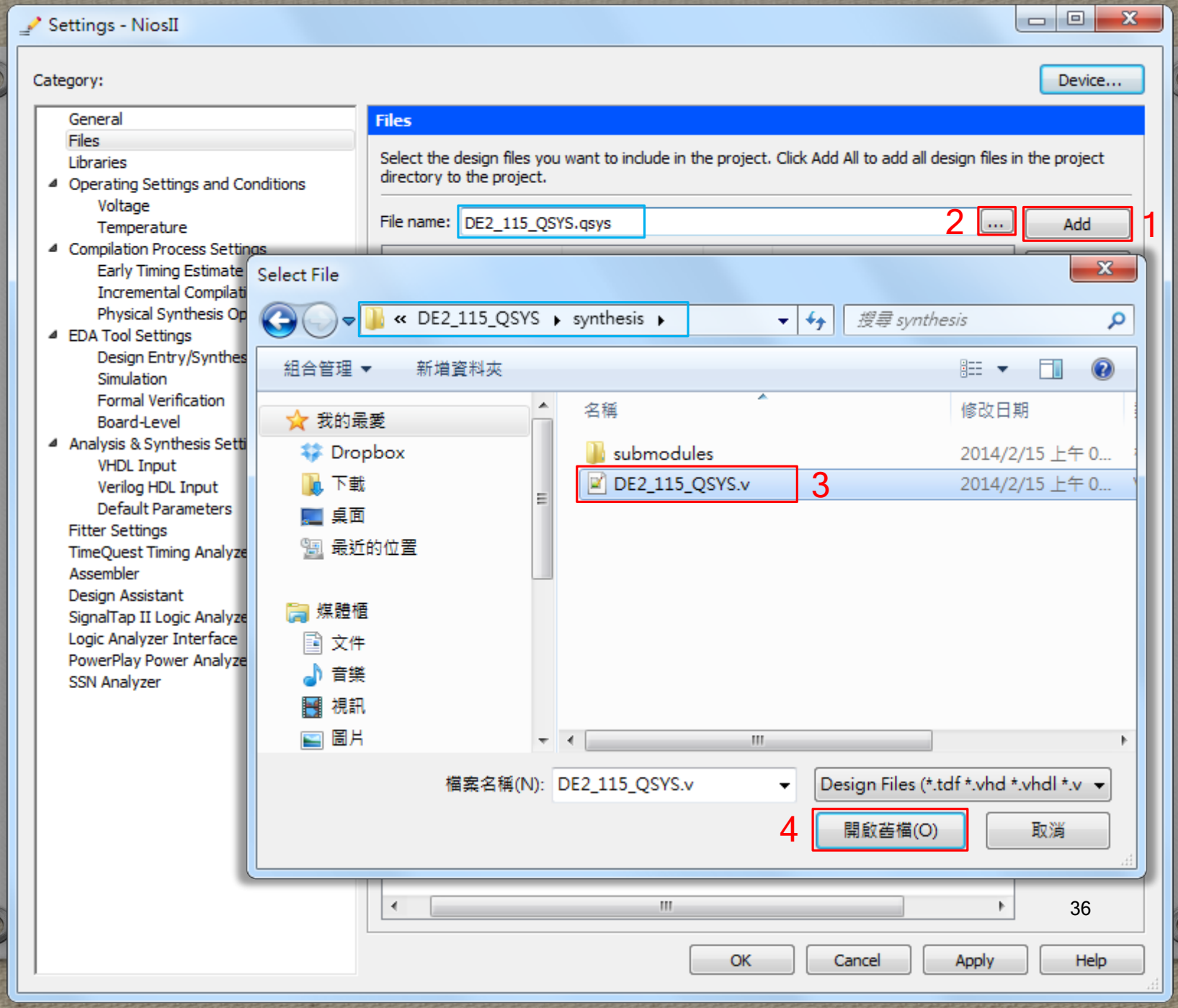
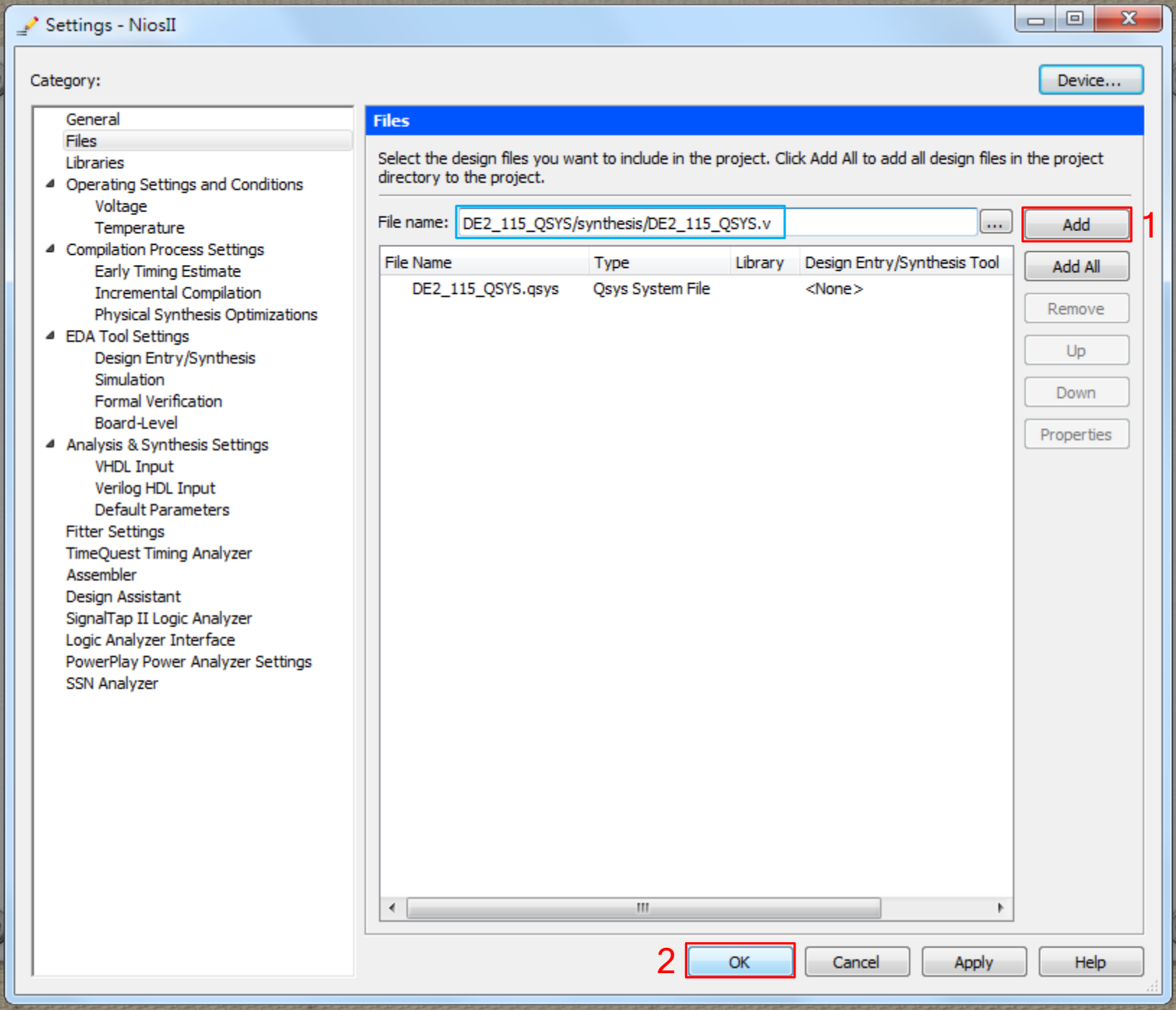
TimeQuest Timing Analyze
Assembler
Design Assistant
SignalTap II Logic Analyze
Logic Analyzer Interface
PowerPlay Power Analyze
SSN Analyzer
Files
Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.
File name:
1
...
Add
Select File
Project
搜尋 Project
組合管理
新增資料夾
我的最愛
Dropbox
下載
桌面
最近的位置
媒體櫃
文件
音樂
視訊
圖片
名稱
修改日期
.qsys_edit
db
DE2_115_QSYS
DE2_115_QSYS.cmp
DE2_115_QSYS.qsys
2
檔案名稱(N):
DE2_115_QSYS.qsys
Design Files (*.tdf *.vhd *.vhdl *.v
3
開啟舊檔(O)
取消
OK
Cancel
Apply
Help


Settings - NiosII
Category:
Device...
General
Files
Libraries
Operating Settings and Conditions
Voltage
Temperature
Compilation Process Settings
Early Timing Estimate
Incremental Compilati
Physical Synthesis Op
EDA Tool Settings
Design Entry/Synthes
Simulation
Formal Verification
Board-Level
Analysis & Synthesis Setti
VHDL Input
Verilog HDL Input
Default Parameters
Fitter Settings
TimeQuest Timing Analyze
Assembler
Design Assistant
SignalTap II Logic Analyze
Logic Analyzer Interface
PowerPlay Power Analyze
SSN Analyzer
Files
Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.
File name: DE2_115_QSYS.qsys
2
...
Add
1
Select File
« DE2_115_QSYS ▸ synthesis ▸
搜尋 synthesis
組合管理
新增資料夾
我的最愛
Dropbox
下載
桌面
最近的位置
媒體櫃
文件
音樂
視訊
圖片
名稱
修改日期
submodules
2014/2/15 上午 0...
DE2_115_QSYS.v
3
2014/2/15 上午 0...
檔案名稱(N): DE2_115_QSYS.v
Design Files (*.tdf *.vhd *.vhdl *.v
4
開啟舊檔(O)
取消
36
OK
Cancel
Apply
Help


Settings - NiosII
Category:
Device...
General
Files
Libraries
Operating Settings and Conditions
Voltage
Temperature
Compilation Process Settings
Early Timing Estimate
Incremental Compilation
Physical Synthesis Optimizations
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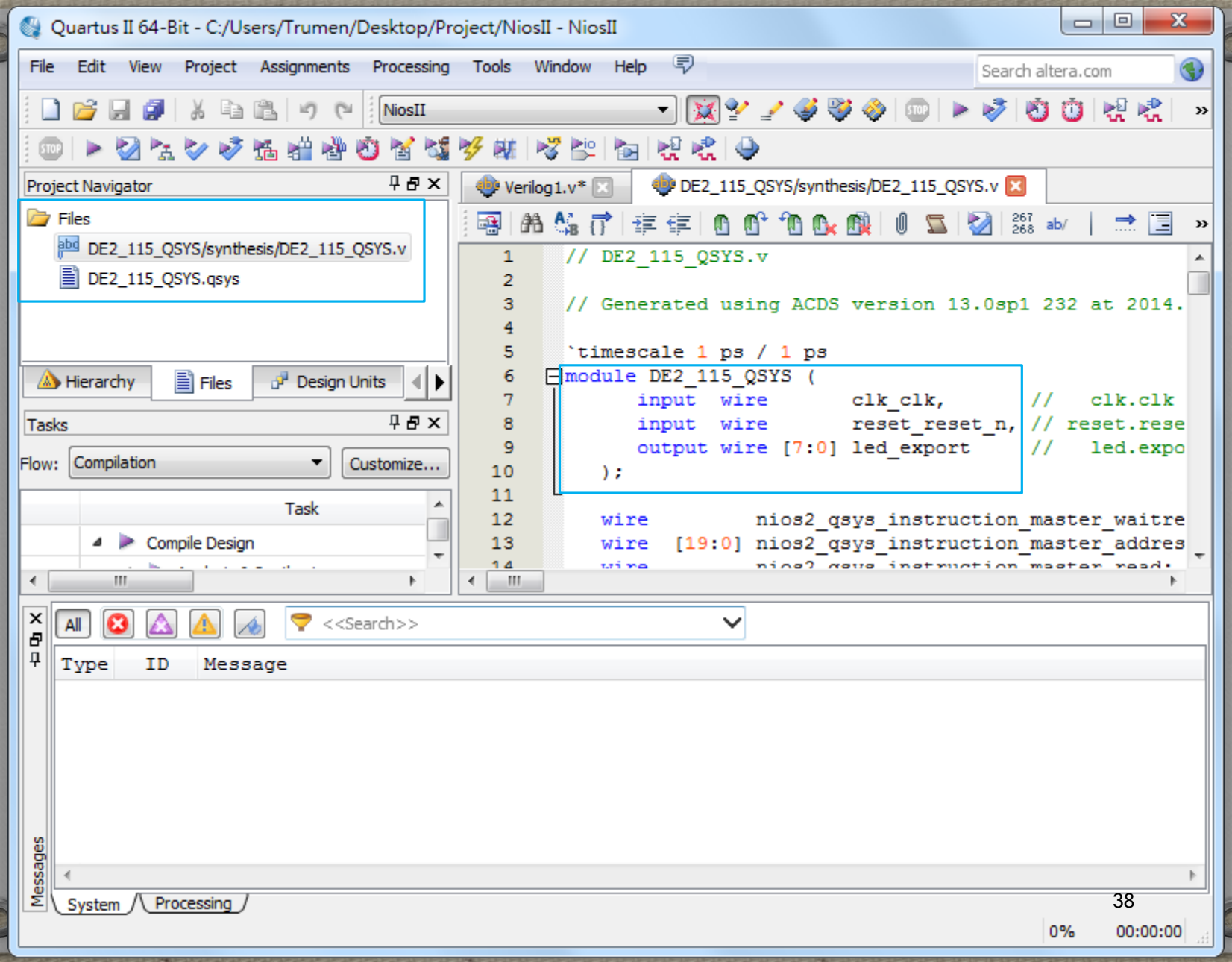
Default Parameters
Fitter Settings
TimeQuest Timing Analyzer
Assembler
Design Assistant
SignalTap II Logic Analyzer
Logic Analyzer Interface
PowerPlay Power Analyzer Settings
SSN Analyzer
Files
Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.
File name:
DE2_115_QSYS/synthesis/DE2_115_QSYS.v
...
Add
1
Add All
Remove
Up
Down
Properties
File Name
Type
Library
Design Entry/Synthesis Tool
DE2_115_QSYS.qsys
Qsys System File
<None>
2
OK
Cancel
Apply
Help


Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
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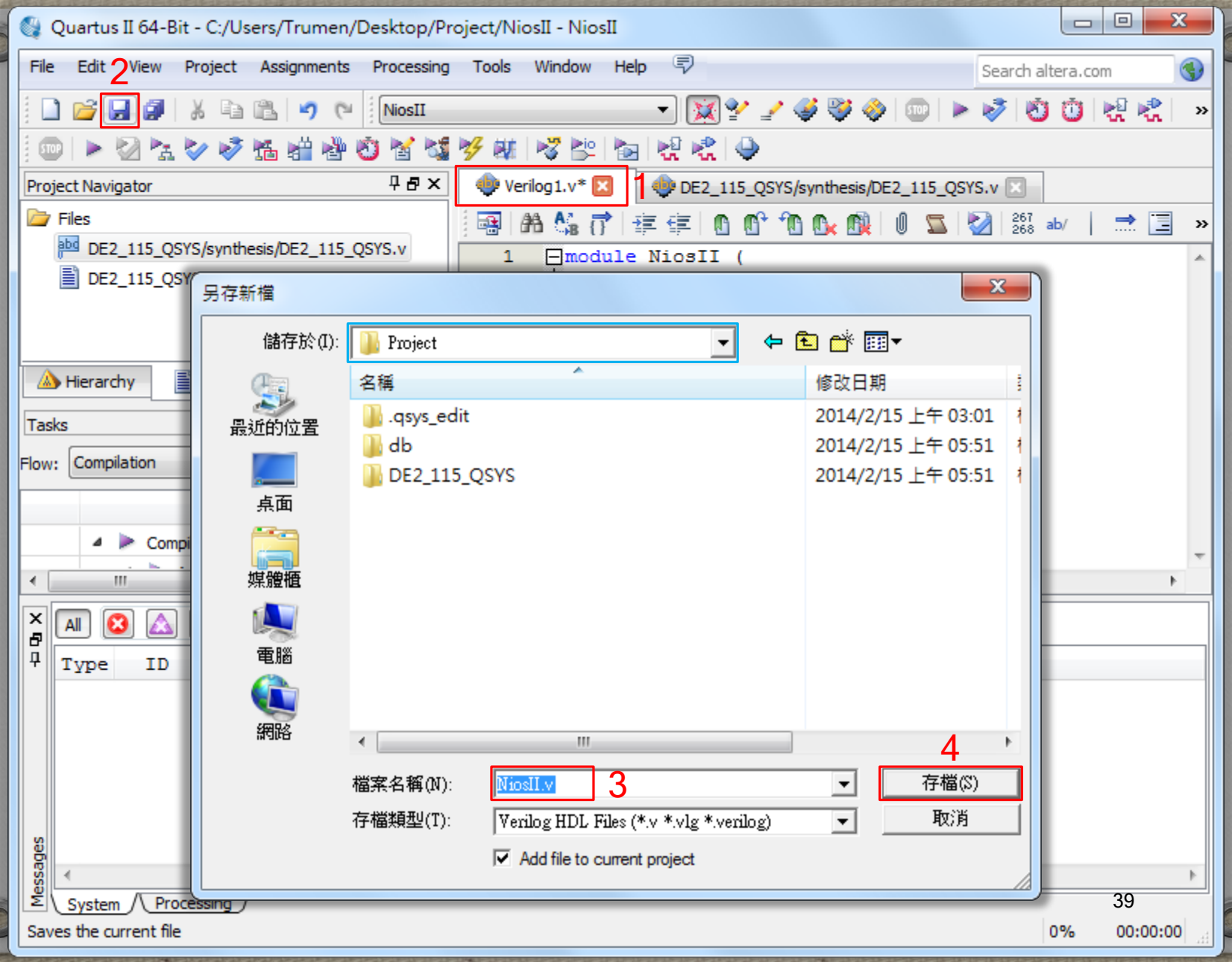
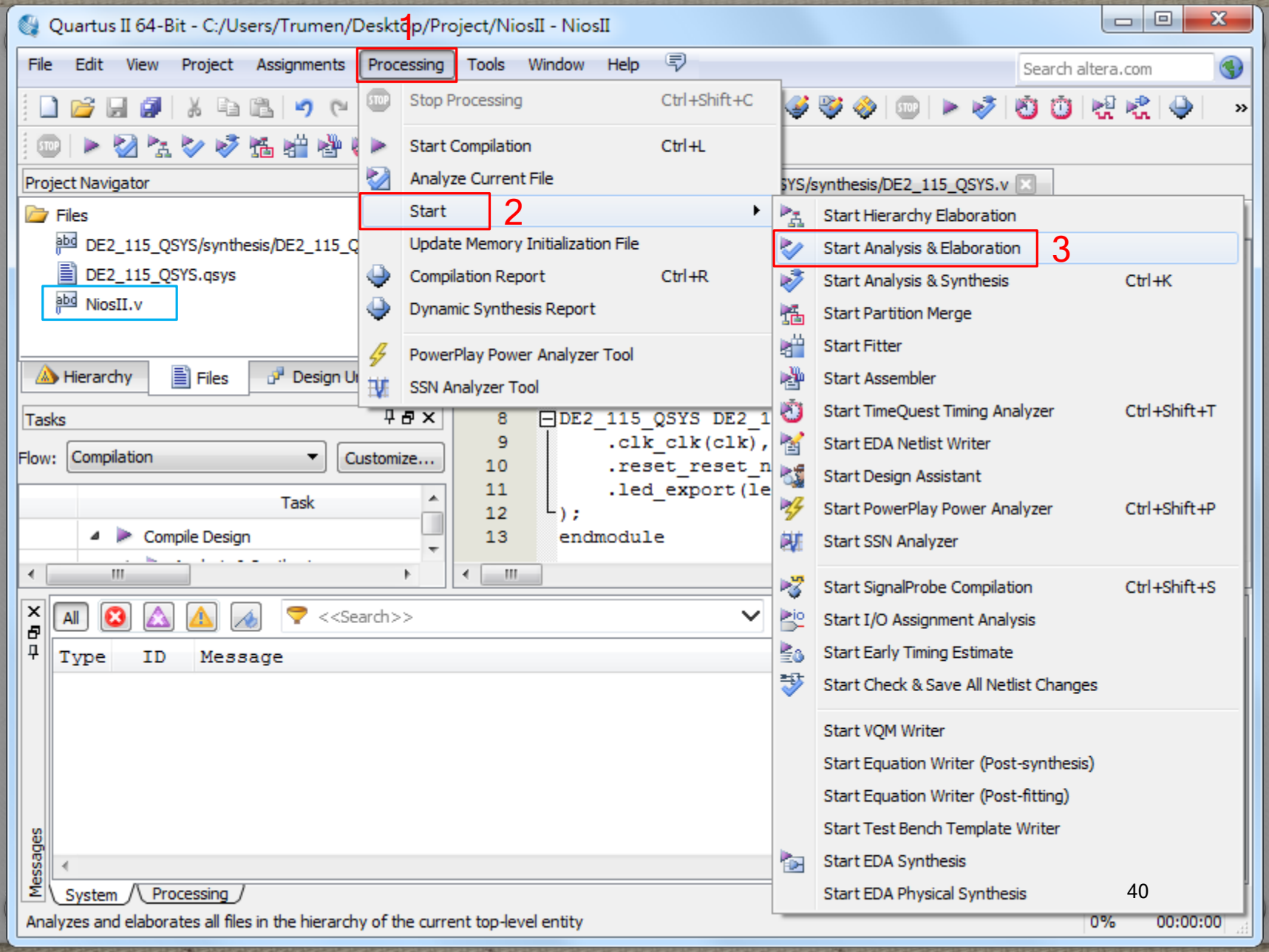
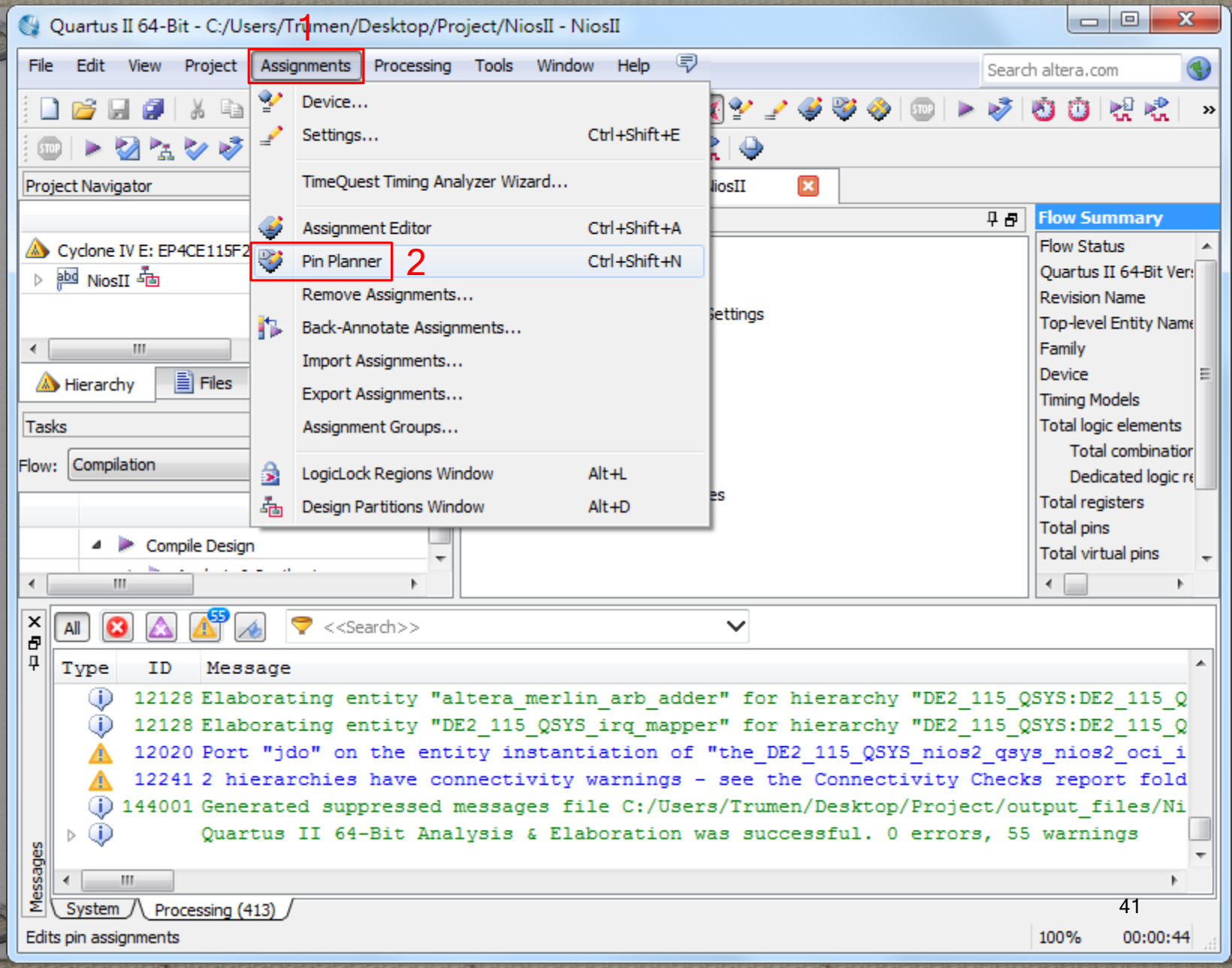
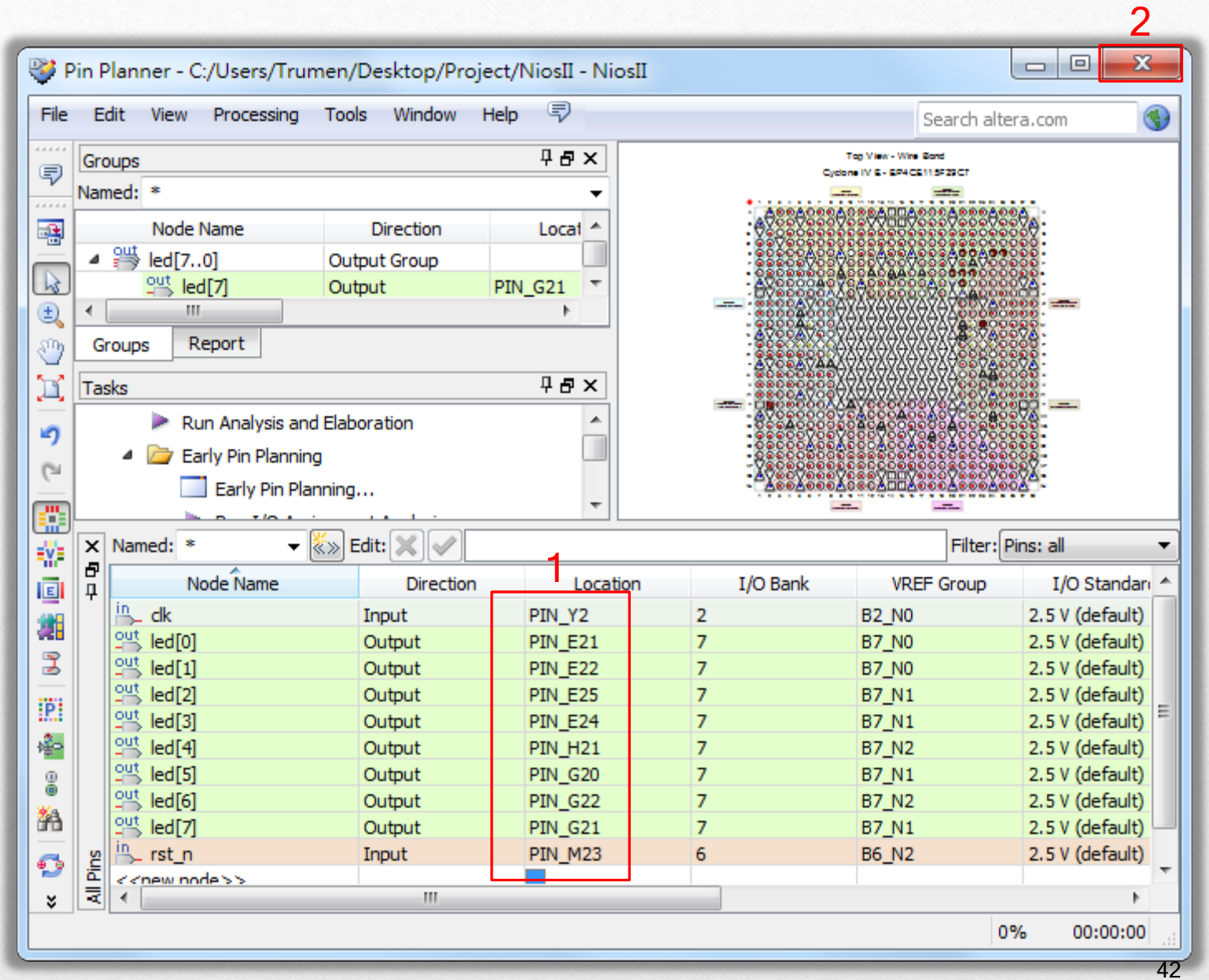
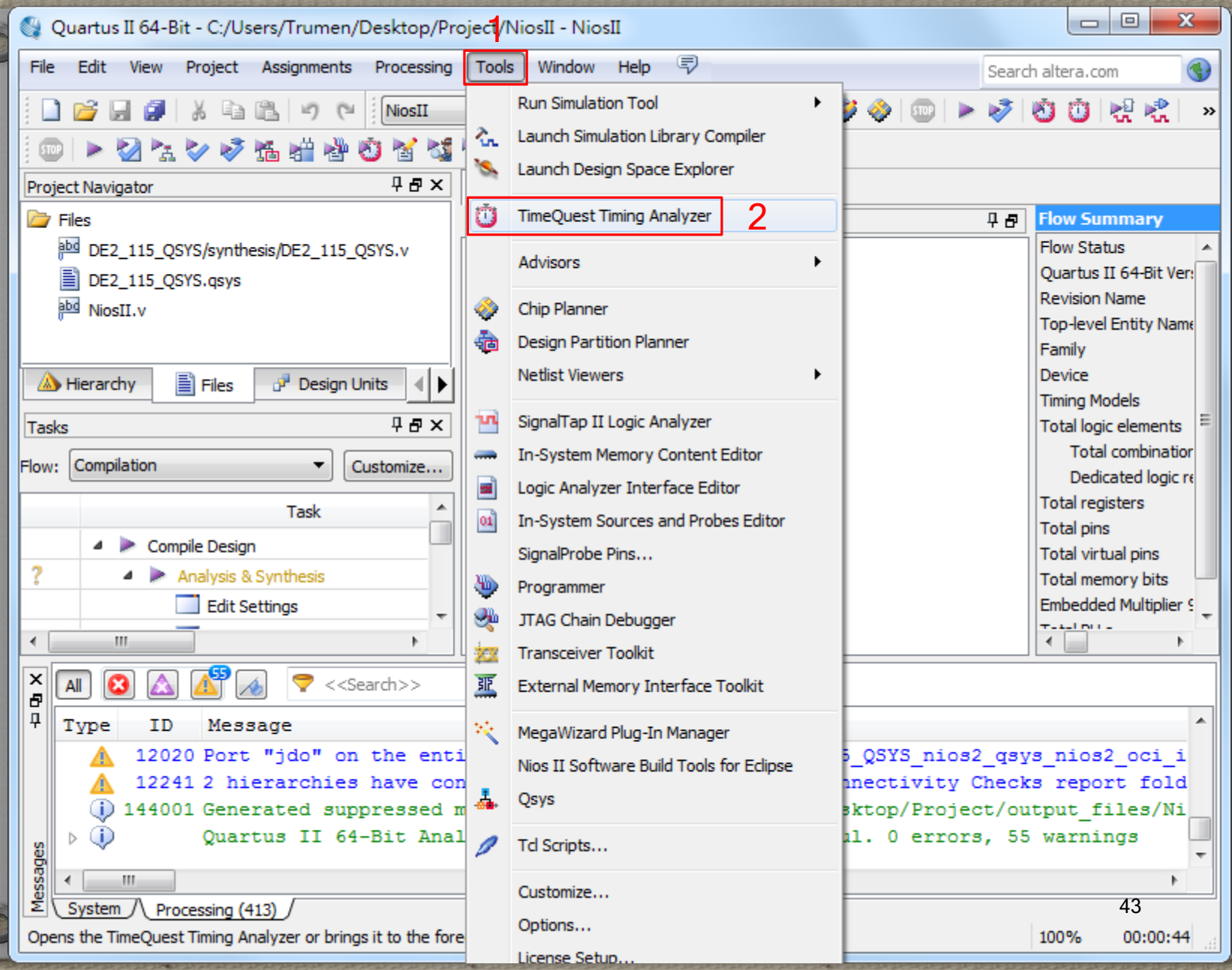
Project Navigator
Files
DE2_115_QSYS/synthesis/DE2_115_QSYS.v
DE2_115_QSYS.qsys
Hierarchy Files Design Units
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Verilog1.v*
DE2_115_QSYS/synthesis/DE2_115_QSYS.v
1 // DE2_115_QSYS.v
2
3 // Generated using ACDS version 13.0sp1 232 at 2014.
4
5 `timescale 1 ps / 1 ps
6 module DE2_115_QSYS (
7 input wire clk_clk, // clk.clk
8 input wire reset_reset_n, // reset.rese
9 output wire [7:0] led_export // led.expo
10);
11
12 wire nios2_qsys_instruction_master_waitre
13 wire [19:0] nios2_qsys_instruction_master_addres
All
<<Search>>
Type ID Message
Messages
System Processing
0% 00:00:00

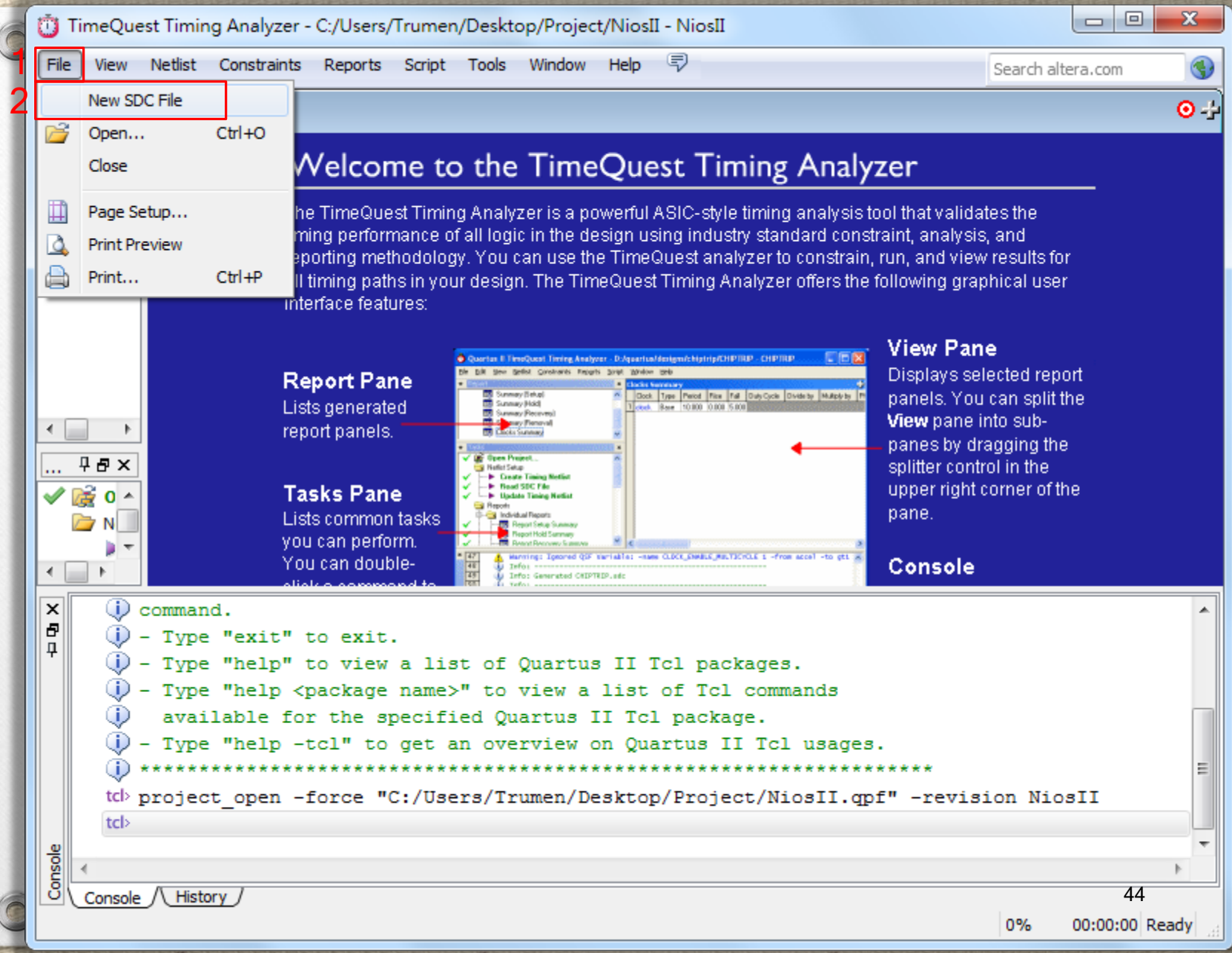

Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
File Edit View Project Assignments Processing Tools Window Help
2
Search altera.com
NiosII
Project Navigator
Files
DE2_115_QSYS/synthesis/DE2_115_QSYS.v
Verilog1.v*
1
DE2_115_QSYS/synthesis/DE2_115_QSYS.v
1 module NiosII (
Hierarchy
Tasks
Flow: Compilation
All
Type ID
Messages
System Processing
Saves the current file
0% 00:00:00
另存新檔
儲存於(I): Project
名稱 修改日期
.qsys_edit 2014/2/15 上午 03:01
db 2014/2/15 上午 05:51
DE2_115_QSYS 2014/2/15 上午 05:51
最近的位置
桌面
媒體櫃
電腦
網路
4
檔案名稱(N): NiosII.v
3
存檔(S)
存檔類型(T): Verilog HDL Files (*.v *.vlg *.verilog)
取消
Add file to current project

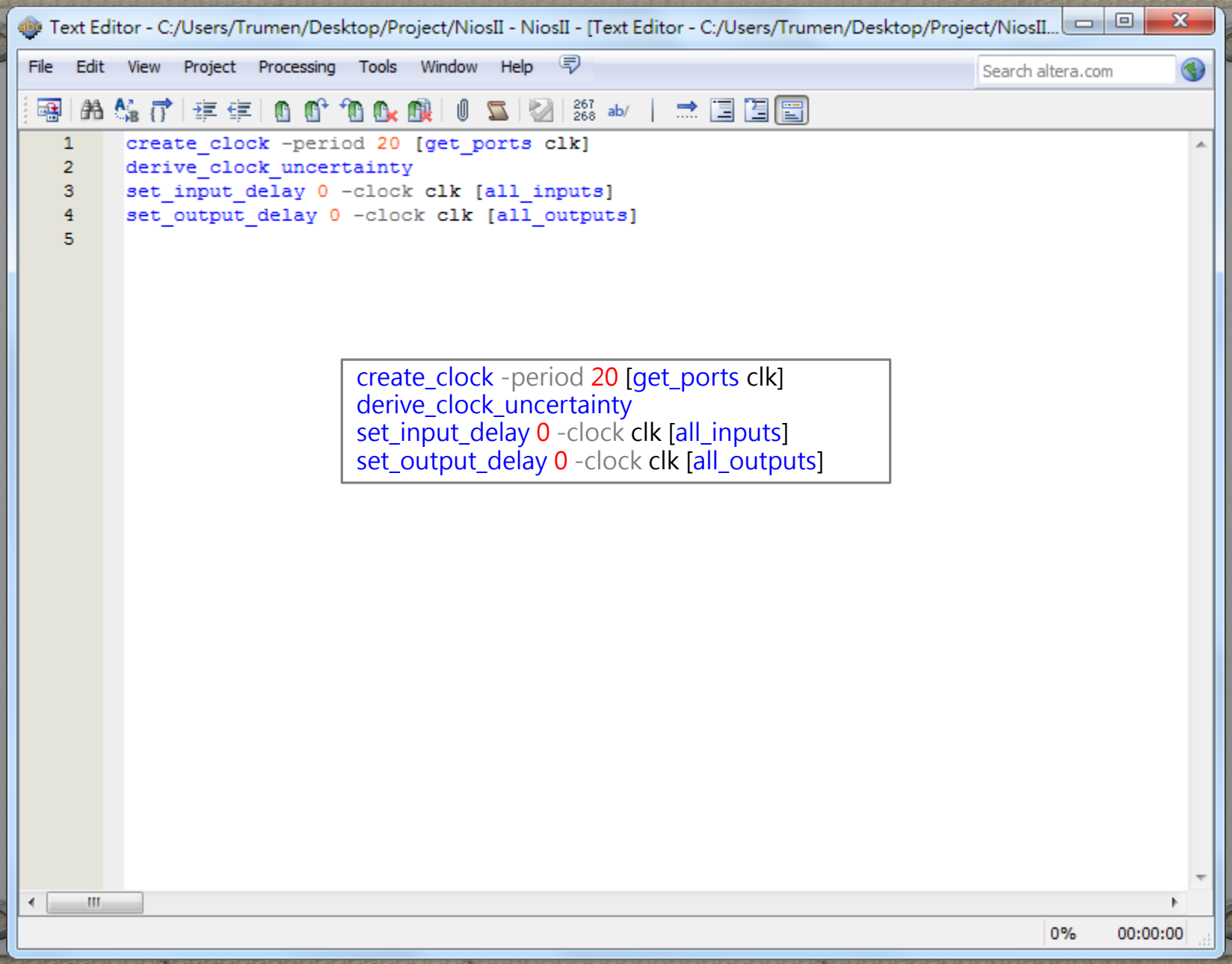

Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Stop Processing Ctrl+Shift+C
Start Compilation Ctrl+L
Analyze Current File
Start
2
Update Memory Initialization File
Compilation Report Ctrl+R
Dynamic Synthesis Report
PowerPlay Power Analyzer Tool
SSN Analyzer Tool
Start Hierarchy Elaboration
Start Analysis & Elaboration
3
Start Analysis & Synthesis Ctrl+K
Start Partition Merge
Start Fitter
Start Assembler
Start TimeQuest Timing Analyzer Ctrl+Shift+T
Start EDA Netlist Writer
Start Design Assistant
Start PowerPlay Power Analyzer Ctrl+Shift+P
Start SSN Analyzer
Start SignalProbe Compilation Ctrl+Shift+S
Start I/O Assignment Analysis
Start Early Timing Estimate
Start Check & Save All Netlist Changes
Start VQM Writer
Start Equation Writer (Post-synthesis)
Start Equation Writer (Post-fitting)
Start Test Bench Template Writer
Start EDA Synthesis
Start EDA Physical Synthesis
Project Navigator
Files
DE2_115_QSYS/synthesis/DE2_115_Q
DE2_115_QSYS.qsys
NiosII.v
Hierarchy Files Design U
Tasks
Flow: Compilation Customize...
Task
Compile Design
8 DE2_115_QSYS DE2_1
9 .clk_clk(clk),
10 .reset_reset_n
11 .led_export(le
12);
13 endmodule
All <<Search>>
Type ID Message
Messages
System Processing
Analyzes and elaborates all files in the hierarchy of the current top-level entity
0% 00:00:00
40


Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
1
File
Edit
View
Project
Assignments
Processing
Tools
Window
Help
Search altera.com
Device...
Settings... Ctrl+Shift+E
TimeQuest Timing Analyzer Wizard...
Assignment Editor Ctrl+Shift+A
Pin Planner Ctrl+Shift+N
2
Remove Assignments...
Back-Annotate Assignments...
Import Assignments...
Export Assignments...
Assignment Groups...
LogicLock Regions Window Alt+L
Design Partitions Window Alt+D
Project Navigator
Cyclone IV E: EP4CE115F2
NiosII
Hierarchy
Files
Tasks
Flow: Compilation
Compile Design
Flow Summary
Flow Status
Quartus II 64-Bit Ver
Revision Name
Top-level Entity Name
Family
Device
Timing Models
Total logic elements
Total combinatior
Dedicated logic re
Total registers
Total pins
Total virtual pins
All
<<Search>>
Type ID Message
12128 Elaborating entity "altera_merlin_arb_adder" for hierarchy "DE2_115_QSYS:DE2_115_Q
12128 Elaborating entity "DE2_115_QSYS_irq_mapper" for hierarchy "DE2_115_QSYS:DE2_115_Q
12020 Port "jdo" on the entity instantiation of "the_DE2_115_QSYS_nios2_qsys_nios2_oci_i
12241 2 hierarchies have connectivity warnings - see the Connectivity Checks report fold
144001 Generated suppressed messages file C:/Users/Trumen/Desktop/Project/output_files/Ni
Quartus II 64-Bit Analysis & Elaboration was successful. 0 errors, 55 warnings
Messages
System
Processing (413)
Edits pin assignments
100%
00:00:44

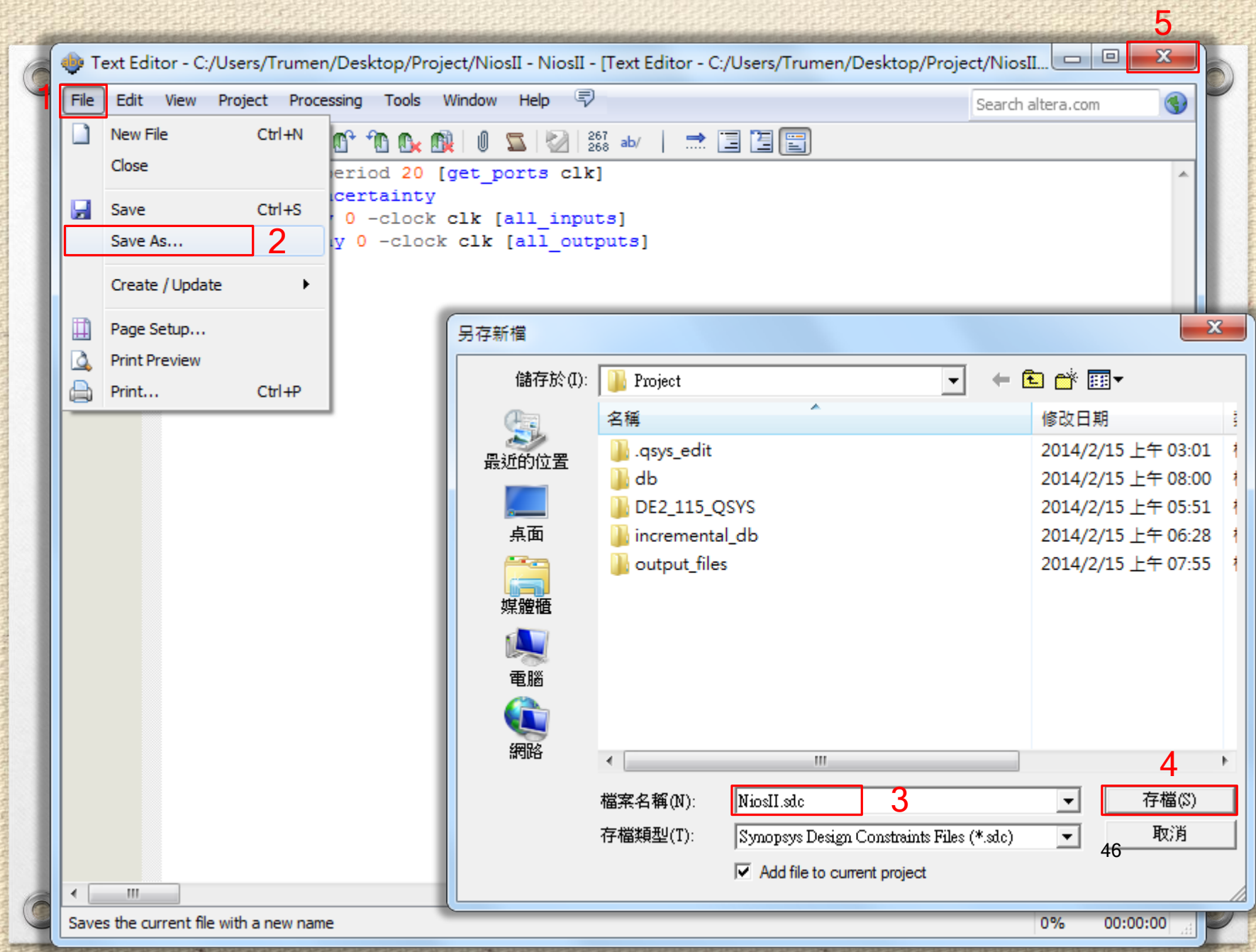

2
Pin Planner - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
File Edit View Processing Tools Window Help
Search altera.com
Groups
Named: *
Node Name Direction Locat
led[7..0] Output Group
led[7] Output PIN_G21
Groups Report
Tasks
Run Analysis and Elaboration
Early Pin Planning
Early Pin Planning...
Named: * Edit: Filter: Pins: all
1
Node Name Direction Location I/O Bank VREF Group I/O Standar
clk Input PIN_Y2 2 B2_N0 2.5 V (default)
led[0] Output PIN_E21 7 B7_N0 2.5 V (default)
led[1] Output PIN_E22 7 B7_N0 2.5 V (default)
led[2] Output PIN_E25 7 B7_N1 2.5 V (default)
led[3] Output PIN_E24 7 B7_N1 2.5 V (default)
led[4] Output PIN_H21 7 B7_N2 2.5 V (default)
led[5] Output PIN_G20 7 B7_N1 2.5 V (default)
led[6] Output PIN_G22 7 B7_N2 2.5 V (default)
led[7] Output PIN_G21 7 B7_N1 2.5 V (default)
rst_n Input PIN_M23 6 B6_N2 2.5 V (default)
<<new node>>
All Pins
0% 00:00:00

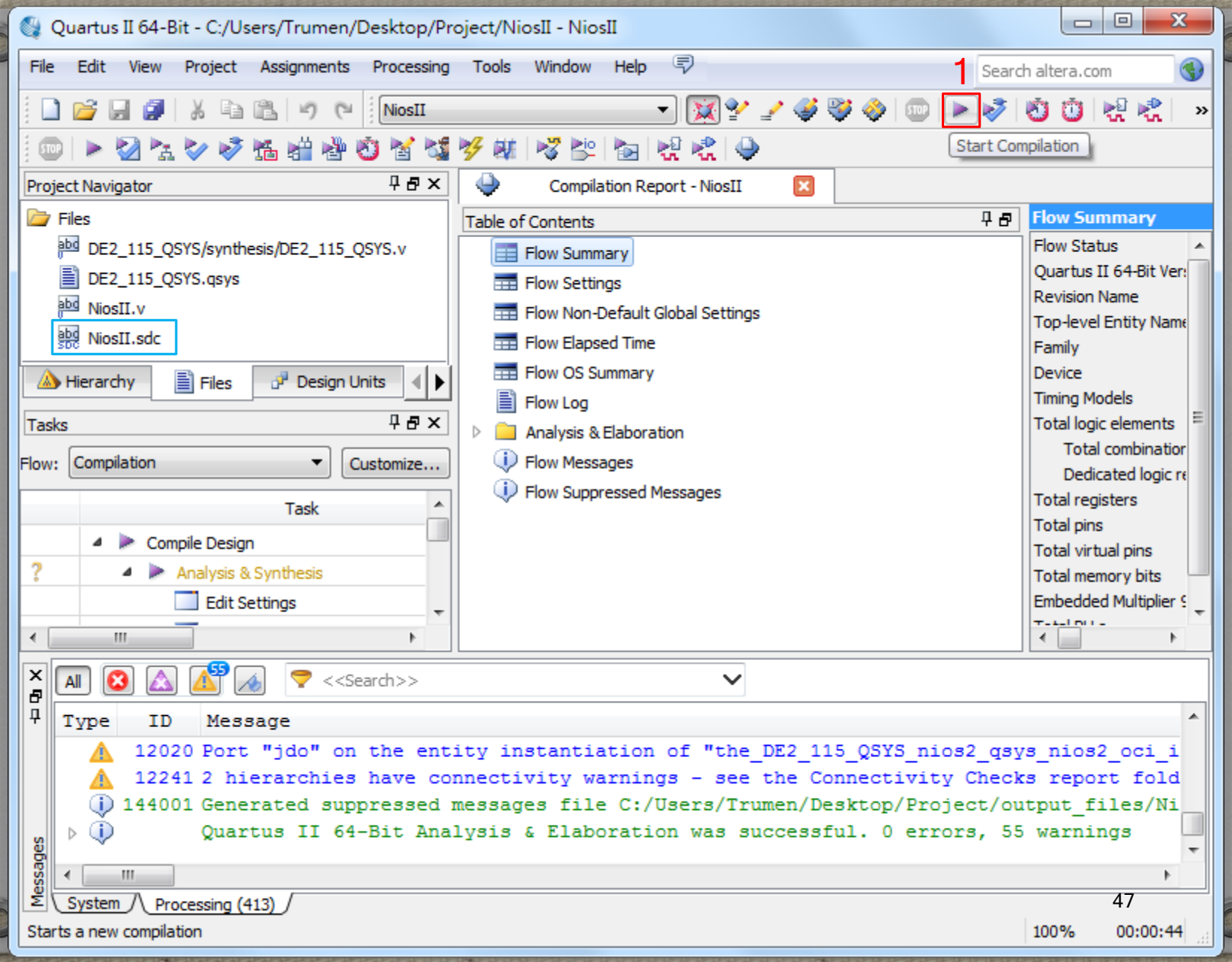

Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Run Simulation Tool
Launch Simulation Library Compiler
Launch Design Space Explorer
TimeQuest Timing Analyzer
2
Advisors
Chip Planner
Design Partition Planner
Netlist Viewers
SignalTap II Logic Analyzer
In-System Memory Content Editor
Logic Analyzer Interface Editor
In-System Sources and Probes Editor
SignalProbe Pins...
Programmer
JTAG Chain Debugger
Transceiver Toolkit
External Memory Interface Toolkit
MegaWizard Plug-In Manager
Nios II Software Build Tools for Eclipse
Qsys
Tcl Scripts...
Customize...
Options...
License Setup...
Project Navigator
Files
DE2_115_QSYS/synthesis/DE2_115_QSYS.v
DE2_115_QSYS.qsys
NiosII.v
Hierarchy
Files
Design Units
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Analysis & Synthesis
Edit Settings
Flow Summary
Flow Status
Quartus II 64-Bit Ver
Revision Name
Top-level Entity Name
Family
Device
Timing Models
Total logic elements
Total combinatior
Dedicated logic re
Total registers
Total pins
Total virtual pins
Total memory bits
Embedded Multiplier
Type ID Message
12020 Port "jdo" on the enti
12241 2 hierarchies have con
144001 Generated suppressed m
Quartus II 64-Bit Anal
_QSYS_nios2_qsys_nios2_oci_i
nnectivity Checks report fold
sktop/Project/output_files/Ni
l. 0 errors, 55 warnings
Messages
System
Processing (413)
Opens the TimeQuest Timing Analyzer or brings it to the fore
100%
00:00:44

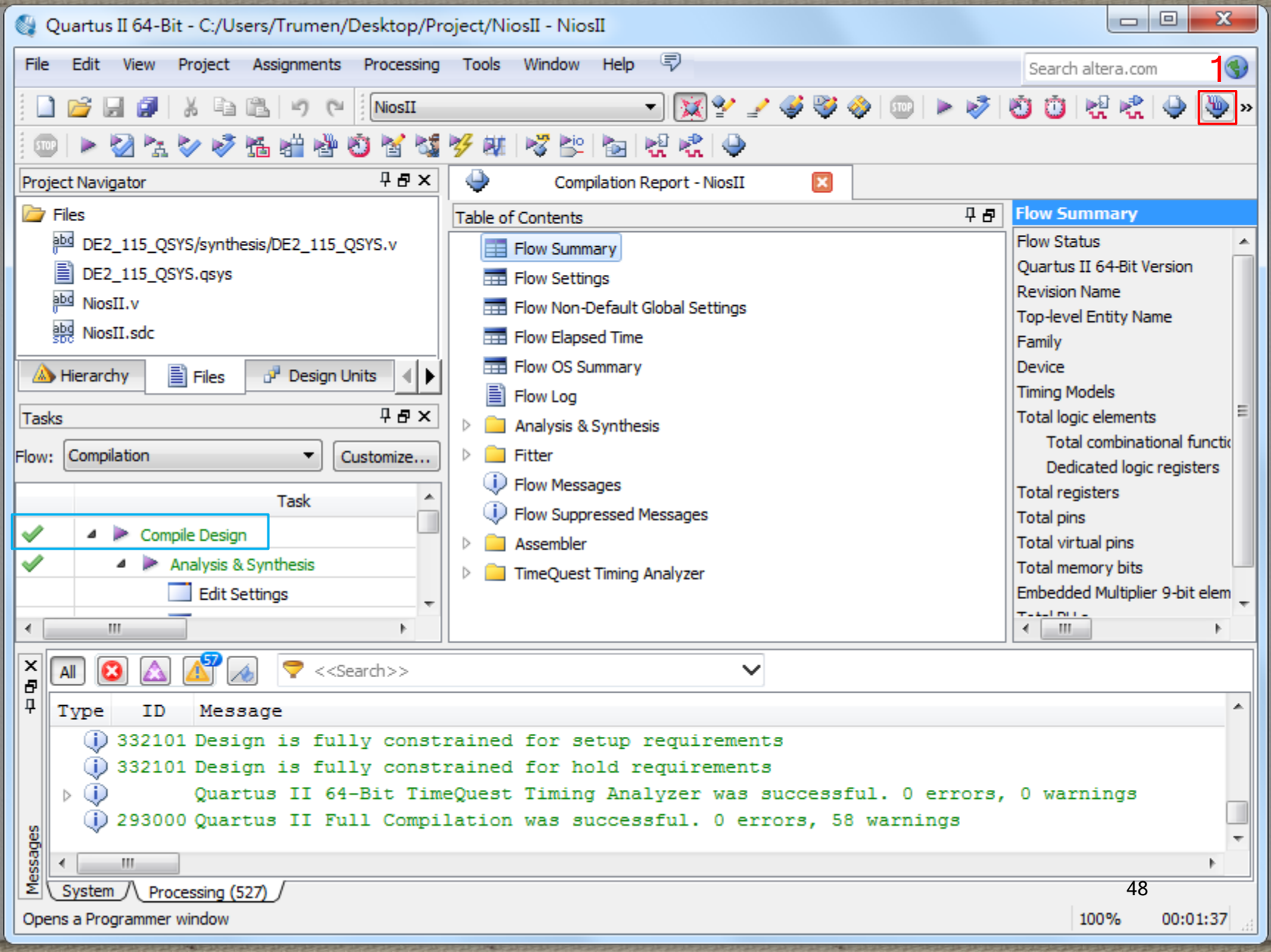

TimeQuest Timing Analyzer - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
1
File
View
Netlist
Constraints
Reports
Script
Tools
Window
Help
Search altera.com
2
New SDC File
Open... Ctrl+O
Close
Page Setup...
Print Preview
Print... Ctrl+P
Welcome to the TimeQuest Timing Analyzer
he TimeQuest Timing Analyzer is a powerful ASIC-style timing analysis tool that validates the
ming performance of all logic in the design using industry standard constraint, analysis, and
eporting methodology. You can use the TimeQuest analyzer to constrain, run, and view results for
ll timing paths in your design. The TimeQuest Timing Analyzer offers the following graphical user
nterface features:
Report Pane
Lists generated report panels.
Tasks Pane
Lists common tasks you can perform. You can double-
View Pane
Displays selected report panels. You can split the View pane into sub-panes by dragging the splitter control in the upper right corner of the pane.
Console
command.
- Type "exit" to exit.
- Type "help" to view a list of Quartus II Tcl packages.
- Type "help <package name>" to view a list of Tcl commands
available for the specified Quartus II Tcl package.
- Type "help -tcl" to get an overview on Quartus II Tcl usages.
tcl> project_open -force "C:/Users/Trumen/Desktop/Project/NiosII.qpf" -revision NiosII
tcl>
Console
Console
History
0%
00:00:00
Ready

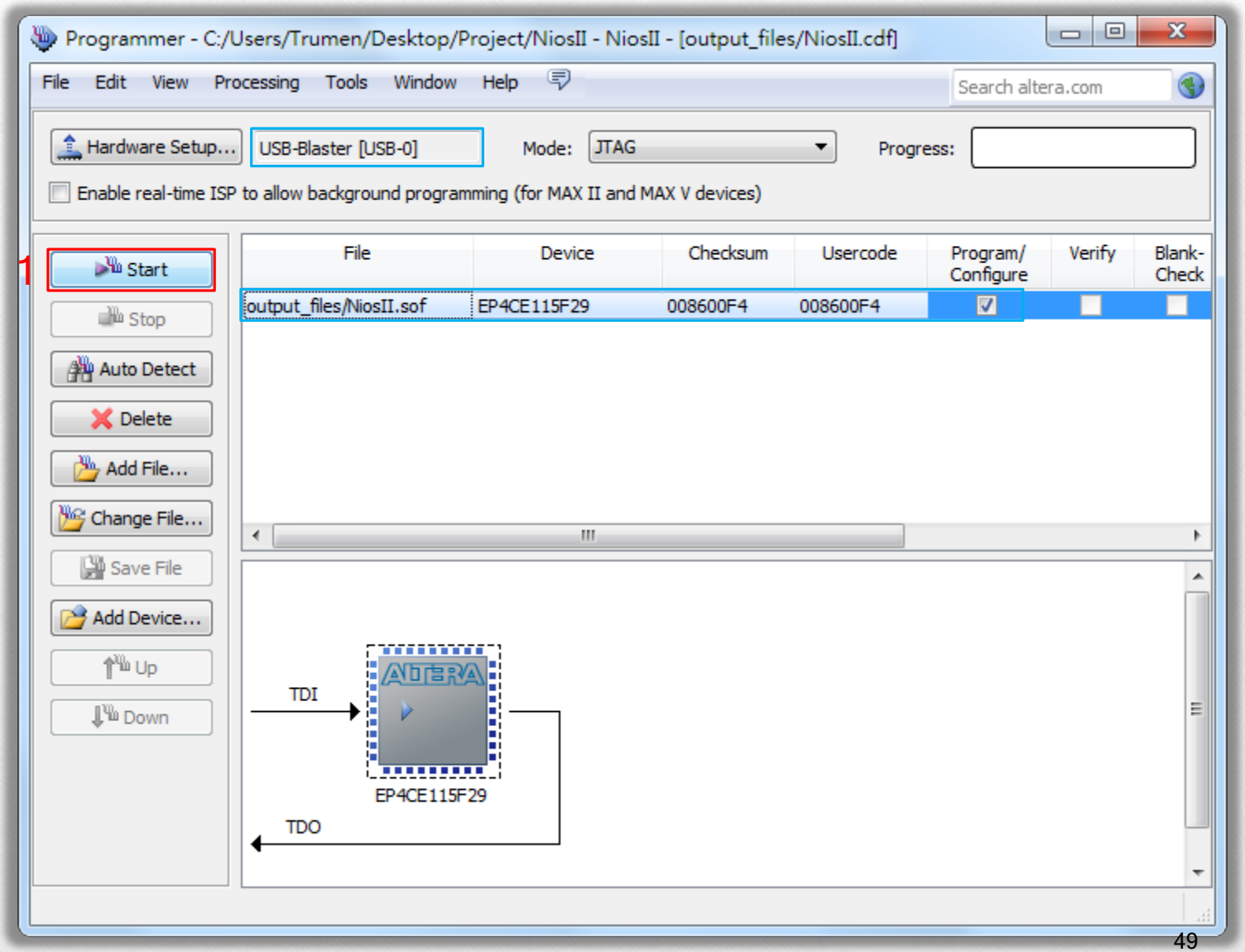


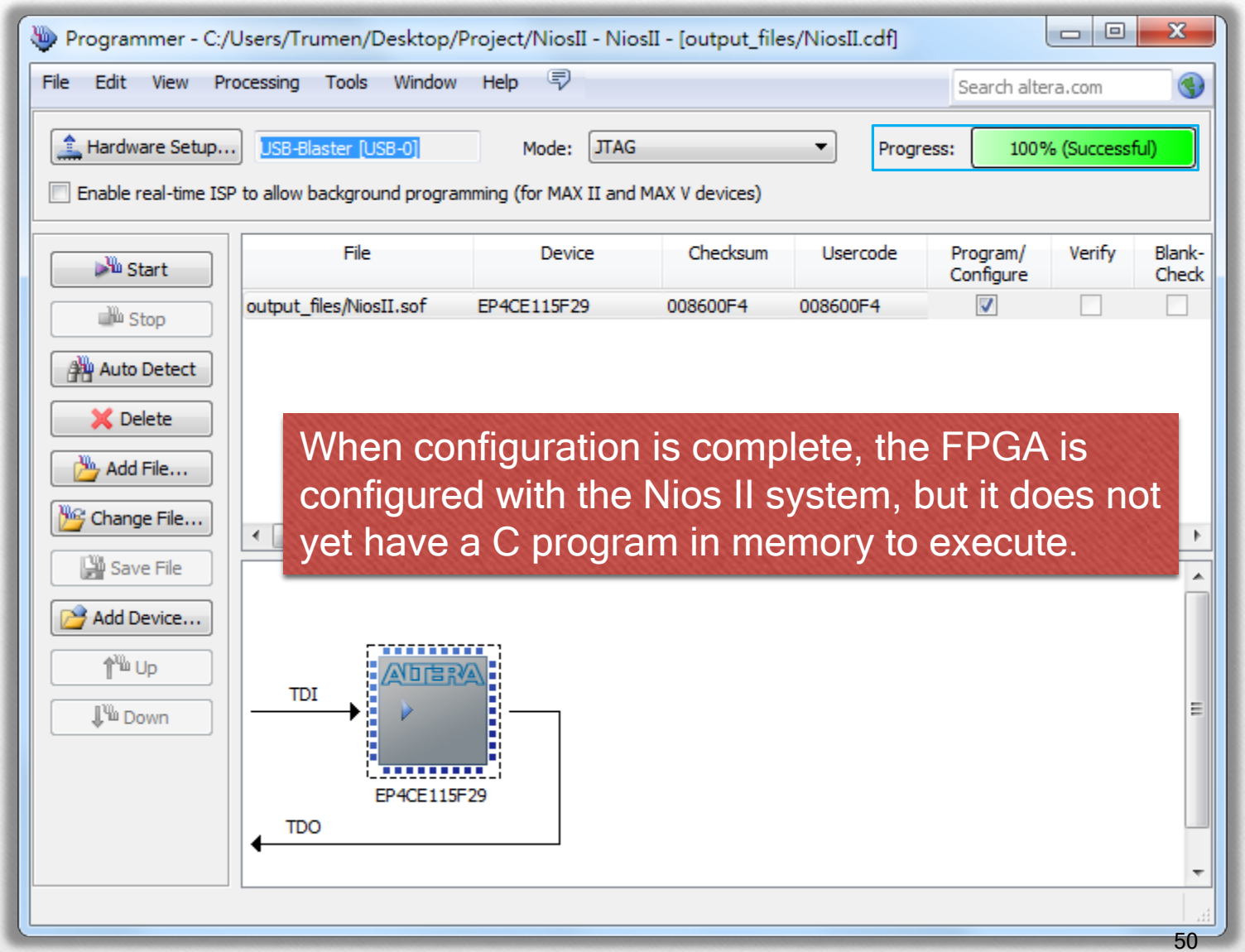

```
create_clock -period 20 [get_ports clk]
derive_clock_uncertainty
set_input_delay 0 -clock clk [all_inputs]
set_output_delay 0 -clock clk [all_outputs]
```


5
Text Editor - C:/Users/Trumen/Desktop/Project/NiosII - NiosII - [Text Editor - C:/Users/Trumen/Desktop/Project/NiosII...
1
File
Edit
View
Project
Processing
Tools
Window
Help
Search altera.com
New File Ctrl+N
Close
Save Ctrl+S
Save As...
2
Create / Update
Page Setup...
Print Preview
Print... Ctrl+P
eriod 20 [get_ports clk]
certainty
0 -clock clk [all_inputs]
y 0 -clock clk [all_outputs]
另存新檔
儲存於(I):
Project
名稱
修改日期
.qsys_edit 2014/2/15 上午 03:01
db 2014/2/15 上午 08:00
DE2_115_QSYS 2014/2/15 上午 05:51
incremental_db 2014/2/15 上午 06:28
output_files 2014/2/15 上午 07:55
最近的位置
桌面
媒體櫃
電腦
網路
4
檔案名稱(N):
NiosII.sdc
3
存檔(S)
存檔類型(T):
Synopsys Design Constraints Files (*.sdc)
取消
Add file to current project
Saves the current file with a new name
0%
00:00:00


Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
File Edit View Project Assignments Processing Tools Window Help
1
Search altera.com
NiosII
Start Compilation
Project Navigator
Files
DE2_115_QSYS/synthesis/DE2_115_QSYS.v
DE2_115_QSYS.qsys
NiosII.v
NiosII.sdc
Hierarchy Files Design Units
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Analysis & Synthesis
Edit Settings
Compilation Report - NiosII
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global Settings
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Elaboration
Flow Messages
Flow Suppressed Messages
Flow Summary
Flow Status
Quartus II 64-Bit Ver
Revision Name
Top-level Entity Name
Family
Device
Timing Models
Total logic elements
Total combinatior
Dedicated logic re
Total registers
Total pins
Total virtual pins
Total memory bits
Embedded Multiplier
All
55
<<Search>>
Type ID Message
12020 Port "jdo" on the entity instantiation of "the_DE2_115_QSYS_nios2_qsys_nios2_oci_i
12241 2 hierarchies have connectivity warnings - see the Connectivity Checks report fold
144001 Generated suppressed messages file C:/Users/Trumen/Desktop/Project/output_files/Ni
Quartus II 64-Bit Analysis & Elaboration was successful. 0 errors, 55 warnings
Messages
System Processing (413)
Starts a new compilation
100%
00:00:44


Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
1
NiosII
Project Navigator
Files
DE2_115_QSYS/synthesis/DE2_115_QSYS.v
DE2_115_QSYS.qsys
NiosII.v
NiosII.sdc
Hierarchy Files Design Units
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Analysis & Synthesis
Edit Settings
Compilation Report - NiosII
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global Settings
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Flow Messages
Flow Suppressed Messages
Assembler
TimeQuest Timing Analyzer
Flow Summary
Flow Status
Quartus II 64-Bit Version
Revision Name
Top-level Entity Name
Family
Device
Timing Models
Total logic elements
Total combinational functic
Dedicated logic registers
Total registers
Total pins
Total virtual pins
Total memory bits
Embedded Multiplier 9-bit elem
All
57
<<Search>>
Type ID Message
332101 Design is fully constrained for setup requirements
332101 Design is fully constrained for hold requirements
Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 0 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 58 warnings
Messages
System
Processing (527)
Opens a Programmer window
100%
00:01:37


Programmer - C:/Users/Trumen/Desktop/Project/NiosII - NiosII - [output_files/NiosII.cdf]
File Edit View Processing Tools Window Help
Search altera.com
Hardware Setup...
USB-Blaster [USB-0]
Mode: JTAG
Progress:
Enable real-time ISP to allow background programming (for MAX II and MAX V devices)
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
output_files/NiosII.sof
EP4CE115F29
008600F4
008600F4
TDI
TDO
EP4CE115F29

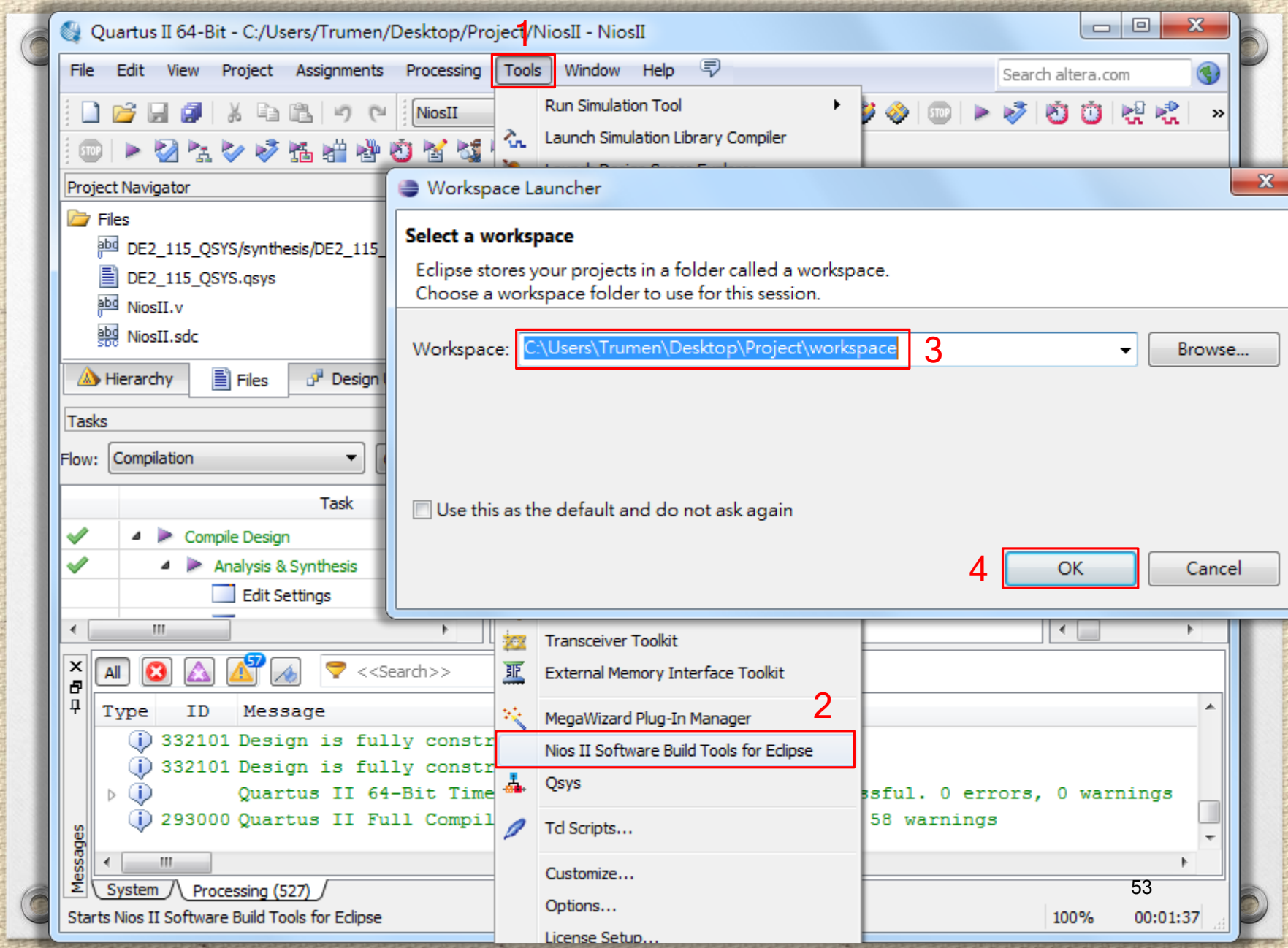

Programmer - C:/Users/Trumen/Desktop/Project/NiosII - NiosII - [output_files/NiosII.cdf]
File Edit View Processing Tools Window Help
Search altera.com
Hardware Setup...
USB-Blaster [USB-0]
Mode: JTAG
Progress: 100% (Successful)
Enable real-time ISP to allow background programming (for MAX II and MAX V devices)
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
output_files/NiosII.sof
EP4CE115F29
008600F4
008600F4
When configuration is complete, the FPGA is configured with the Nios II system, but it does not yet have a C program in memory to execute.
TDI
TDO
EP4CE115F29

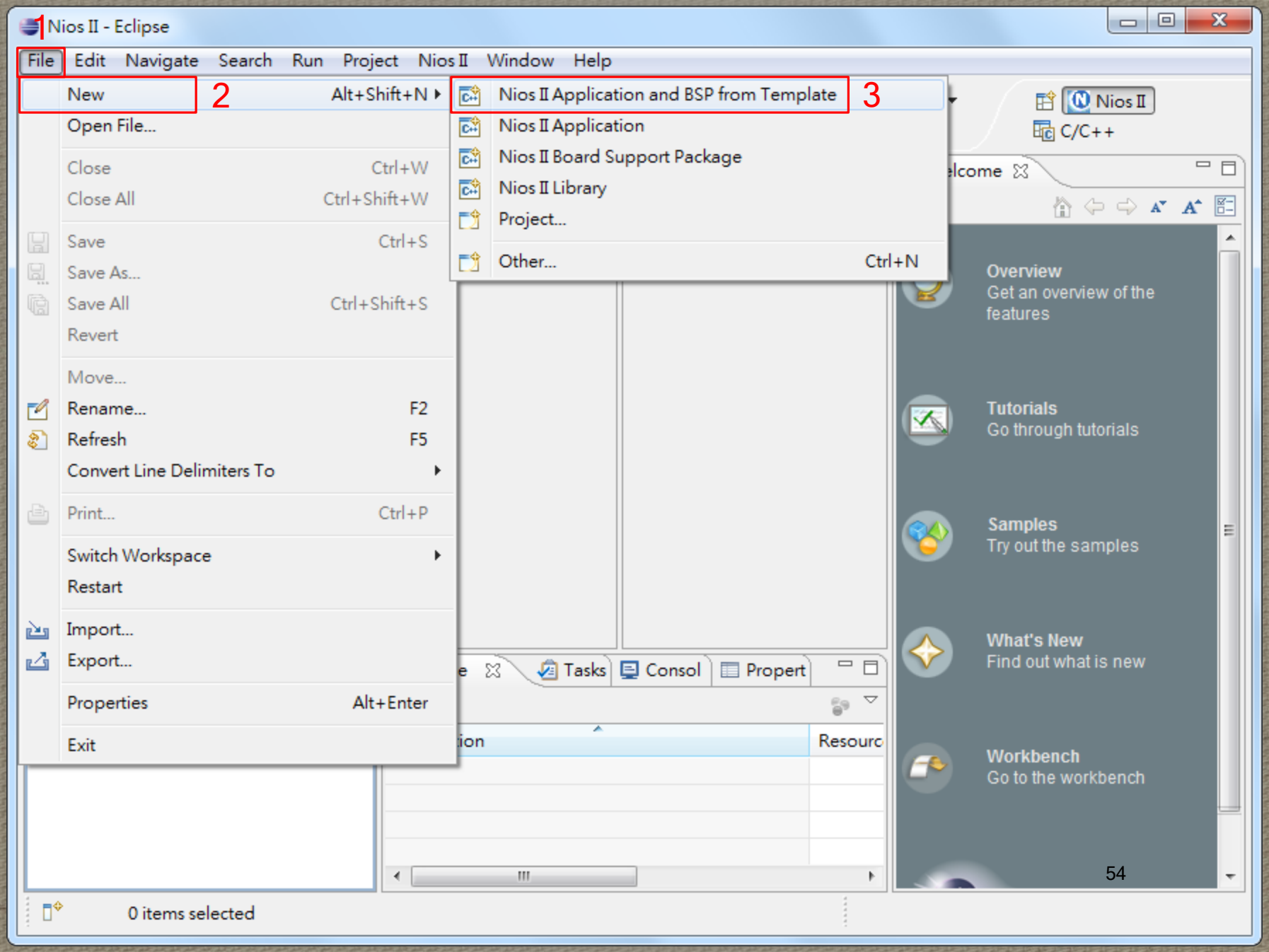
NIOS II IDE Build Flow

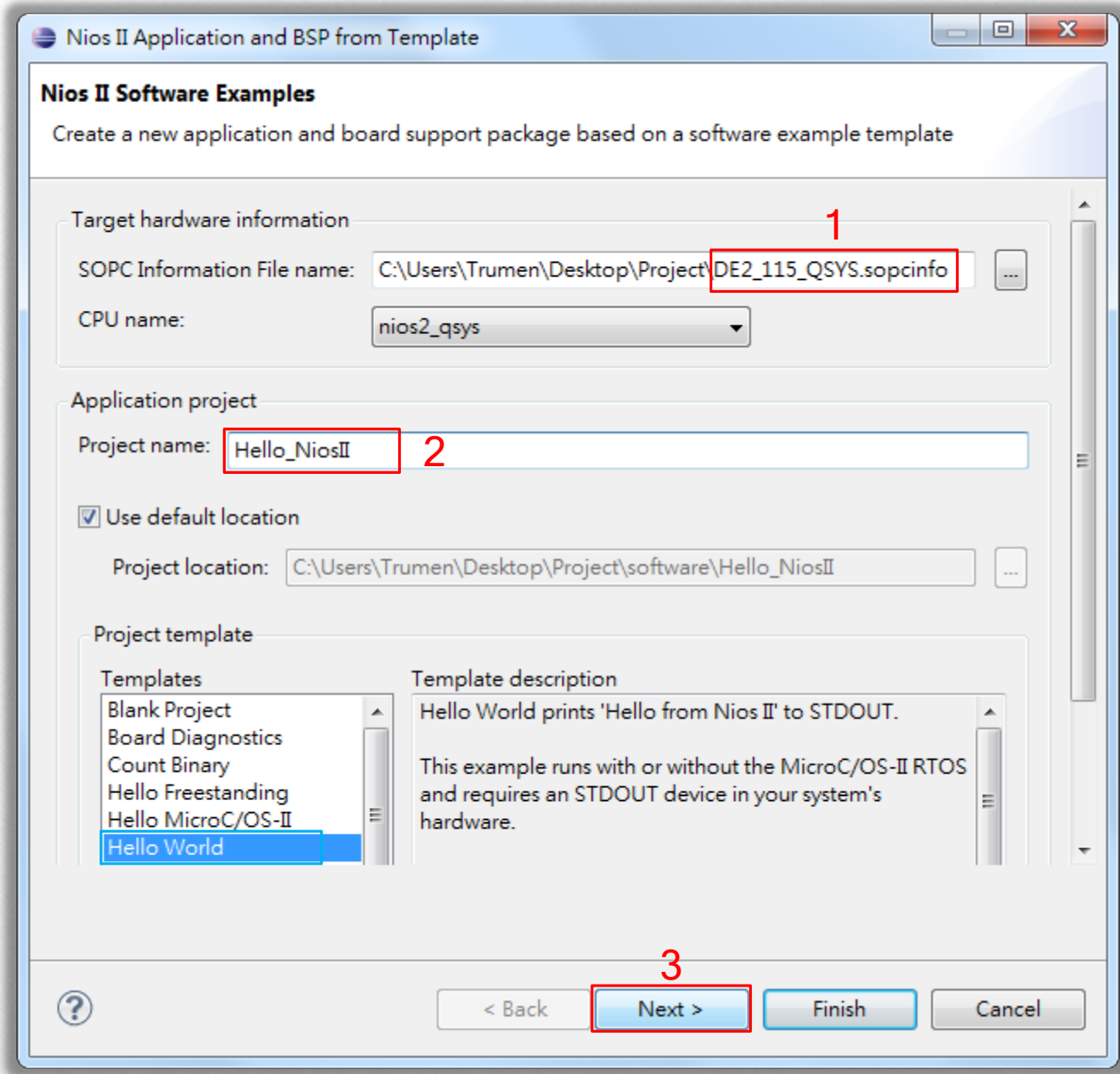
This Chapter covers build flow of Nios II C coded software program.

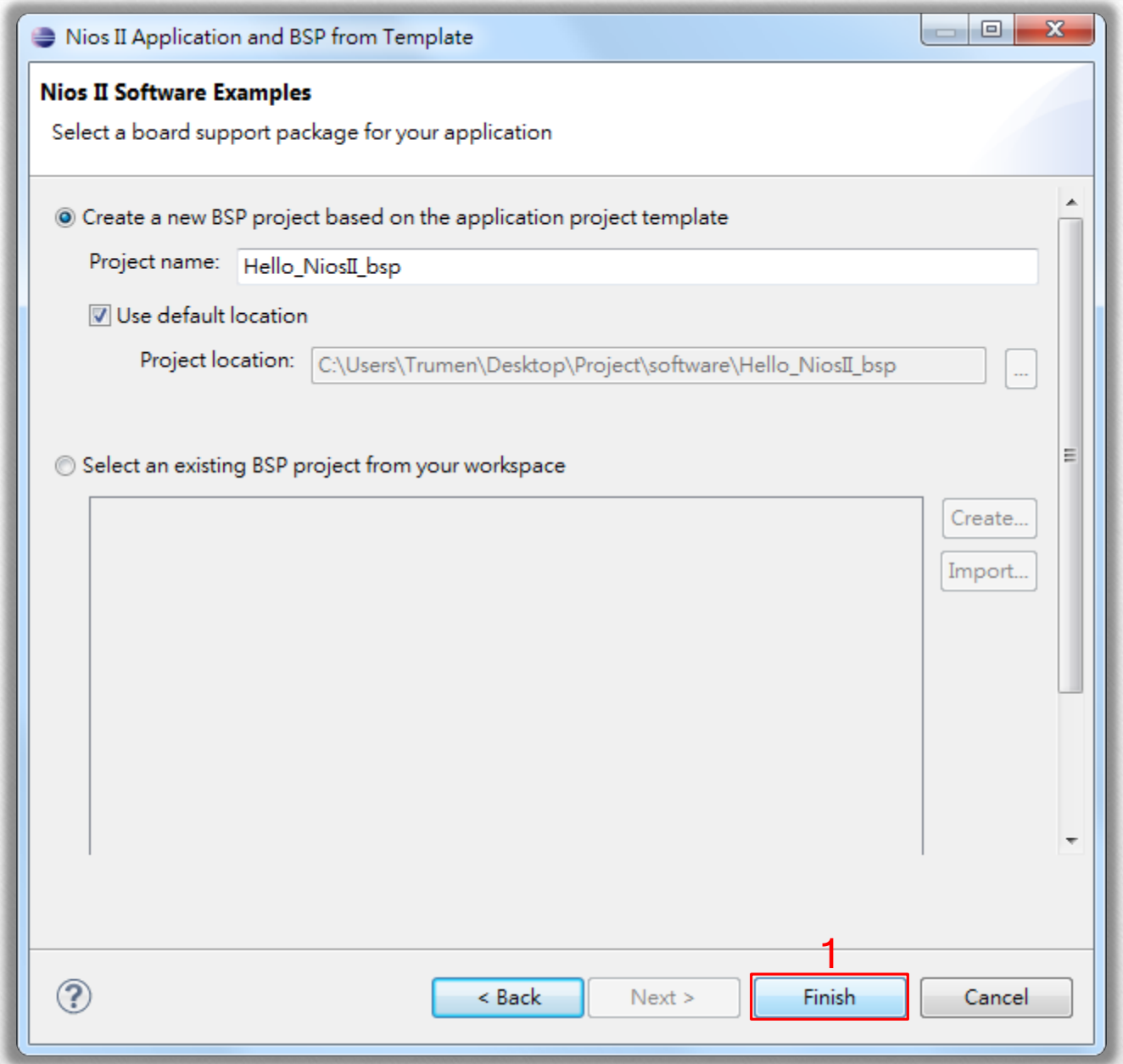
Introduction

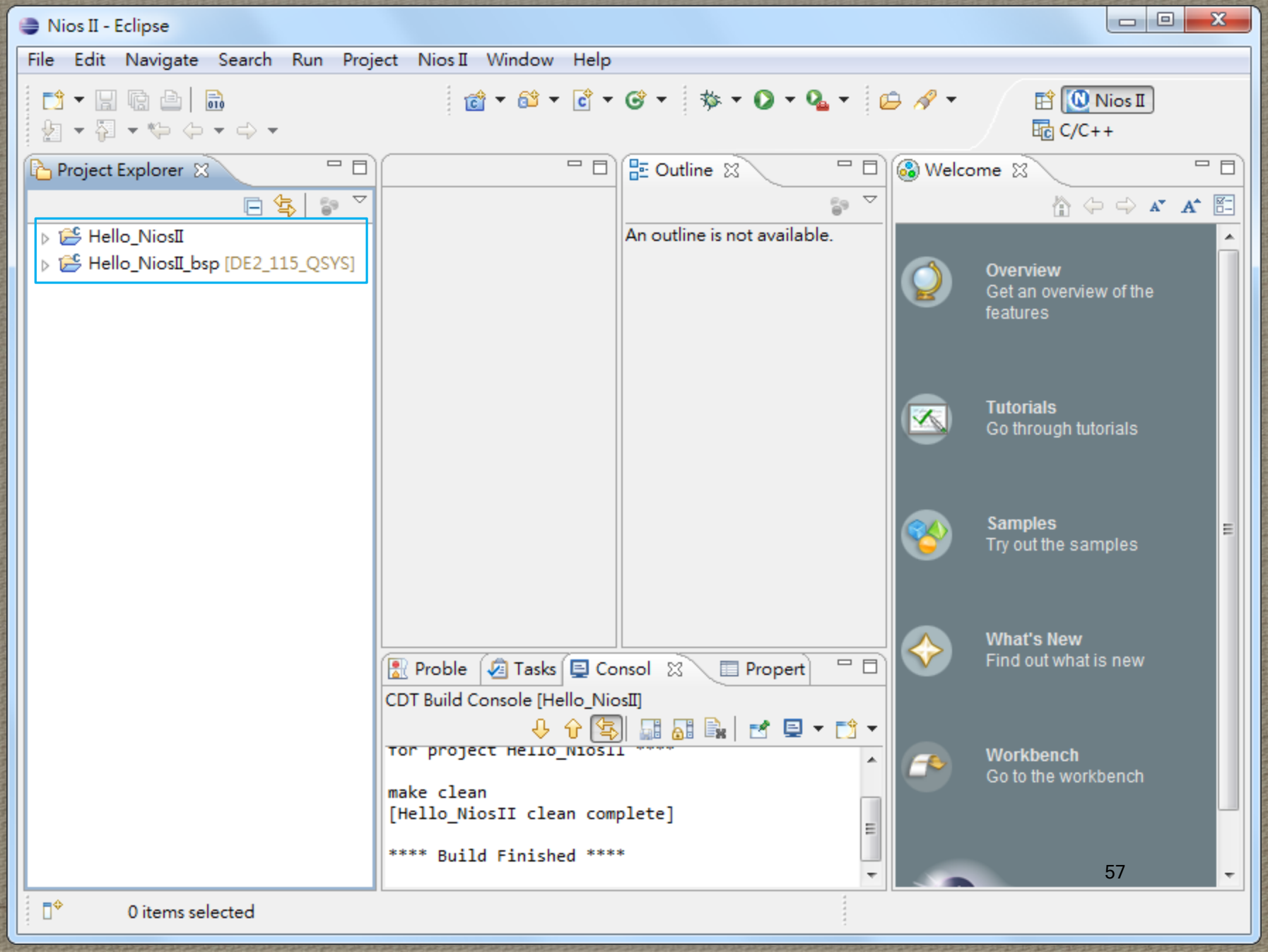
- The Nios II IDE build flow is an easy-to-use graphical user interface (GUI) that automates build and makefile management.
- In this section you will use the Nios II IDE to compile a simple C language example software program to run on the Nios II standard system configured onto the FPGA on your development board.


Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Run Simulation Tool
Launch Simulation Library Compiler
Project Navigator
Files
DE2_115_QSYS/synthesis/DE2_115_
DE2_115_QSYS.qsys
NiosII.v
NiosII.sdc
Hierarchy Files Design
Tasks
Flow: Compilation
Task
Compile Design
Analysis & Synthesis
Edit Settings
Workspace Launcher
Select a workspace
Eclipse stores your projects in a folder called a workspace.
Choose a workspace folder to use for this session.
Workspace: C:\Users\Trumen\Desktop\Project\workspace
3
Browse...
Use this as the default and do not ask again
4
OK
Cancel
Transceiver Toolkit
External Memory Interface Toolkit
MegaWizard Plug-In Manager
2
Nios II Software Build Tools for Eclipse
Qsys
Tcl Scripts...
Customize...
Options...
License Setup...
All
<<Search>>
Type ID Message
332101 Design is fully constr
332101 Design is fully constr
Quartus II 64-Bit Time
293000 Quartus II Full Compil
ssful. 0 errors, 0 warnings
58 warnings
Messages
System Processing (527)
Starts Nios II Software Build Tools for Eclipse
100% 00:01:37


1
Nios II - Eclipse
File
Edit
Navigate
Search
Run
Project
Nios II
Window
Help
New
Alt+Shift+N
2
Open File...
Close
Ctrl+W
Close All
Ctrl+Shift+W
Save
Ctrl+S
Save As...
Save All
Ctrl+Shift+S
Revert
Move...
Rename...
F2
Refresh
F5
Convert Line Delimiters To
Print...
Ctrl+P
Switch Workspace
Restart
Import...
Export...
Properties
Alt+Enter
Exit
Nios II Application and BSP from Template
3
Nios II Application
Nios II Board Support Package
Nios II Library
Project...
Other...
Ctrl+N
Nios II
C/C++
Overview
Get an overview of the features
Tutorials
Go through tutorials
Samples
Try out the samples
What's New
Find out what is new
Workbench
Go to the workbench
Tasks
Consol
Propert
Resourc
0 items selected
54

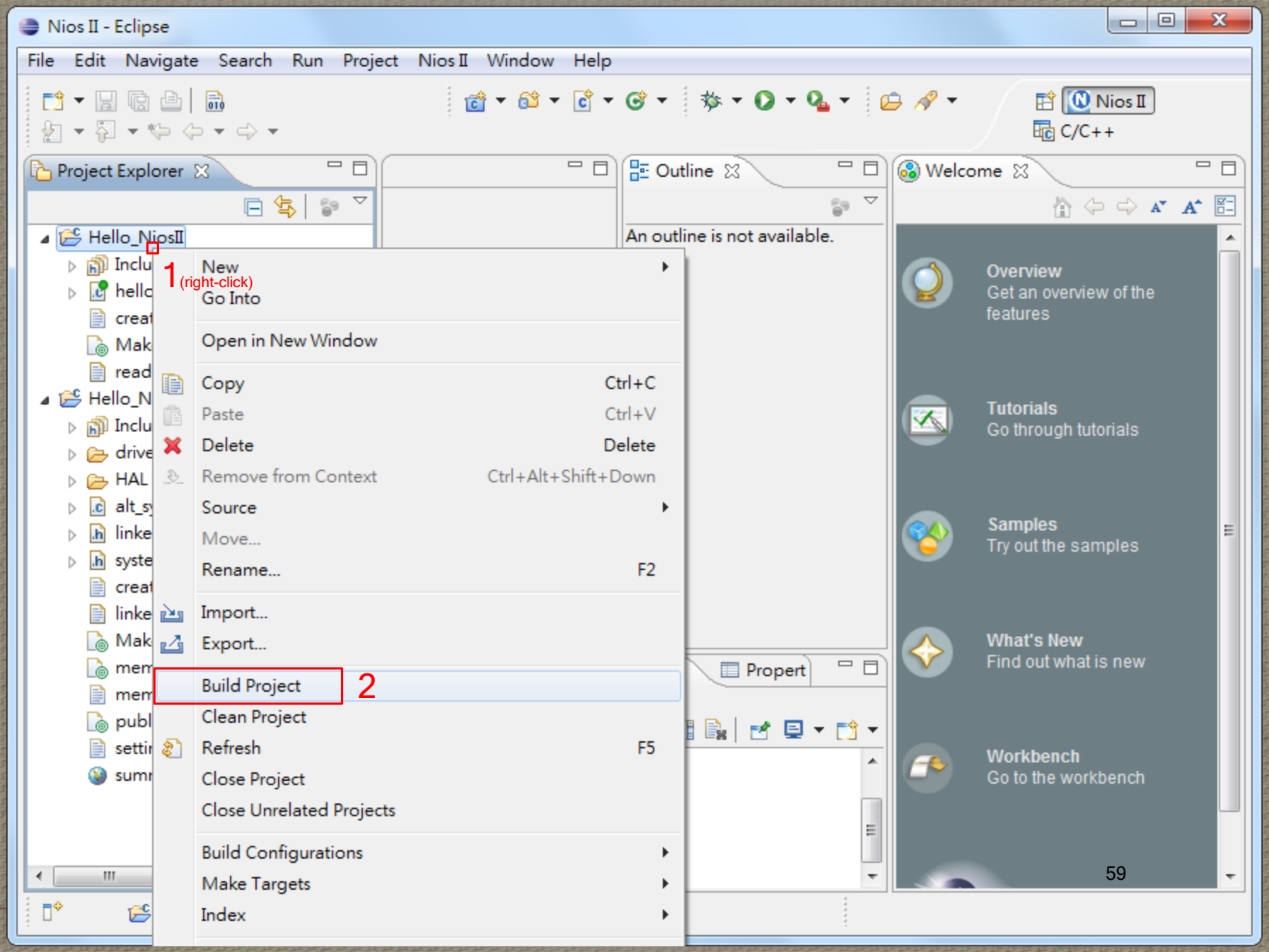

Nios II Application and BSP from Template
Nios II Software Examples
Create a new application and board support package based on a software example template
Target hardware information
1
SOPC Information File name:
C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.sopcinfo
CPU name:
nios2_qsys
Application project
Project name:
Hello_NiosII
2
Use default location
Project location:
C:\Users\Trumen\Desktop\Project\software\Hello_NiosII
Project template
Templates
Blank Project
Board Diagnostics
Count Binary
Hello Freestanding
Hello MicroC/OS-II
Hello World
Template description
Hello World prints 'Hello from Nios II' to STDOUT.
This example runs with or without the MicroC/OS-II RTOS and requires an STDOUT device in your system's hardware.
3
< Back
Next >
Finish
Cancel

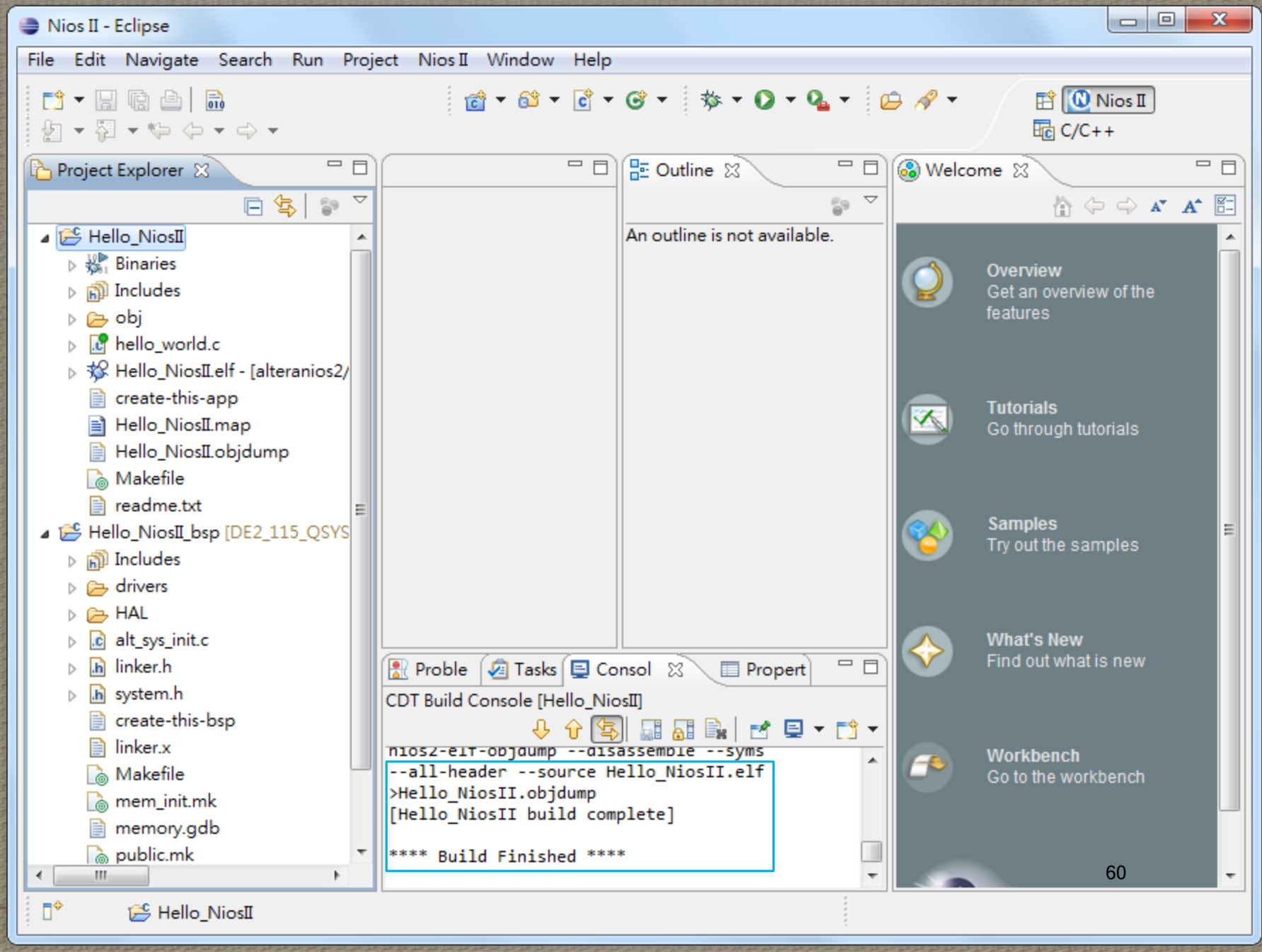

Nios II Application and BSP from Template
Nios II Software Examples
Select a board support package for your application
Create a new BSP project based on the application project template
Project name:
Hello_NiosII_bsp
Use default location
Project location:
C:\Users\Trumen\Desktop\Project\software\Hello_NiosII_bsp
...
Select an existing BSP project from your workspace
Create...
Import...
1
< Back
Next >
Finish
Cancel


Nios II - Eclipse
File Edit Navigate Search Run Project Nios II Window Help
Nios II
C/C++
Project Explorer
Hello_NiosII
Hello_NiosII_bsp [DE2_115_QSYS]
Outline
An outline is not available.
Welcome
Overview
Get an overview of the features
Tutorials
Go through tutorials
Samples
Try out the samples
What's New
Find out what is new
Workbench
Go to the workbench
Proble
Tasks
Consol
Propert
CDT Build Console [Hello_NiosII]
for project Hello_NiosII ****
make clean
[Hello_NiosII clean complete]
**** Build Finished ****
0 items selected

Project Description

- When you create a new project, the NIOS II SBT for Eclipse creates two new projects in the NIOS II C/C++ Projects tab:
  - **Hello_NiosII** is your C/C++ application project. This project contains the source and header files for your application.
  - **Hello_NiosII_bsp** is a board support package that encapsulates the details of the Nios II system hardware.


Nios II - Eclipse
File Edit Navigate Search Run Project Nios II Window Help
Nios II
C/C++
Project Explorer
Hello_NiosII
Outline
An outline is not available.
Welcome
Overview
Get an overview of the features
Tutorials
Go through tutorials
Samples
Try out the samples
What's New
Find out what is new
Workbench
Go to the workbench
1 (right-click)
New
Go Into
Open in New Window
Copy Ctrl+C
Paste Ctrl+V
Delete Delete
Remove from Context Ctrl+Alt+Shift+Down
Source
Move...
Rename... F2
Import...
Export...
Build Project
2
Clean Project
Refresh F5
Close Project
Close Unrelated Projects
Build Configurations
Make Targets
Index
59


Nios II - Eclipse
File Edit Navigate Search Run Project Nios II Window Help
Nios II
C/C++
Project Explorer
Hello_NiosII
Binaries
Includes
obj
hello_world.c
Hello_NiosII.elf - [alteranios2/
create-this-app
Hello_NiosII.map
Hello_NiosII.objdump
Makefile
readme.txt
Hello_NiosII_bsp [DE2_115_QSYS
Includes
drivers
HAL
alt_sys_init.c
linker.h
system.h
create-this-bsp
linker.x
Makefile
mem_init.mk
memory.gdb
public.mk
Outline
An outline is not available.
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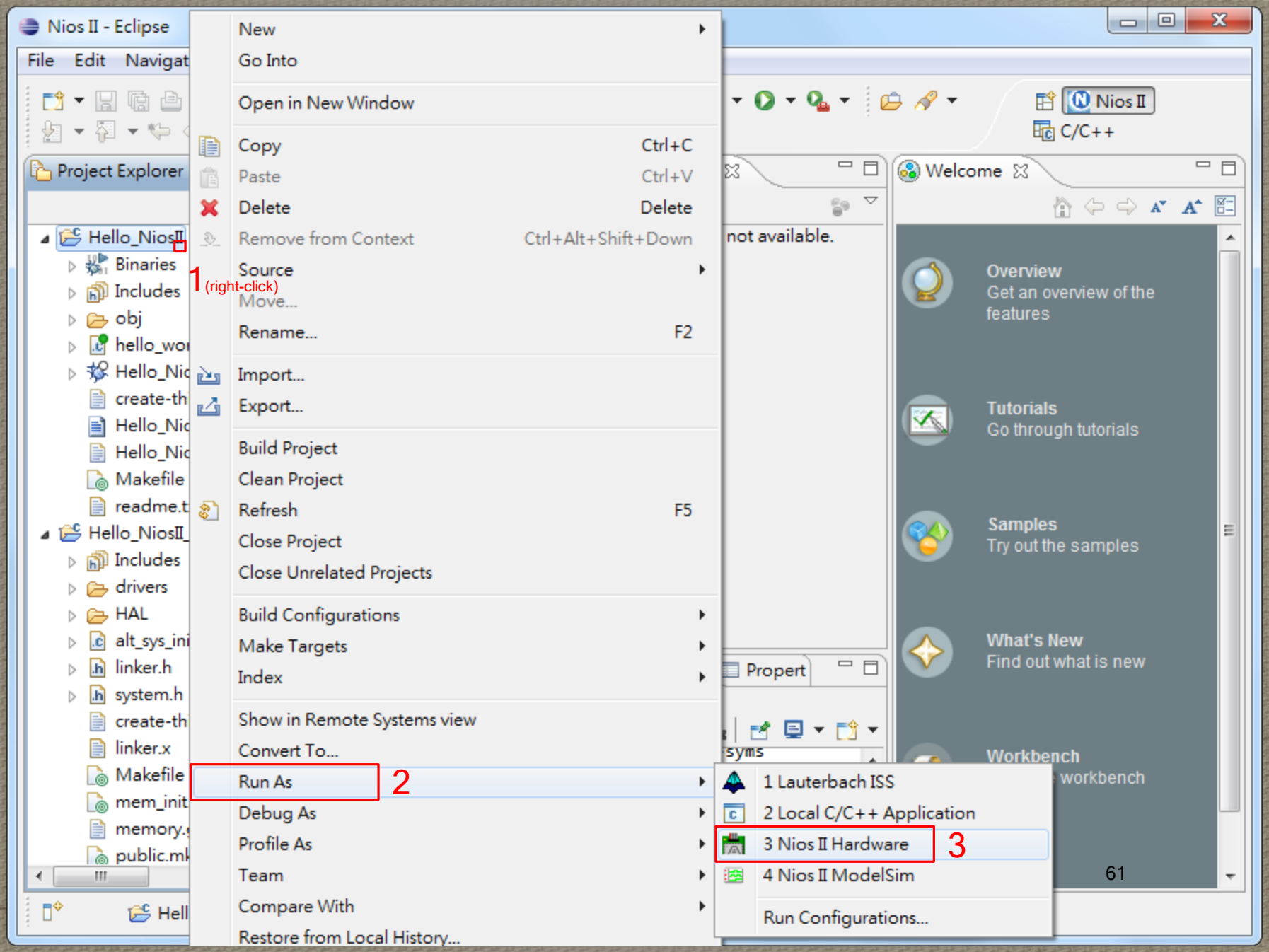
Go through tutorials
Samples
Try out the samples
What's New
Find out what is new
Workbench
Go to the workbench
Proble
Tasks
Consol
Propert
CDT Build Console [Hello_NiosII]
nios2-elf-objdump --disassemble --syms
--all-header --source Hello_NiosII.elf
>Hello_NiosII.objdump
[Hello_NiosII build complete]
**** Build Finished ****
Hello_NiosII


Nios II - Eclipse
File Edit Navigat
Project Explorer
Hello_NiosII
Binaries
Includes
obj
Hello_NiosII_
drivers
HAL
linker.h
system.h
linker.x
Makefile
mem_init
public.mk
1 (right-click)
New
Go Into
Open in New Window
Copy Ctrl+C
Paste Ctrl+V
Delete Delete
Remove from Context Ctrl+Alt+Shift+Down
Source
Move...
Rename... F2
Import...
Export...
Build Project
Clean Project
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Close Project
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Convert To...
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Team
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Restore from Local History...
2
1 Lauterbach ISS
2 Local C/C++ Application
3 Nios II Hardware
4 Nios II ModelSim
Run Configurations...
3
Nios II
C/C++
Welcome
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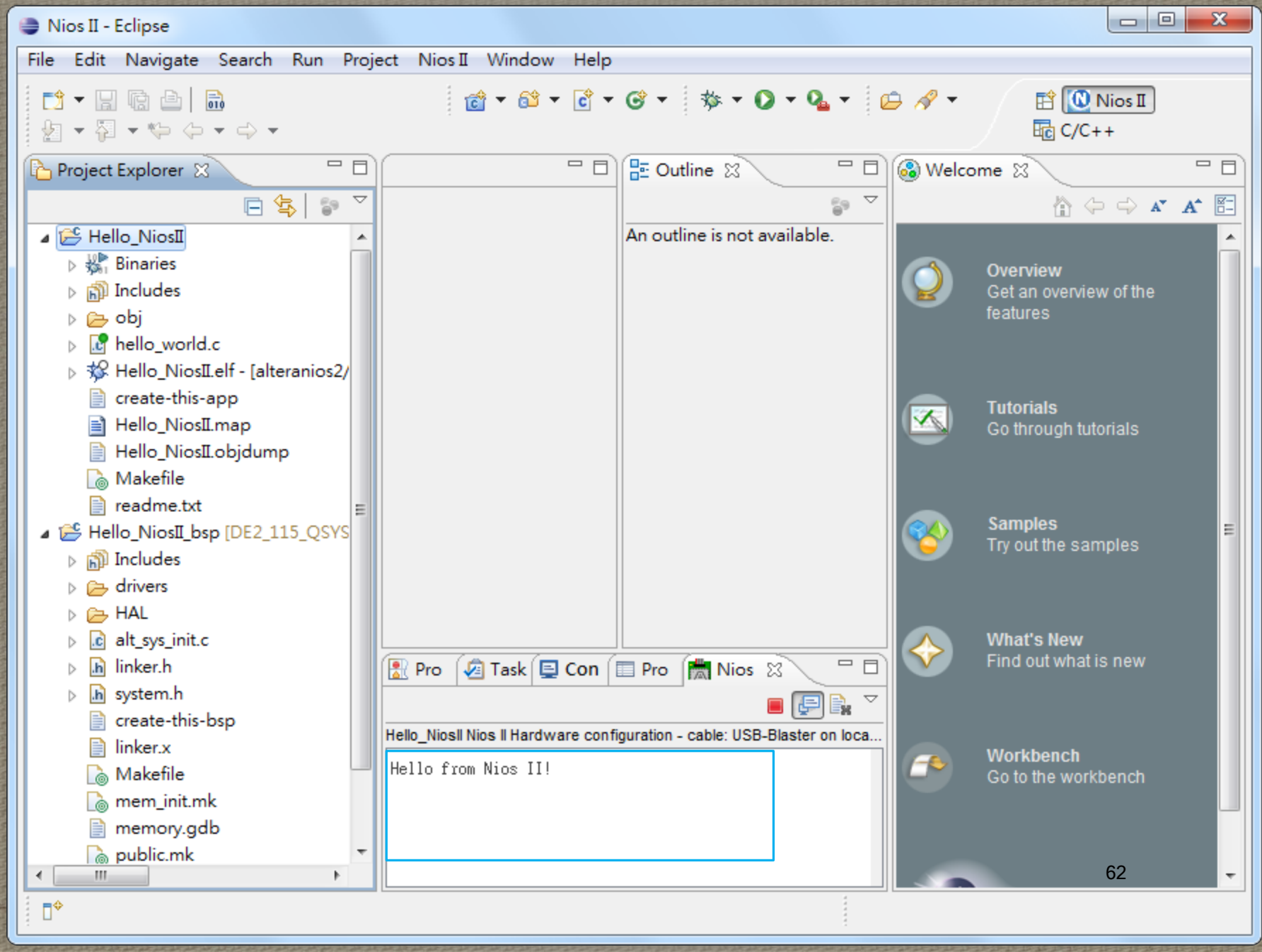
Get an overview of the features
Tutorials
Go through tutorials
Samples
Try out the samples
What's New
Find out what is new
Workbench
workbench
not available.
Propert
61


Nios II - Eclipse
File Edit Navigate Search Run Project Nios II Window Help
Nios II
C/C++
Project Explorer
Hello_NiosII
Binaries
Includes
obj
hello_world.c
Hello_NiosII.elf - [alteranios2/
create-this-app
Hello_NiosII.map
Hello_NiosII.objdump
Makefile
readme.txt
Hello_NiosII_bsp [DE2_115_QSYS
Includes
drivers
HAL
alt_sys_init.c
linker.h
system.h
create-this-bsp
linker.x
Makefile
mem_init.mk
memory.gdb
public.mk
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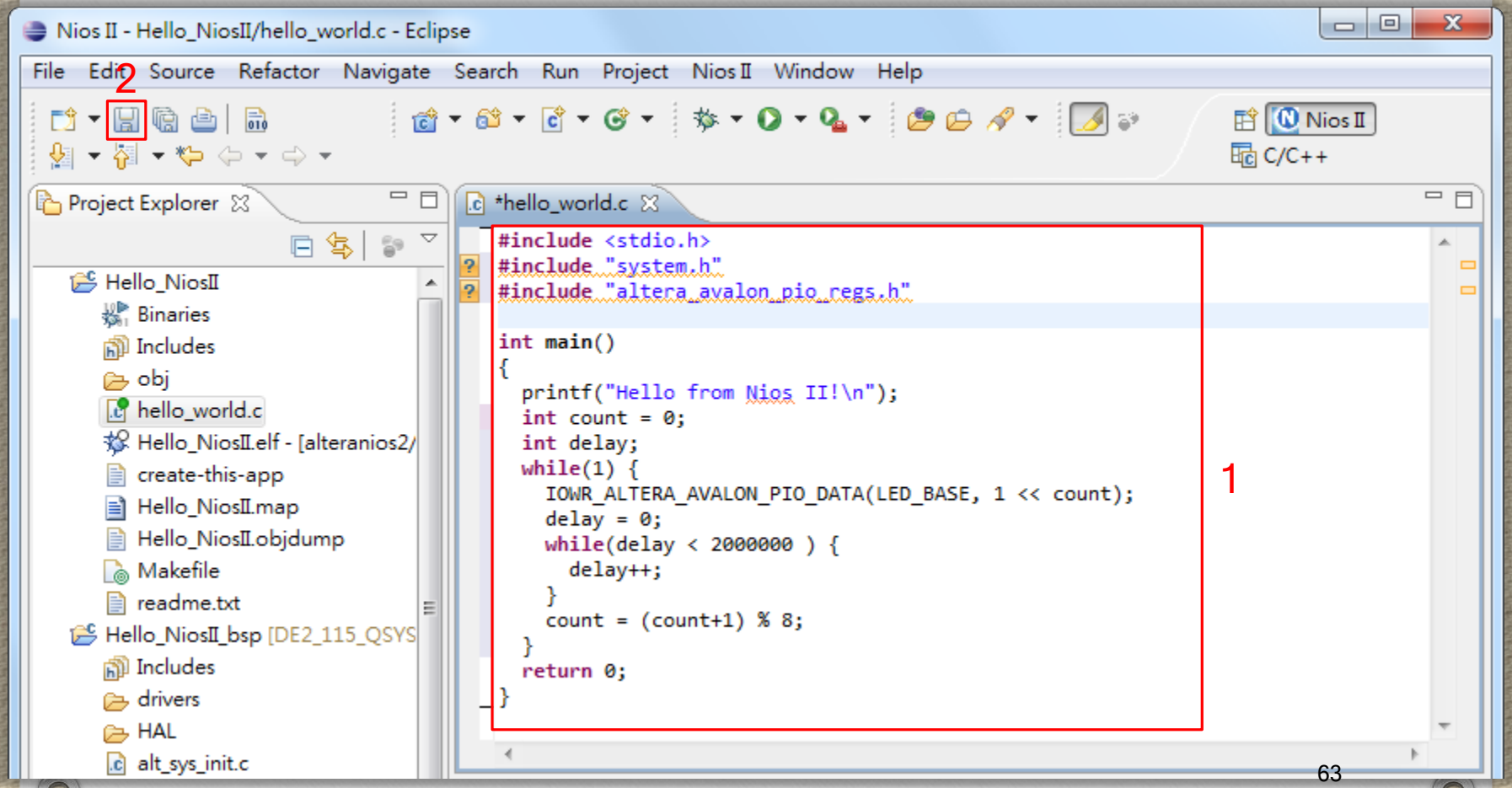
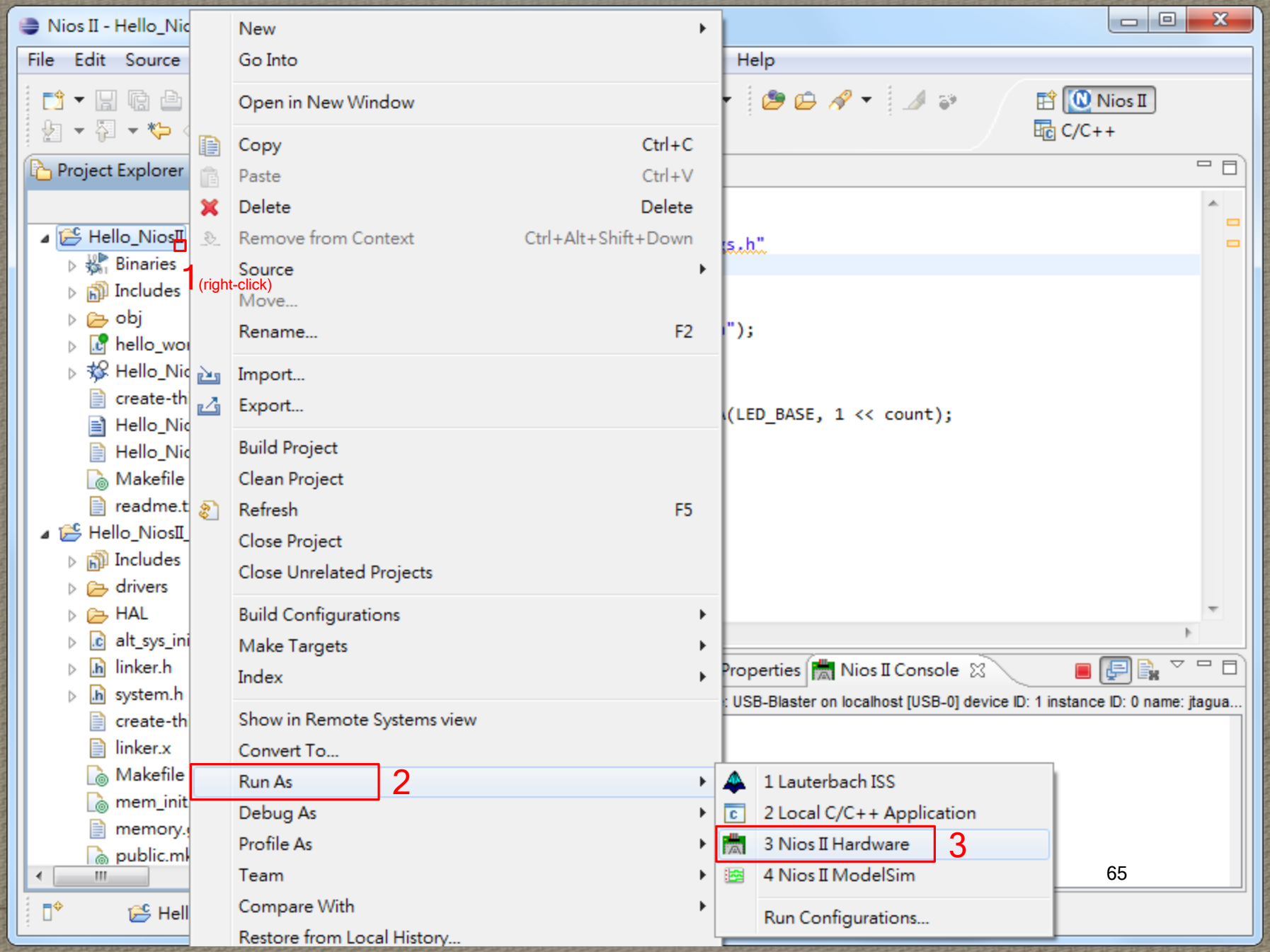
Tutorials
Go through tutorials
Samples
Try out the samples
What's New
Find out what is new
Workbench
Go to the workbench
Pro
Task
Con
Pro
Nios
Hello_NiosII Nios II Hardware configuration - cable: USB-Blaster on loca...
Hello from Nios II!

Edit and Re-Run the Program



```c
#include <stdio.h>
#include "system.h"
#include "altera_avalon_pio_regs.h"

int main()
{
  printf("Hello from Nios II!\n");
  int count = 0;
  int delay;
  while(1) {
    IOWR_ALTERA_AVALON_PIO_DATA(LED_BASE, 1 << count);
    delay = 0;
    while(delay < 2000000 ) {
      delay++;
    }
    count = (count+1) % 8;
  }
  return 0;
}
```


Nios II - Hello_Nic
File Edit Source
Help
Nios II
C/C++
Project Explorer
Hello_NiosII
Binaries
Includes
obj
Makefile
readme.t
Hello_NiosII_
drivers
HAL
linker.h
system.h
linker.x
public.mk
1
(right-click)
New
Go Into
Open in New Window
Copy Ctrl+C
Paste Ctrl+V
Delete Delete
Remove from Context Ctrl+Alt+Shift+Down
Source
Move...
Rename... F2
Import...
Export...
Build Project
Clean Project
Refresh F5
Close Project
Close Unrelated Projects
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Convert To...
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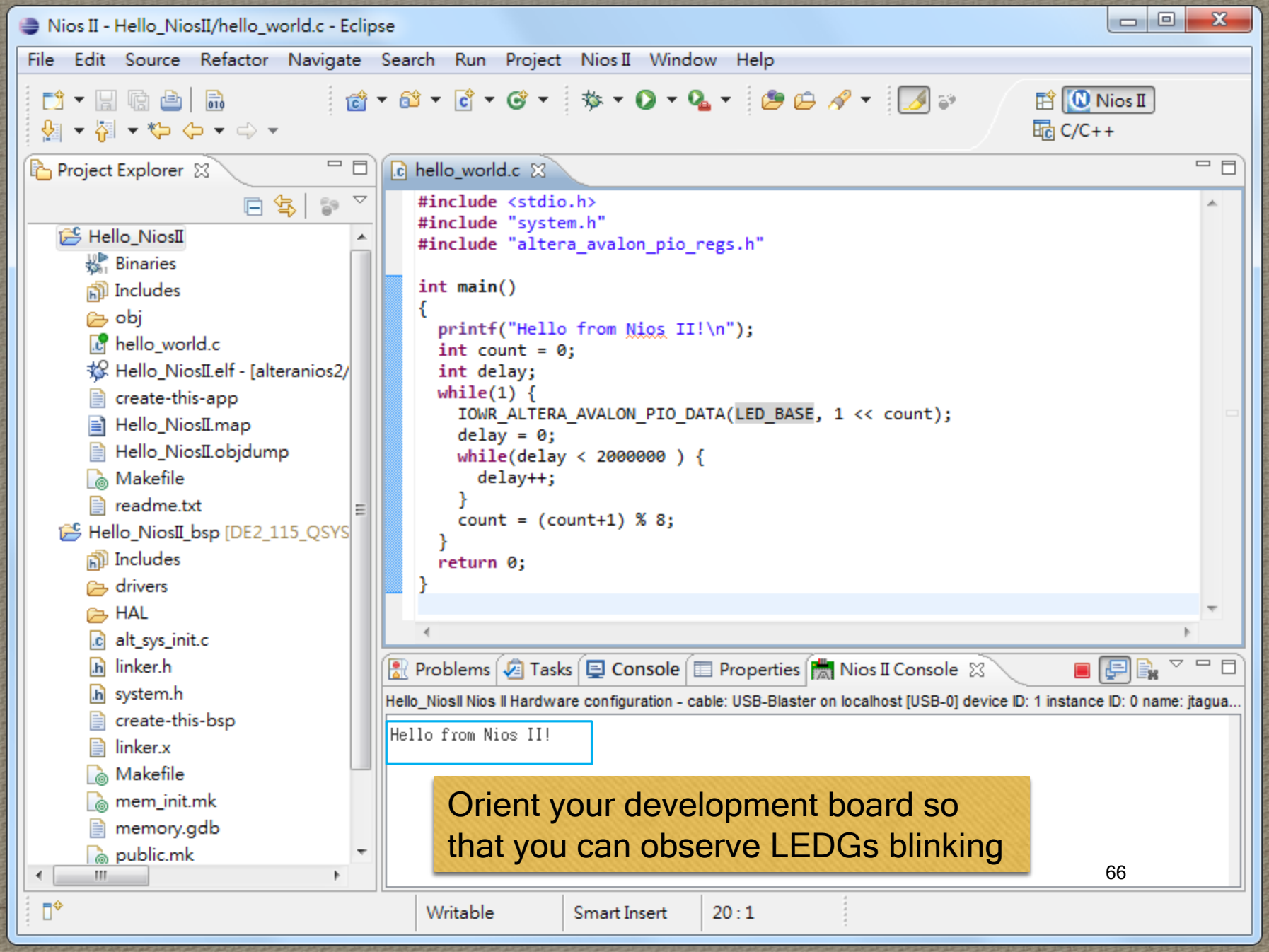
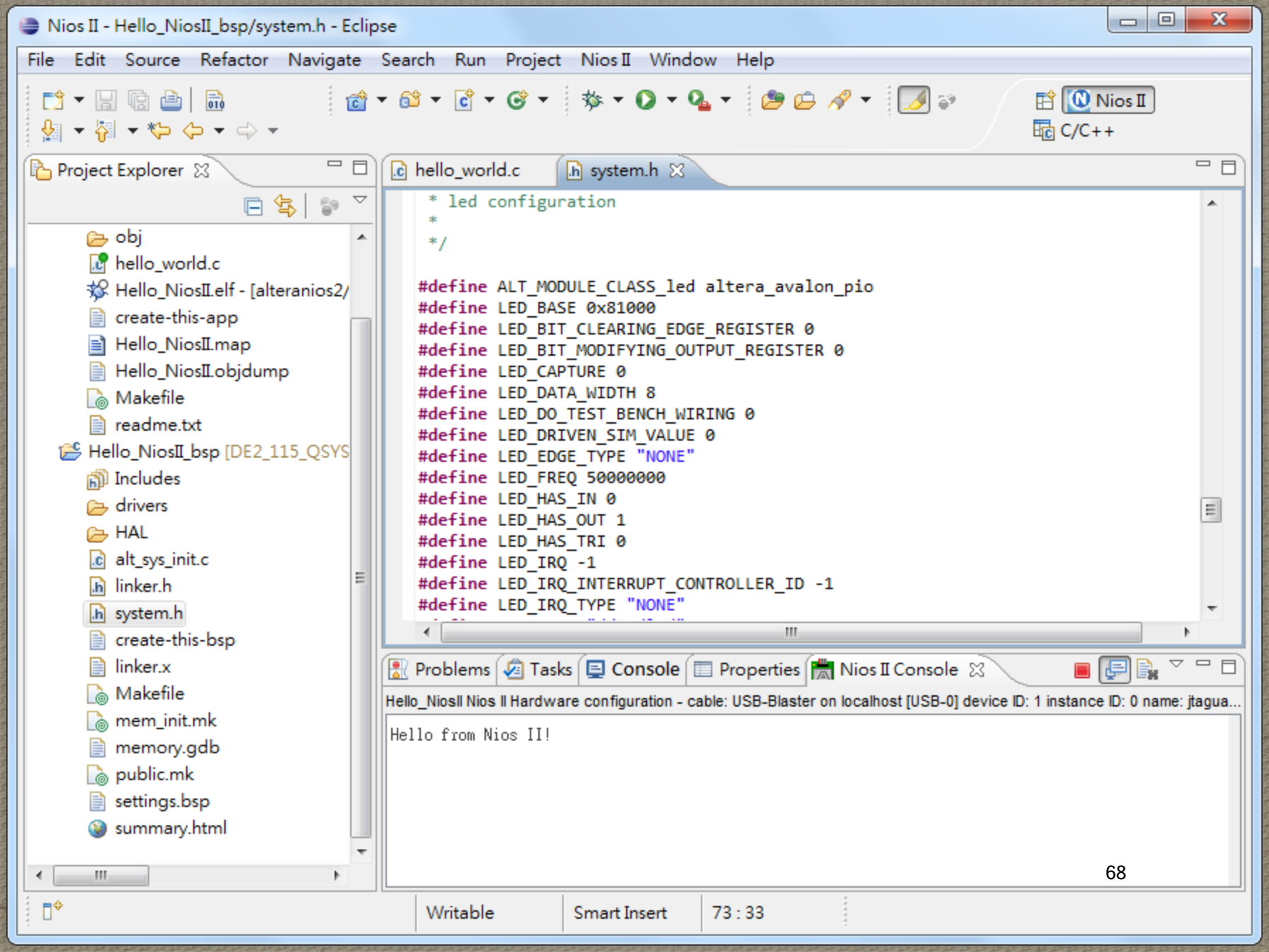
Restore from Local History...
2
1 Lauterbach ISS
2 Local C/C++ Application
3 Nios II Hardware
4 Nios II ModelSim
Run Configurations...
3
(LED_BASE, 1 << count);
Properties
Nios II Console
USB-Blaster on localhost [USB-0] device ID: 1 instance ID: 0 name: jtagua...
65


Nios II - Hello_NiosII/hello_world.c - Eclipse
File Edit Source Refactor Navigate Search Run Project Nios II Window Help
Nios II
C/C++
Project Explorer
Hello_NiosII
Binaries
Includes
obj
hello_world.c
Hello_NiosII.elf - [alteranios2/
create-this-app
Hello_NiosII.map
Hello_NiosII.objdump
Makefile
readme.txt
Hello_NiosII_bsp [DE2_115_QSYS
Includes
drivers
HAL
alt_sys_init.c
linker.h
system.h
create-this-bsp
linker.x
Makefile
mem_init.mk
memory.gdb
public.mk
hello_world.c
#include <stdio.h>
#include "system.h"
#include "altera_avalon_pio_regs.h"
int main()
{
printf("Hello from Nios II!\n");
int count = 0;
int delay;
while(1) {
IOWR_ALTERA_AVALON_PIO_DATA(LED_BASE, 1 << count);
delay = 0;
while(delay < 2000000) {
delay++;
}
count = (count+1) % 8;
}
return 0;
}
Problems Tasks Console Properties Nios II Console
Hello_NiosII Nios II Hardware configuration - cable: USB-Blaster on localhost [USB-0] device ID: 1 instance ID: 0 name: jtagua...
Hello from Nios II!
Orient your development board so that you can observe LEDGs blinking
Writable
Smart Insert
20 : 1

Why the LEDs Blink? (1/2)

- The Nios II system description header file, system.h, contains the software definitions, name, locations, base addresses, and settings for all of the components in the Nios II hardware system.
- The system.h file is located in the in the Hello_NiosII_bsp directory.


Nios II - Hello_NiosII_bsp/system.h - Eclipse
File Edit Source Refactor Navigate Search Run Project Nios II Window Help
Nios II
C/C++
Project Explorer
obj
hello_world.c
Hello_NiosII.elf - [alteranios2/
create-this-app
Hello_NiosII.map
Hello_NiosII.objdump
Makefile
readme.txt
Hello_NiosII_bsp [DE2_115_QSYS
Includes
drivers
HAL
alt_sys_init.c
linker.h
system.h
create-this-bsp
linker.x
Makefile
mem_init.mk
memory.gdb
public.mk
settings.bsp
summary.html
hello_world.c
system.h
* led configuration
*
*/
#define ALT_MODULE_CLASS_led altera_avalon_pio
#define LED_BASE 0x81000
#define LED_BIT_CLEARING_EDGE_REGISTER 0
#define LED_BIT_MODIFYING_OUTPUT_REGISTER 0
#define LED_CAPTURE 0
#define LED_DATA_WIDTH 8
#define LED_DO_TEST_BENCH_WIRING 0
#define LED_DRIVEN_SIM_VALUE 0
#define LED_EDGE_TYPE "NONE"
#define LED_FREQ 50000000
#define LED_HAS_IN 0
#define LED_HAS_OUT 1
#define LED_HAS_TRI 0
#define LED_IRQ -1
#define LED_IRQ_INTERRUPT_CONTROLLER_ID -1
#define LED_IRQ_TYPE "NONE"
Problems Tasks Console Properties Nios II Console
Hello_NiosII Nios II Hardware configuration - cable: USB-Blaster on localhost [USB-0] device ID: 1 instance ID: 0 name: jtagua...
Hello from Nios II!
Writable
Smart Insert
73 : 33

Why the LED Blinks? (2/2)

- The Nios II processor controls the PIO ports (and thereby the LED) by reading and writing to the register map.
- For the PIO, there are four registers: data, direction, interrupt mask, and edge capture.
- To turn the LED on and off, the application writes to the PIO data register.

Register Map File (1/2)

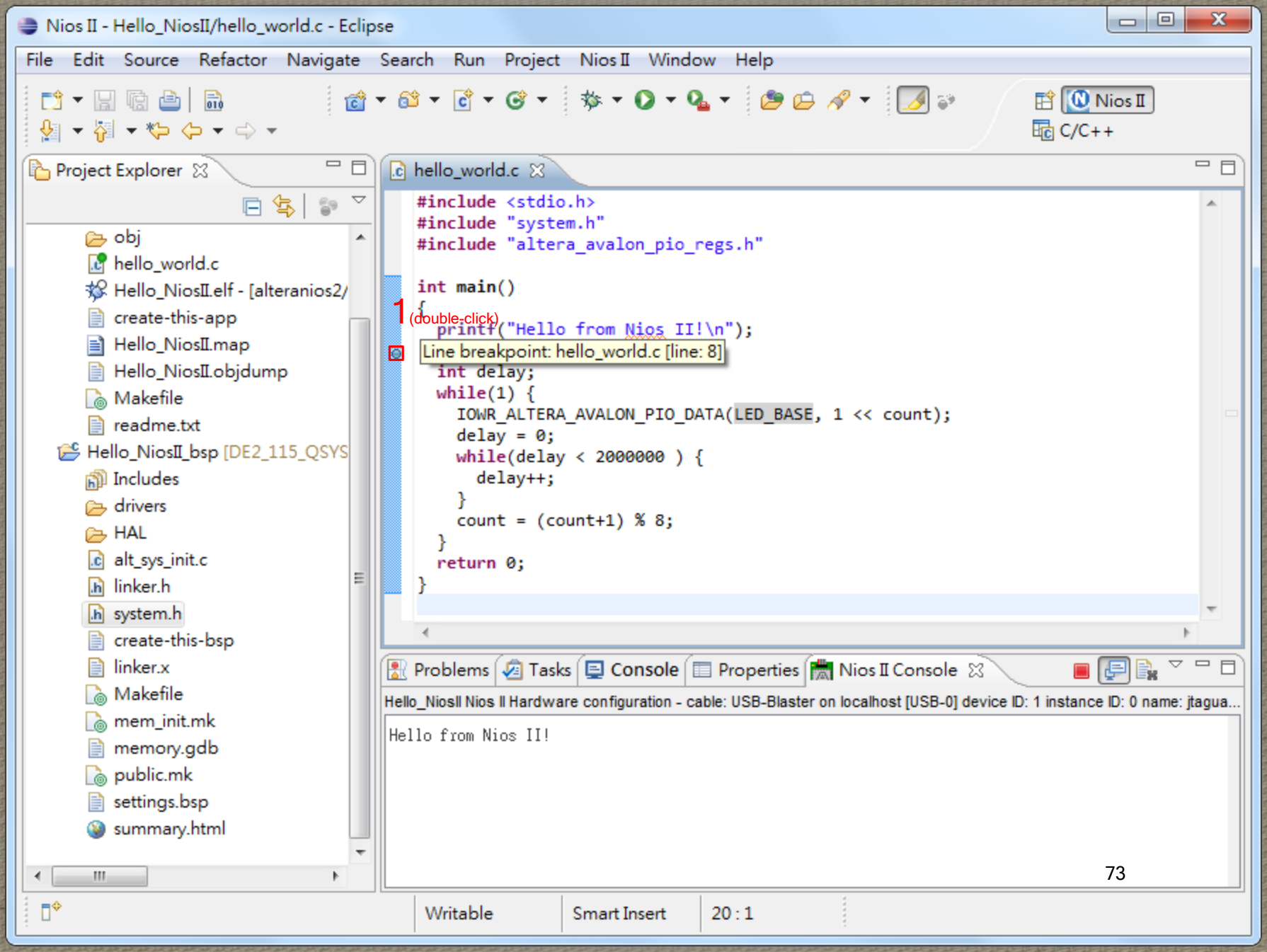
- The PIO core has an associated software file altera_avalon_pio_regs.h.
  - This file defines the core's register map, providing symbolic constants to access the low-level hardware.
  - This file is located in Project\software\Hello_NiosII_bsp\drivers\inc\.

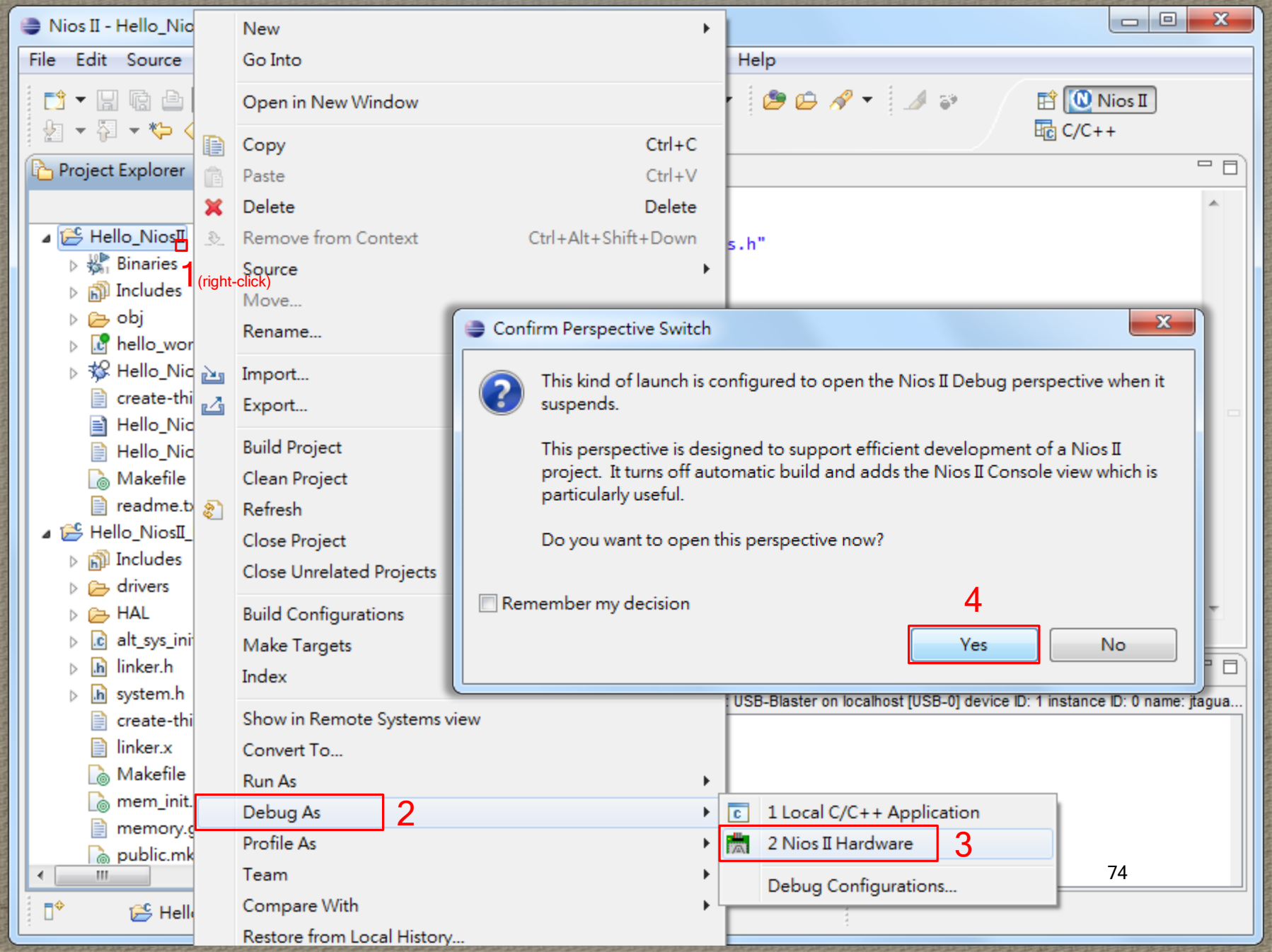
Register Map File (2/2)

- When you include this file, several useful functions that manipulate the PIO core registers are available to your program.
- In particular, the function IOWR_ALTERA_AVALON_PIO_DATA (base, data) can write to the PIO data register, turning the LED on and off.
- The PIO is just one of many SOPC peripherals that you can use in a system.

Debugging the Application

- Before you can debug a project in the NIOS II SBT for Eclipse, you need to create a debug configuration that specifies how to run the software.


Nios II - Hello_NiosII/hello_world.c - Eclipse
File Edit Source Refactor Navigate Search Run Project Nios II Window Help
Nios II
C/C++
Project Explorer
obj
hello_world.c
Hello_NiosII.elf - [alteranios2/
create-this-app
Hello_NiosII.map
Hello_NiosII.objdump
Makefile
readme.txt
Hello_NiosII_bsp [DE2_115_QSYS
Includes
drivers
HAL
alt_sys_init.c
linker.h
system.h
create-this-bsp
linker.x
Makefile
mem_init.mk
memory.gdb
public.mk
settings.bsp
summary.html
hello_world.c
#include <stdio.h>
#include "system.h"
#include "altera_avalon_pio_regs.h"
int main()
{
1
(double-click)
printf("Hello from Nios II!\n");
Line breakpoint: hello_world.c [line: 8]
int delay;
while(1) {
IOWR_ALTERA_AVALON_PIO_DATA(LED_BASE, 1 << count);
delay = 0;
while(delay < 2000000) {
delay++;
}
count = (count+1) % 8;
}
return 0;
}
Problems
Tasks
Console
Properties
Nios II Console
Hello_NiosII Nios II Hardware configuration - cable: USB-Blaster on localhost [USB-0] device ID: 1 instance ID: 0 name: jtagua...
Hello from Nios II!
Writable
Smart Insert
20 : 1


Nios II - Hello_Nio
File Edit Source
Help
Nios II
C/C++
Project Explorer
Hello_NiosII
Binaries
Includes
obj
Makefile
Hello_NiosII_
drivers
HAL
linker.h
system.h
linker.x
mem_init.
public.mk
1
(right-click)
New
Go Into
Open in New Window
Copy Ctrl+C
Paste Ctrl+V
Delete Delete
Remove from Context Ctrl+Alt+Shift+Down
Source
Move...
Rename...
Import...
Export...
Build Project
Clean Project
Refresh
Close Project
Close Unrelated Projects
Build Configurations
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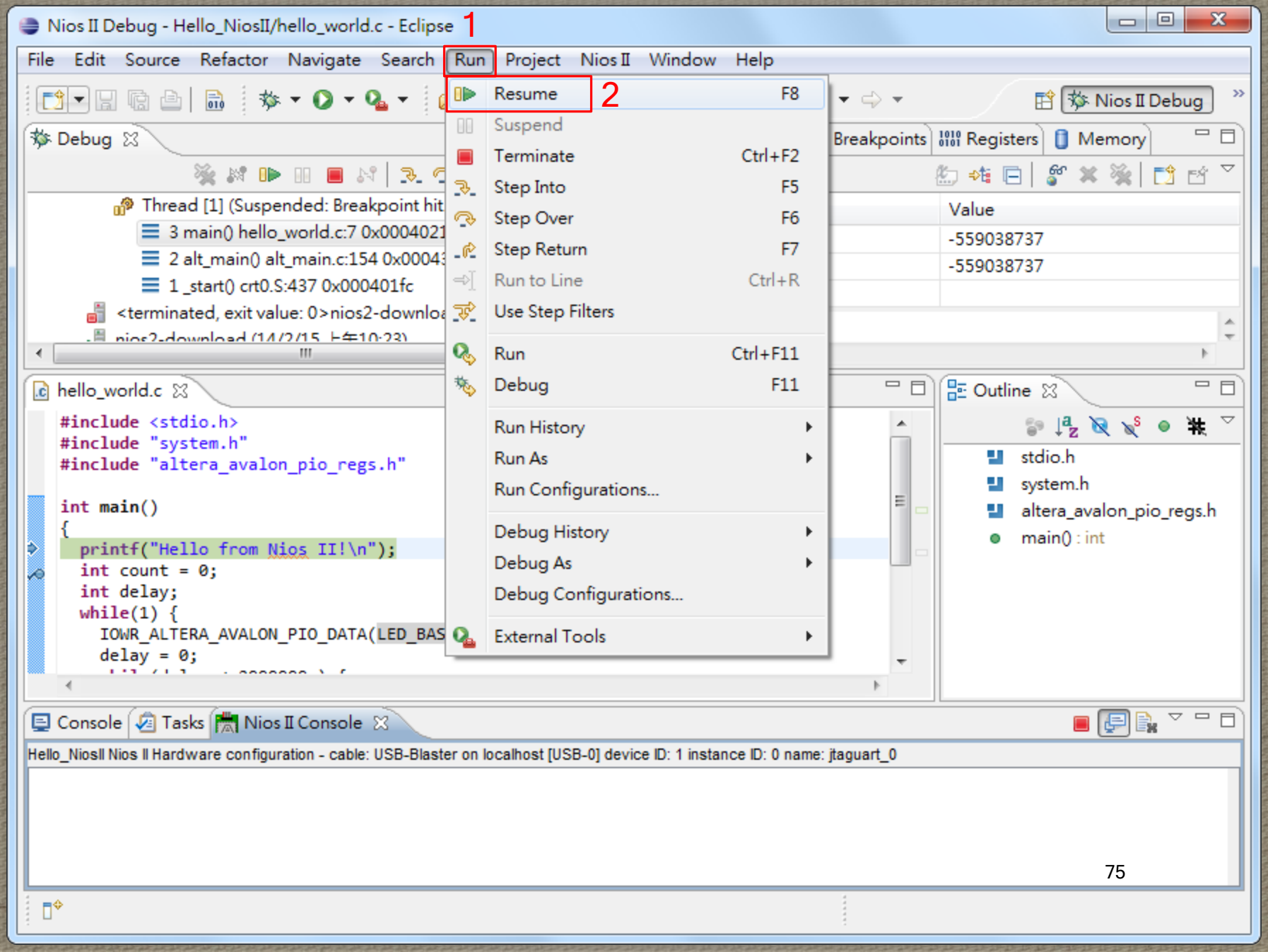
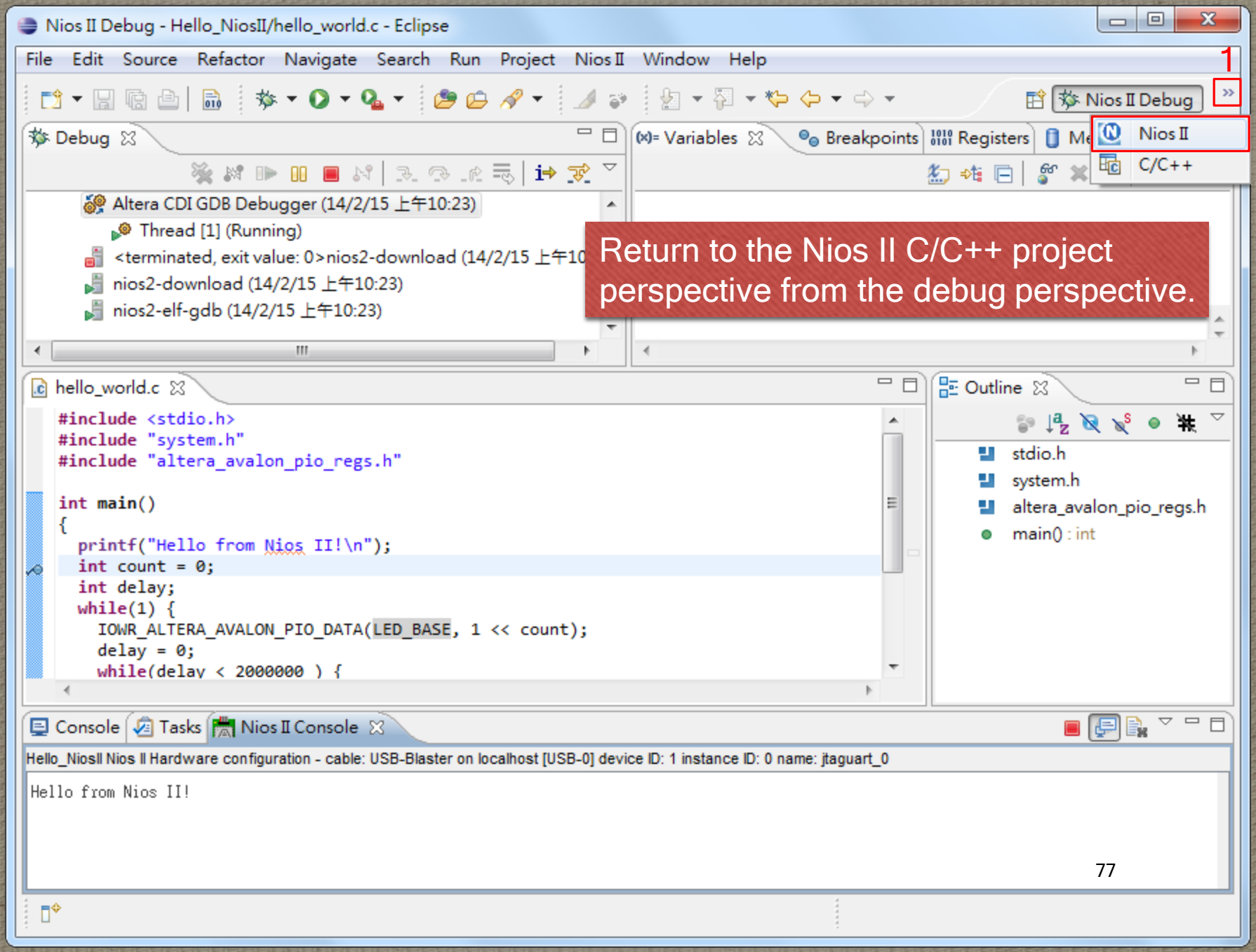
Convert To...
Run As
Debug As
Profile As
Team
Compare With
Restore from Local History...
2
1 Local C/C++ Application
2 Nios II Hardware
3
Debug Configurations...
Confirm Perspective Switch
This kind of launch is configured to open the Nios II Debug perspective when it suspends.
This perspective is designed to support efficient development of a Nios II project. It turns off automatic build and adds the Nios II Console view which is particularly useful.
Do you want to open this perspective now?
Remember my decision
4
Yes
No
USB-Blaster on localhost [USB-0] device ID: 1 instance ID: 0 name: jtagua...
74


Nios II Debug - Hello_NiosII/hello_world.c - Eclipse
1
File Edit Source Refactor Navigate Search Run Project Nios II Window Help
Resume F8
2
Suspend
Terminate Ctrl+F2
Step Into F5
Step Over F6
Step Return F7
Run to Line Ctrl+R
Use Step Filters
Run Ctrl+F11
Debug F11
Run History
Run As
Run Configurations...
Debug History
Debug As
Debug Configurations...
External Tools
Nios II Debug
Debug
Thread [1] (Suspended: Breakpoint hit
3 main() hello_world.c:7 0x0004021
2 alt_main() alt_main.c:154 0x0004
1 _start() crt0.S:437 0x000401fc
<terminated, exit value: 0>nios2-downloa
Breakpoints Registers Memory
Value
-559038737
-559038737
hello_world.c
#include <stdio.h>
#include "system.h"
#include "altera_avalon_pio_regs.h"
int main()
{
printf("Hello from Nios II!\n");
int count = 0;
int delay;
while(1) {
IOWR_ALTERA_AVALON_PIO_DATA(LED_BAS
delay = 0;
Outline
stdio.h
system.h
altera_avalon_pio_regs.h
main() : int
Console Tasks Nios II Console
Hello_NiosII Nios II Hardware configuration - cable: USB-Blaster on localhost [USB-0] device ID: 1 instance ID: 0 name: jtaguart_0

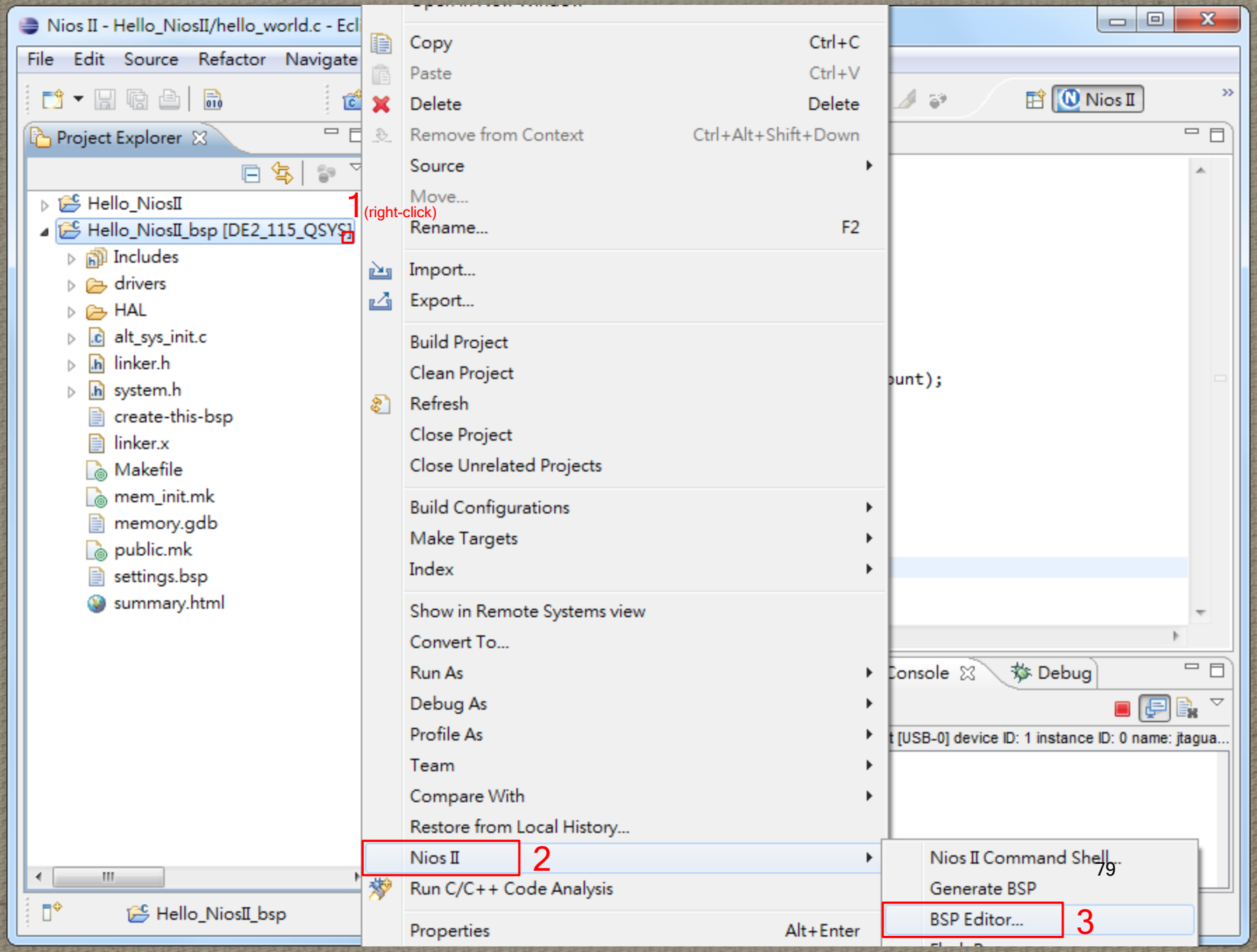
Debugging Tips

- When debugging a project in the Nios II SBT for Eclipse, you can pause, stop or single step the program, set breakpoints, examine variables, and perform many other common debugging tasks.


Nios II Debug - Hello_NiosII/hello_world.c - Eclipse
File Edit Source Refactor Navigate Search Run Project Nios II Window Help
1
Nios II Debug
Nios II
C/C++
2
Debug
Variables
Breakpoints
Registers
Altera CDI GDB Debugger (14/2/15 上午10:23)
Thread [1] (Running)
<terminated, exit value: 0>nios2-download (14/2/15 上午10
nios2-download (14/2/15 上午10:23)
nios2-elf-gdb (14/2/15 上午10:23)
Return to the Nios II C/C++ project perspective from the debug perspective.
hello_world.c
#include <stdio.h>
#include "system.h"
#include "altera_avalon_pio_regs.h"
int main()
{
printf("Hello from Nios II!\n");
int count = 0;
int delay;
while(1) {
IOWR_ALTERA_AVALON_PIO_DATA(LED_BASE, 1 << count);
delay = 0;
while(delay < 2000000) {
Outline
stdio.h
system.h
altera_avalon_pio_regs.h
main() : int
Console
Tasks
Nios II Console
Hello_NiosII Nios II Hardware configuration - cable: USB-Blaster on localhost [USB-0] device ID: 1 instance ID: 0 name: jtaguart_0
Hello from Nios II!

Configure BSP Editor

- In this section you will learn how to configure some advanced options about the target memory or other things.
- By performing the following steps, you can charge all the available settings.


Nios II - Hello_NiosII/hello_world.c - Ecl
File Edit Source Refactor Navigate
Project Explorer
Hello_NiosII
Hello_NiosII_bsp [DE2_115_QSYS]
Includes
drivers
HAL
alt_sys_init.c
linker.h
system.h
create-this-bsp
linker.x
Makefile
mem_init.mk
memory.gdb
public.mk
settings.bsp
summary.html
Hello_NiosII_bsp
1
(right-click)
Copy Ctrl+C
Paste Ctrl+V
Delete Delete
Remove from Context Ctrl+Alt+Shift+Down
Source
Move...
Rename... F2
Import...
Export...
Build Project
Clean Project
Refresh
Close Project
Close Unrelated Projects
Build Configurations
Make Targets
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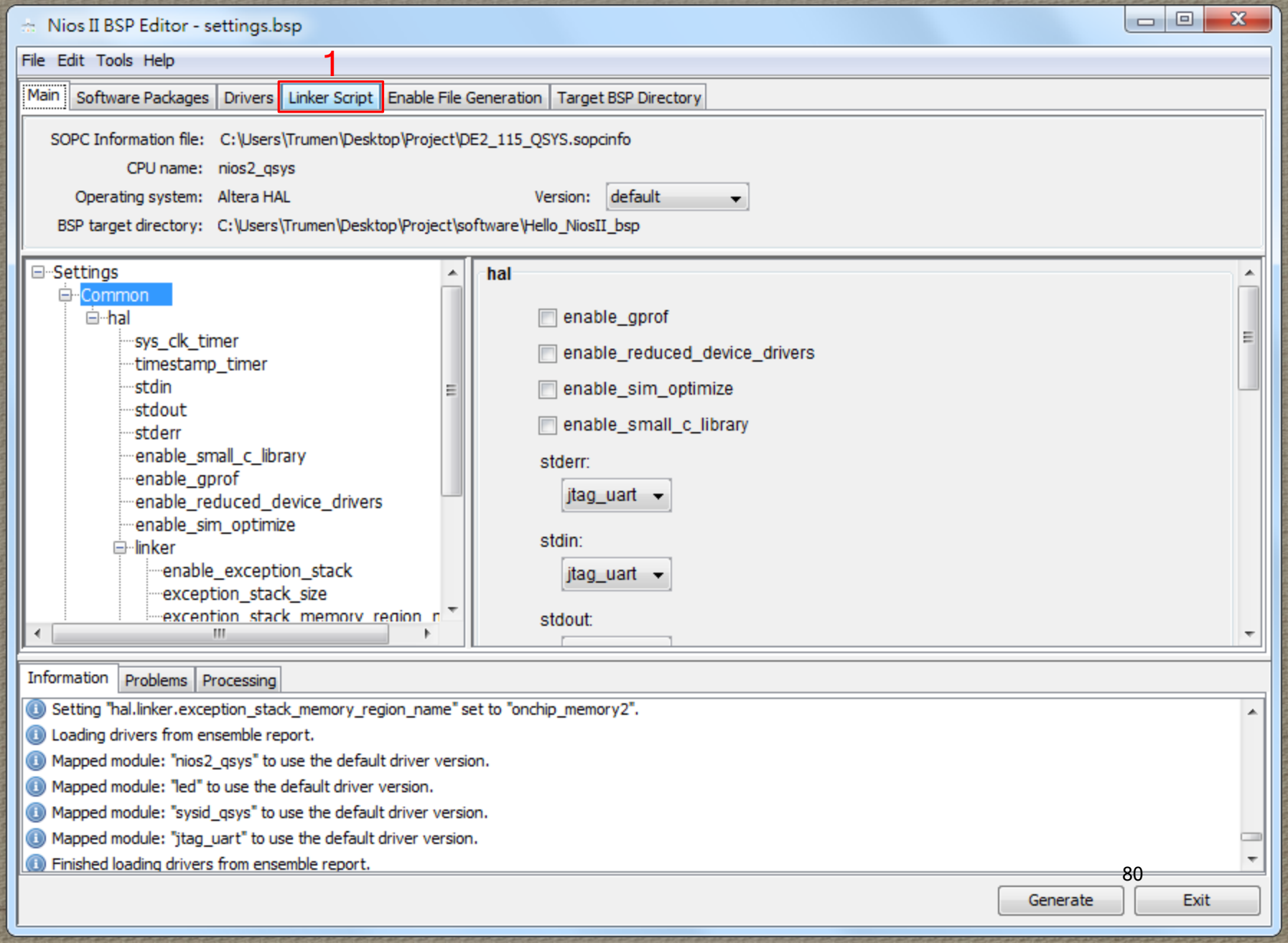
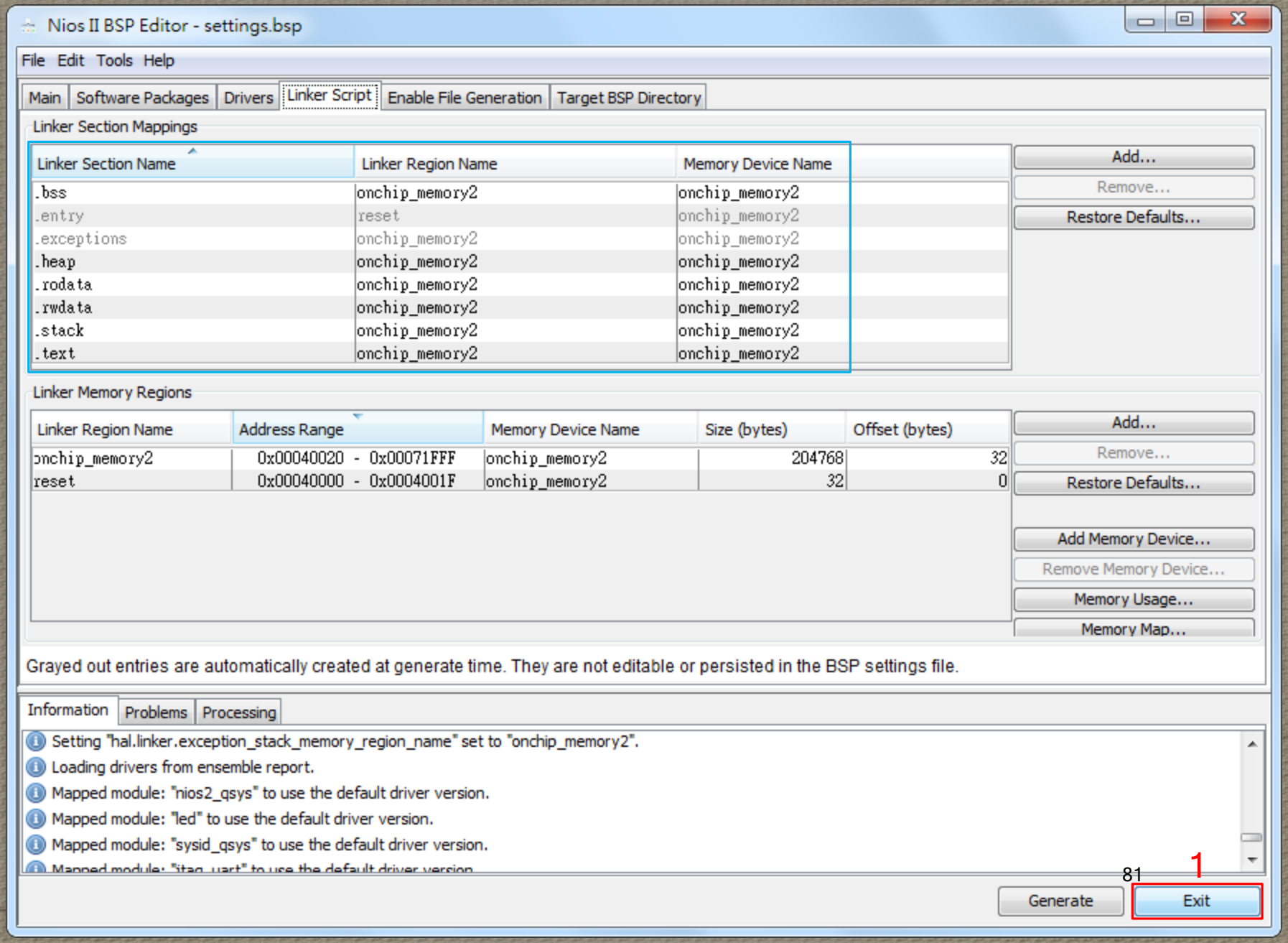
Show in Remote Systems view
Convert To...
Run As
Debug As
Profile As
Team
Compare With
Restore from Local History...
Nios II
2
Run C/C++ Code Analysis
Properties Alt+Enter
Nios II Command Shell...
Generate BSP
BSP Editor...
3
Nios II
Console
Debug
[USB-0] device ID: 1 instance ID: 0 name: jtagua...


Nios II BSP Editor - settings.bsp
File Edit Tools Help
1
Main
Software Packages
Drivers
Linker Script
Enable File Generation
Target BSP Directory
SOPC Information file: C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.sopcinfo
CPU name: nios2_qsys
Operating system: Altera HAL
Version: default
BSP target directory: C:\Users\Trumen\Desktop\Project\software\Hello_NiosII_bsp
Settings
Common
hal
sys_clk_timer
timestamp_timer
stdin
stdout
stderr
enable_small_c_library
enable_gprof
enable_reduced_device_drivers
enable_sim_optimize
linker
enable_exception_stack
exception_stack_size
hal
enable_gprof
enable_reduced_device_drivers
enable_sim_optimize
enable_small_c_library
stderr:
jtag_uart
stdin:
jtag_uart
stdout:
Information
Problems
Processing
Setting "hal.linker.exception_stack_memory_region_name" set to "onchip_memory2".
Loading drivers from ensemble report.
Mapped module: "nios2_qsys" to use the default driver version.
Mapped module: "led" to use the default driver version.
Mapped module: "sysid_qsys" to use the default driver version.
Mapped module: "jtag_uart" to use the default driver version.
Finished loading drivers from ensemble report.
Generate
Exit


Nios II BSP Editor - settings.bsp
File Edit Tools Help
Main Software Packages Drivers Linker Script Enable File Generation Target BSP Directory
Linker Section Mappings
Linker Section Name | Linker Region Name | Memory Device Name
.bss | onchip_memory2 | onchip_memory2
.entry | reset | onchip_memory2
.exceptions | onchip_memory2 | onchip_memory2
.heap | onchip_memory2 | onchip_memory2
.rodata | onchip_memory2 | onchip_memory2
.rwdata | onchip_memory2 | onchip_memory2
.stack | onchip_memory2 | onchip_memory2
.text | onchip_memory2 | onchip_memory2
Add...
Remove...
Restore Defaults...
Linker Memory Regions
Linker Region Name | Address Range | Memory Device Name | Size (bytes) | Offset (bytes)
onchip_memory2 | 0x00040020 - 0x00071FFF | onchip_memory2 | 204768 | 32
reset | 0x00040000 - 0x0004001F | onchip_memory2 | 32 | 0
Add...
Remove...
Restore Defaults...
Add Memory Device...
Remove Memory Device...
Memory Usage...
Memory Map...
Grayed out entries are automatically created at generate time. They are not editable or persisted in the BSP settings file.
Information Problems Processing
Setting "hal.linker.exception_stack_memory_region_name" set to "onchip_memory2".
Loading drivers from ensemble report.
Mapped module: "nios2_qsys" to use the default driver version.
Mapped module: "led" to use the default driver version.
Mapped module: "sysid_qsys" to use the default driver version.
Generate
Exit
81
1

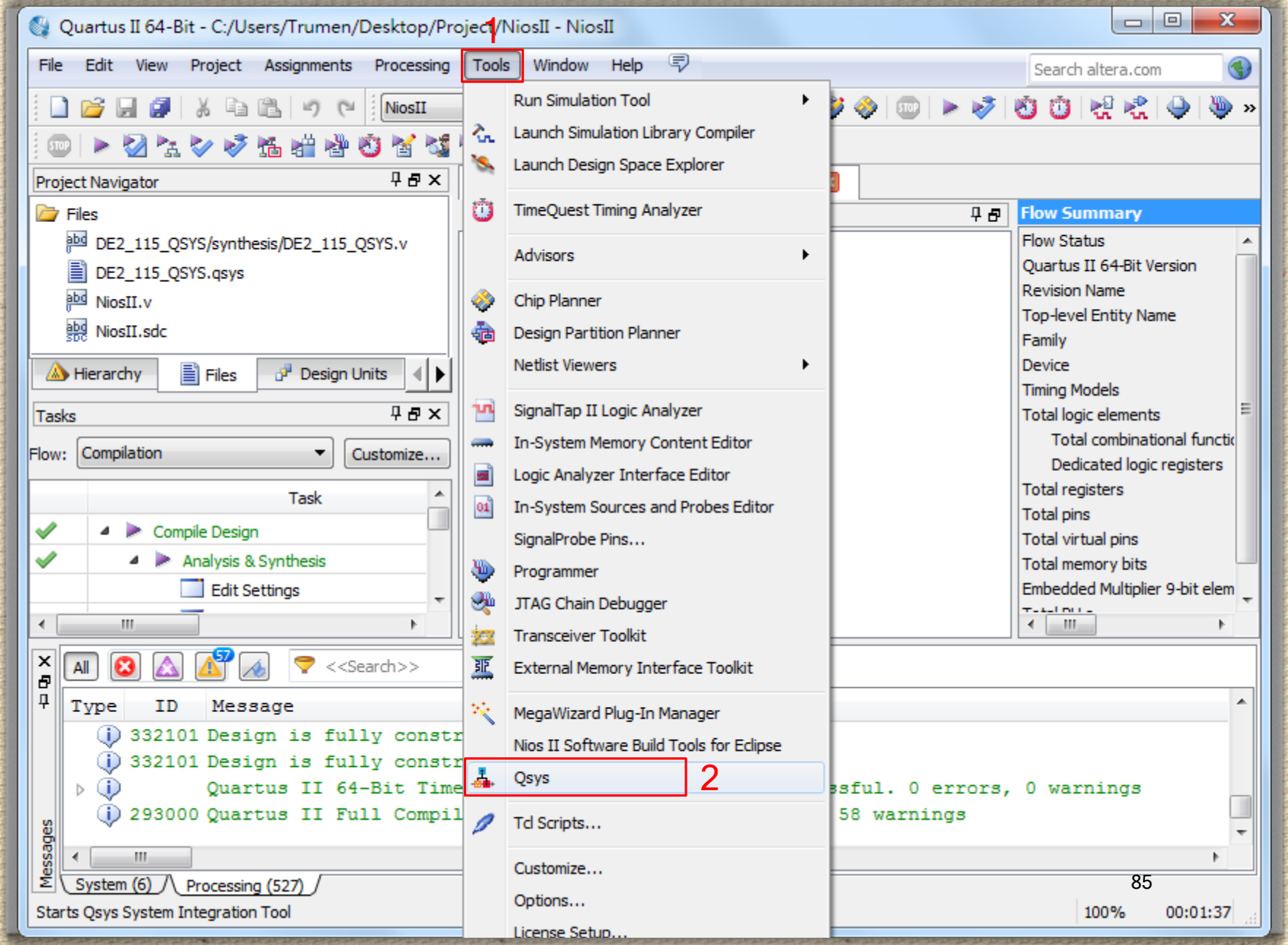
Note

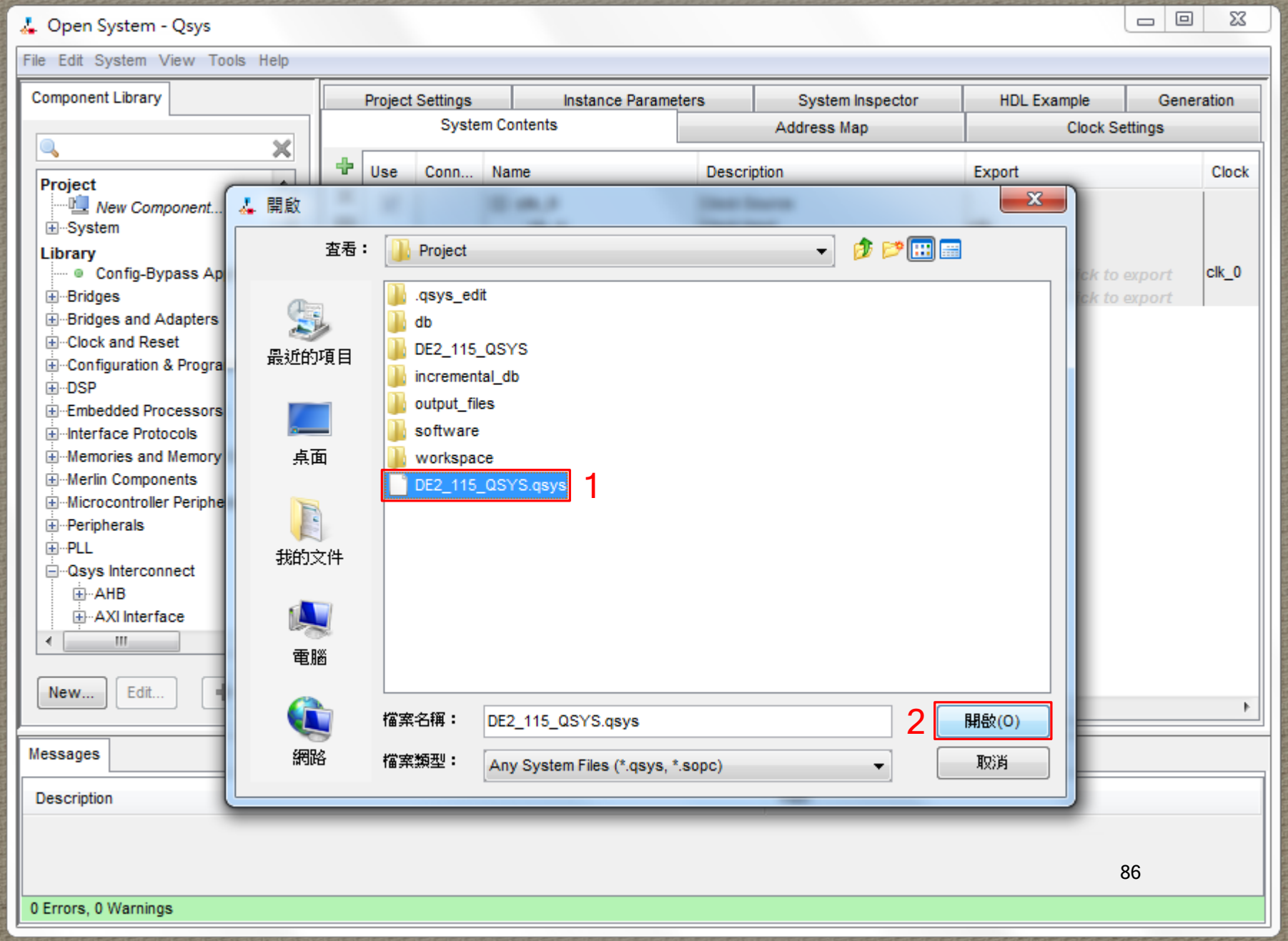
- If you make changes to the system properties or the Qsys properties or your hardware, you must rebuild your project
- To rebuild, right-click the Hello_NiosII_BSP->Nios II->Generate BSP and then Rebuild Hello_NiosII Project.

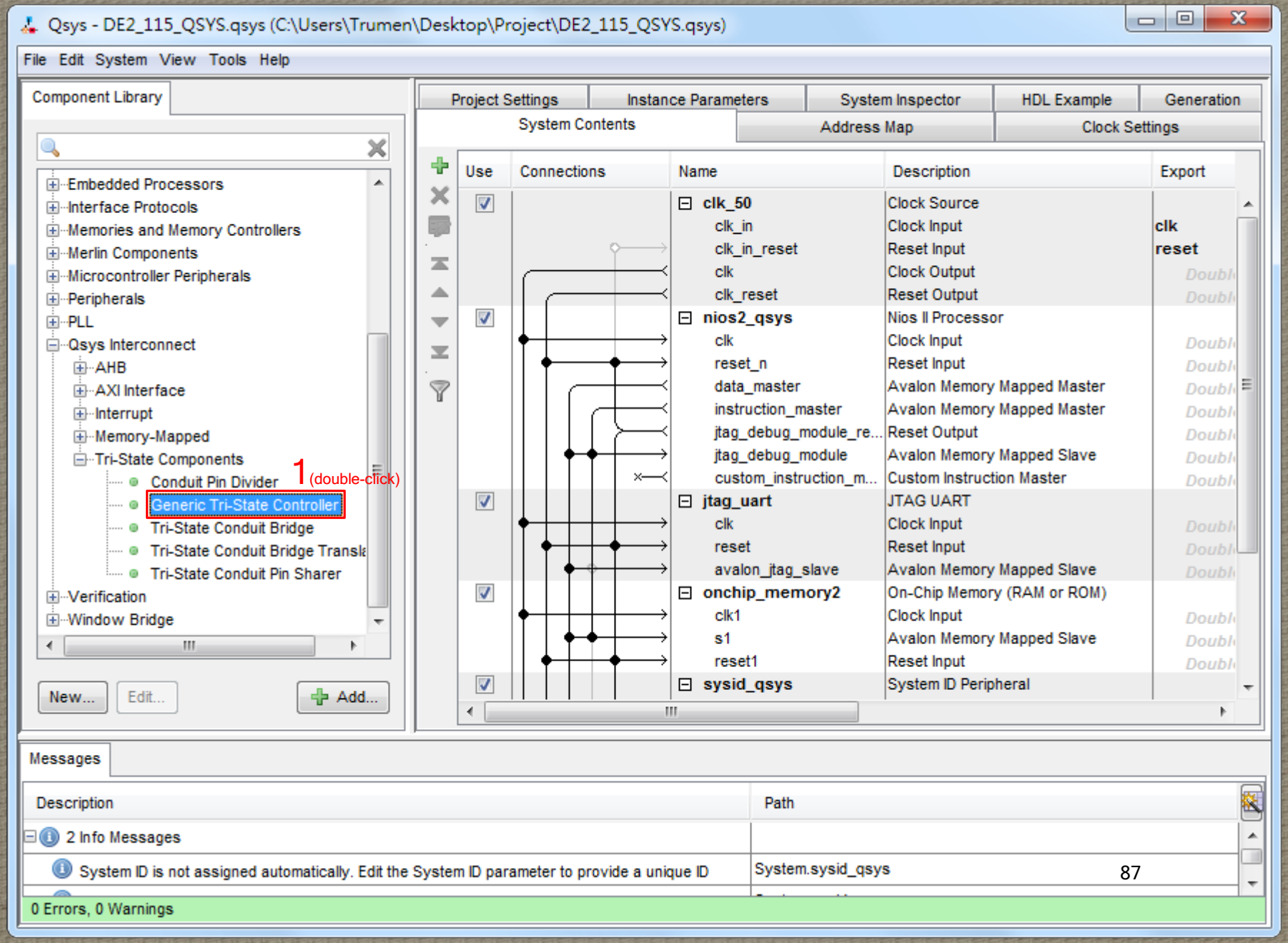
Programming the CFI Flash

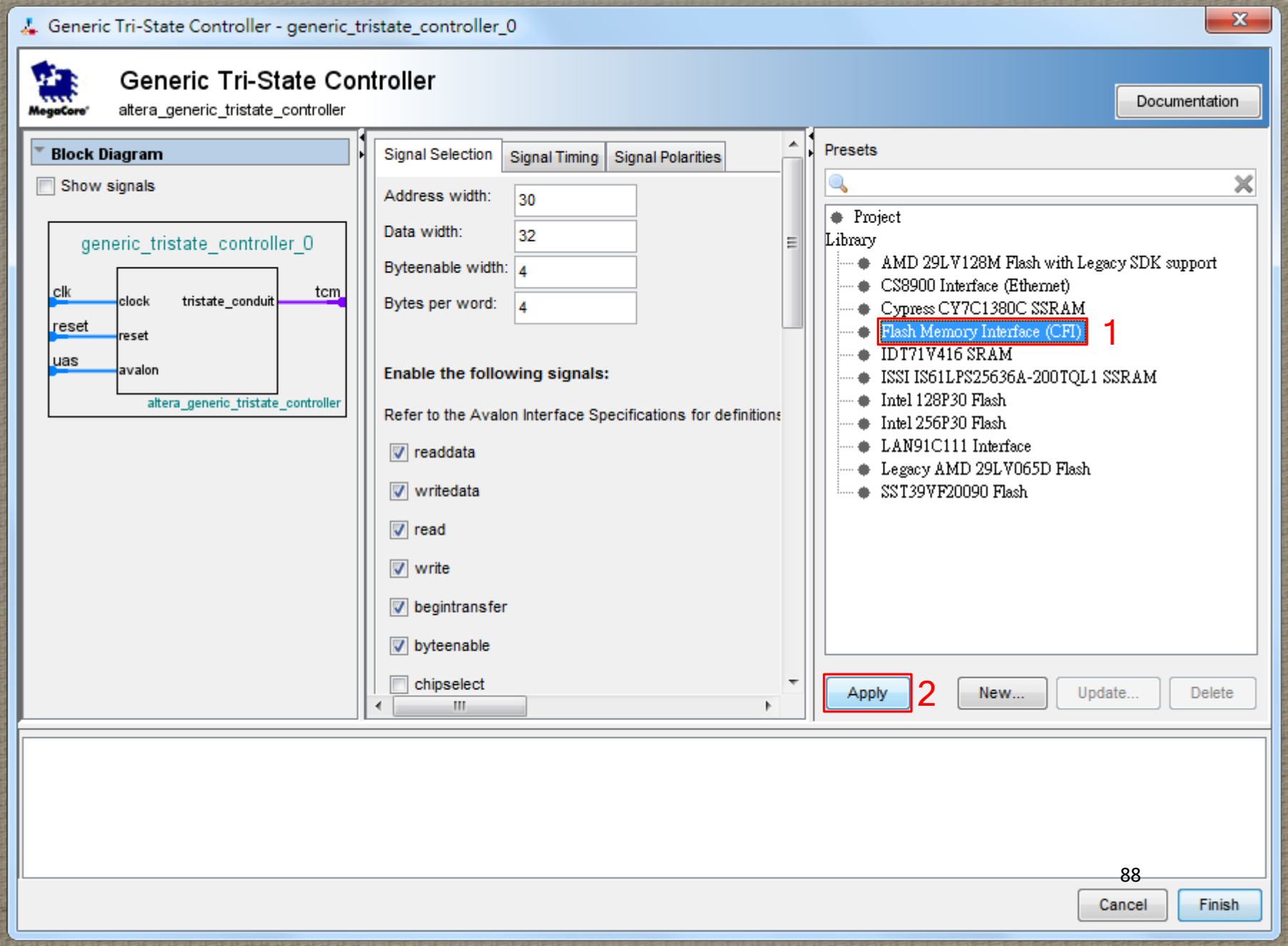
Introduction

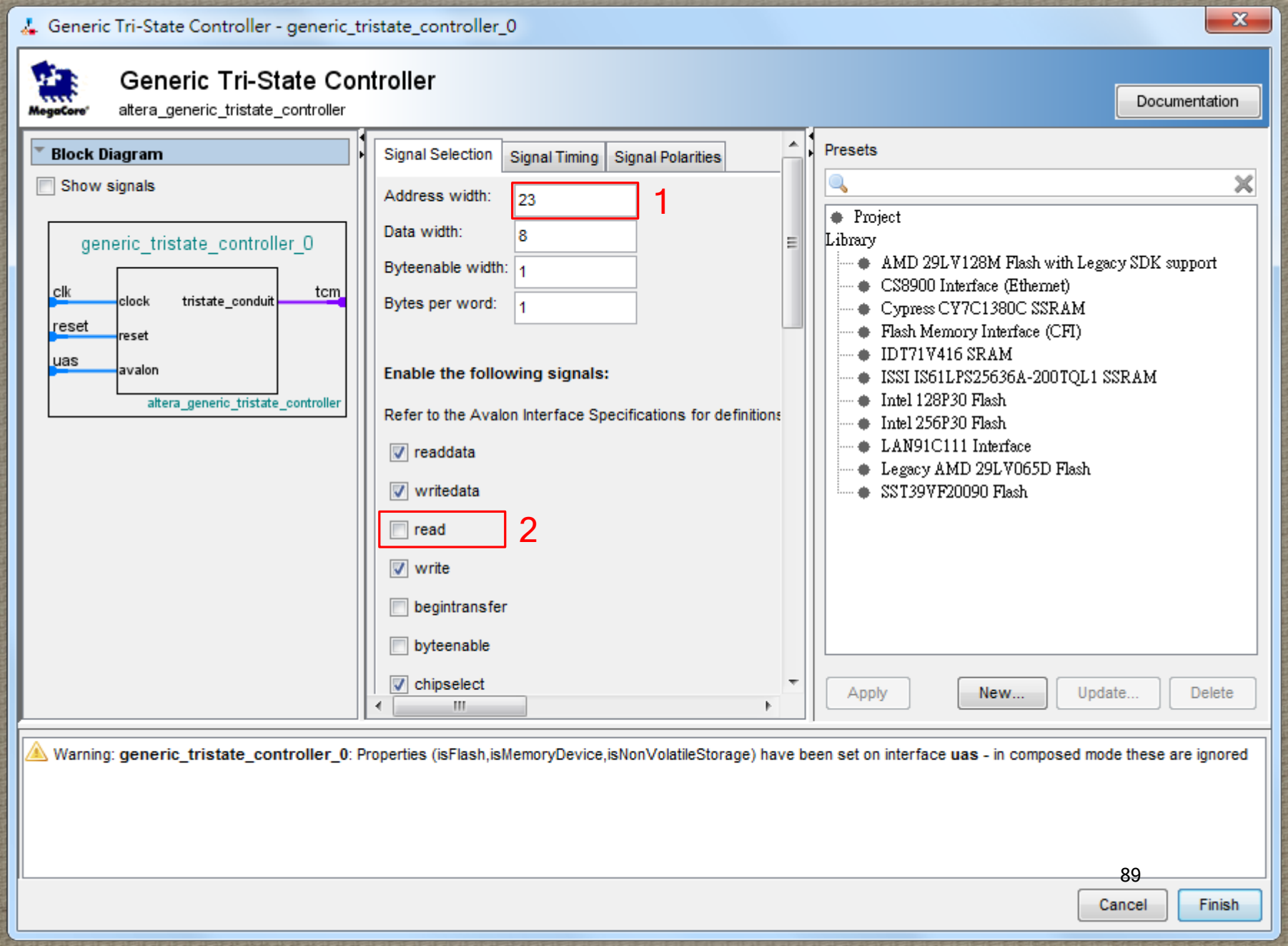
- With the density of FPGAs increasing, the need for larger configuration storage is also increasing.
- If your system contains a common flash interface (CFI) flash memory, you can use your system for FPGA configuration storage as well.

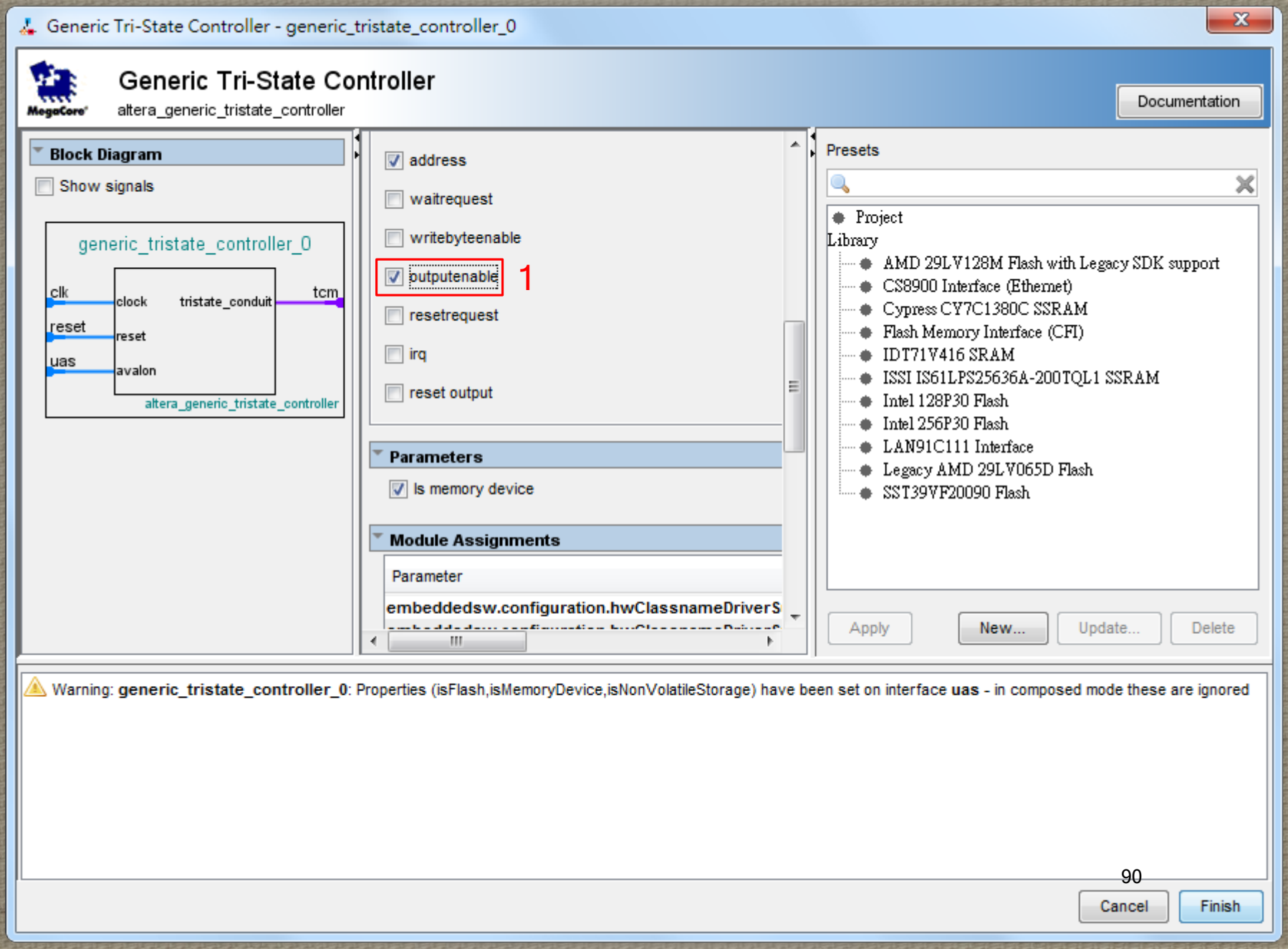

Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
NiosII
Project Navigator
Files
DE2_115_QSYS/synthesis/DE2_115_QSYS.v
DE2_115_QSYS.qsys
NiosII.v
NiosII.sdc
Hierarchy Files Design Units
Tasks
Flow: Compilation Customize...
Task
Compile Design
Analysis & Synthesis
Edit Settings
Run Simulation Tool
Launch Simulation Library Compiler
Launch Design Space Explorer
TimeQuest Timing Analyzer
Advisors
Chip Planner
Design Partition Planner
Netlist Viewers
SignalTap II Logic Analyzer
In-System Memory Content Editor
Logic Analyzer Interface Editor
In-System Sources and Probes Editor
SignalProbe Pins...
Programmer
JTAG Chain Debugger
Transceiver Toolkit
External Memory Interface Toolkit
MegaWizard Plug-In Manager
Nios II Software Build Tools for Eclipse
Qsys
2
Tcl Scripts...
Customize...
Options...
License Setup...
Flow Summary
Flow Status
Quartus II 64-Bit Version
Revision Name
Top-level Entity Name
Family
Device
Timing Models
Total logic elements
Total combinational functic
Dedicated logic registers
Total registers
Total pins
Total virtual pins
Total memory bits
Embedded Multiplier 9-bit elem
All
<<Search>>
Type ID Message
332101 Design is fully constr
332101 Design is fully constr
Quartus II 64-Bit Time
293000 Quartus II Full Compil
ssful. 0 errors, 0 warnings
58 warnings
Messages
System (6) Processing (527)
Starts Qsys System Integration Tool
100% 00:01:37

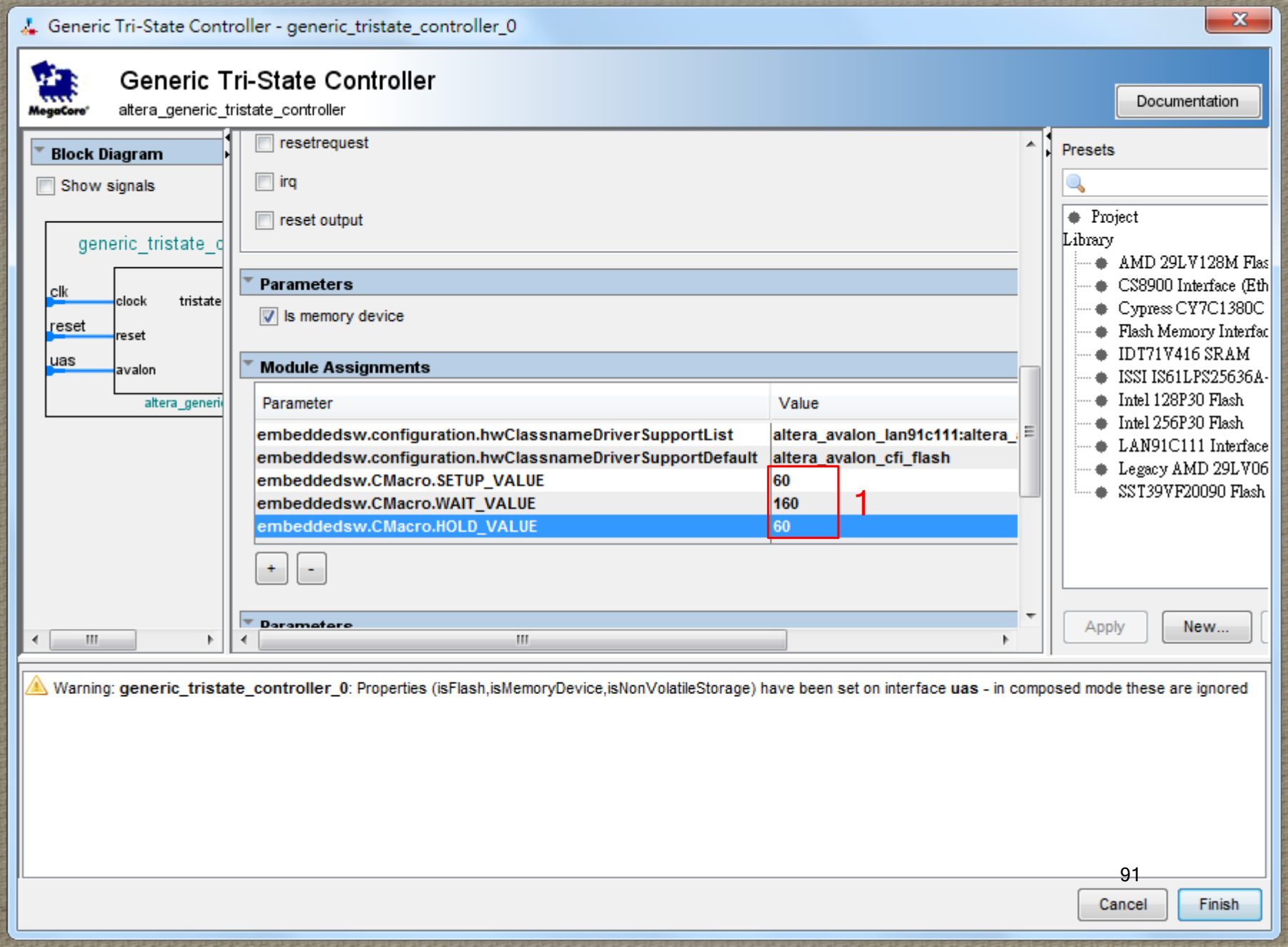

Open System - Qsys
File Edit System View Tools Help
Component Library
Project
New Component...
System
Library
Config-Bypass Ap
Bridges
Bridges and Adapters
Clock and Reset
Configuration & Progra
DSP
Embedded Processors
Interface Protocols
Memories and Memory
Merlin Components
Microcontroller Periphe
Peripherals
PLL
Qsys Interconnect
AHB
AXI Interface
New...
Edit...
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
System Contents
Address Map
Clock Settings
Use
Conn...
Name
Description
Export
Clock
clk_0
開啟
查看：
Project
.qsys_edit
db
DE2_115_QSYS
incremental_db
output_files
software
workspace
DE2_115_QSYS.qsys
1
最近的項目
桌面
我的文件
電腦
網路
檔案名稱：
DE2_115_QSYS.qsys
2
開啟(O)
檔案類型：
Any System Files (*.qsys, *.sopc)
取消
Messages
Description
0 Errors, 0 Warnings

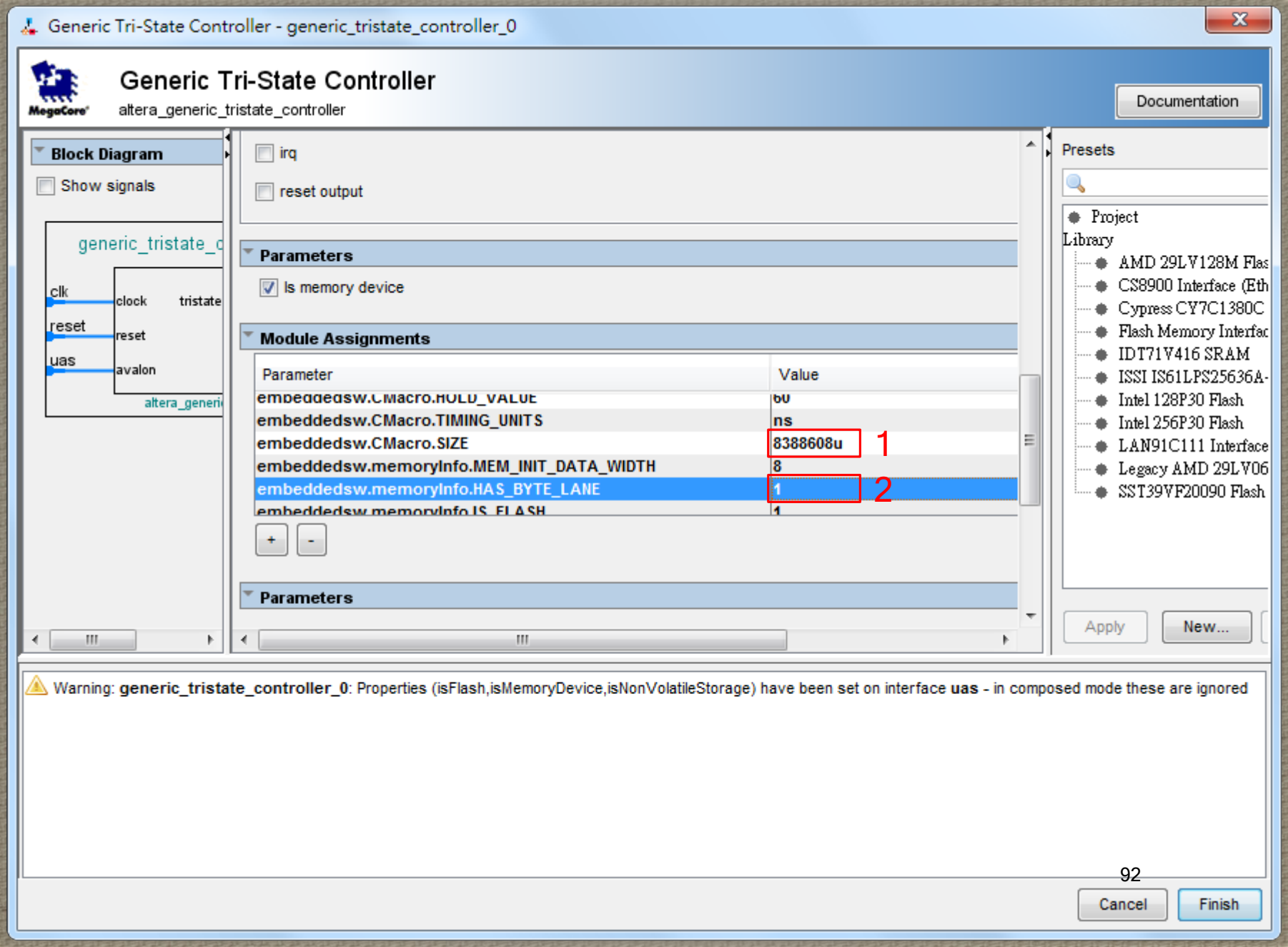

Qsys - DE2_115_QSYS.qsys (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
File Edit System View Tools Help
Component Library
Embedded Processors
Interface Protocols
Memories and Memory Controllers
Merlin Components
Microcontroller Peripherals
Peripherals
PLL
Qsys Interconnect
AHB
AXI Interface
Interrupt
Memory-Mapped
Tri-State Components
Conduit Pin Divider
Generic Tri-State Controller
Tri-State Conduit Bridge
Tri-State Conduit Bridge Transl
Tri-State Conduit Pin Sharer
Verification
Window Bridge
1 (double-click)
New...
Edit...
Add...
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
System Contents
Address Map
Clock Settings
Use
Connections
Name
Description
Export
clk_50
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
reset
clk
Clock Output
clk_reset
Reset Output
nios2_qsys
Nios II Processor
clk
Clock Input
reset_n
Reset Input
data_master
Avalon Memory Mapped Master
instruction_master
Avalon Memory Mapped Master
jtag_debug_module_re...
Reset Output
jtag_debug_module
Avalon Memory Mapped Slave
custom_instruction_m...
Custom Instruction Master
jtag_uart
JTAG UART
clk
Clock Input
reset
Reset Input
avalon_jtag_slave
Avalon Memory Mapped Slave
onchip_memory2
On-Chip Memory (RAM or ROM)
clk1
Clock Input
s1
Avalon Memory Mapped Slave
reset1
Reset Input
sysid_qsys
System ID Peripheral
Messages
Description
Path
2 Info Messages
System ID is not assigned automatically. Edit the System ID parameter to provide a unique ID
System.sysid_qsys
0 Errors, 0 Warnings

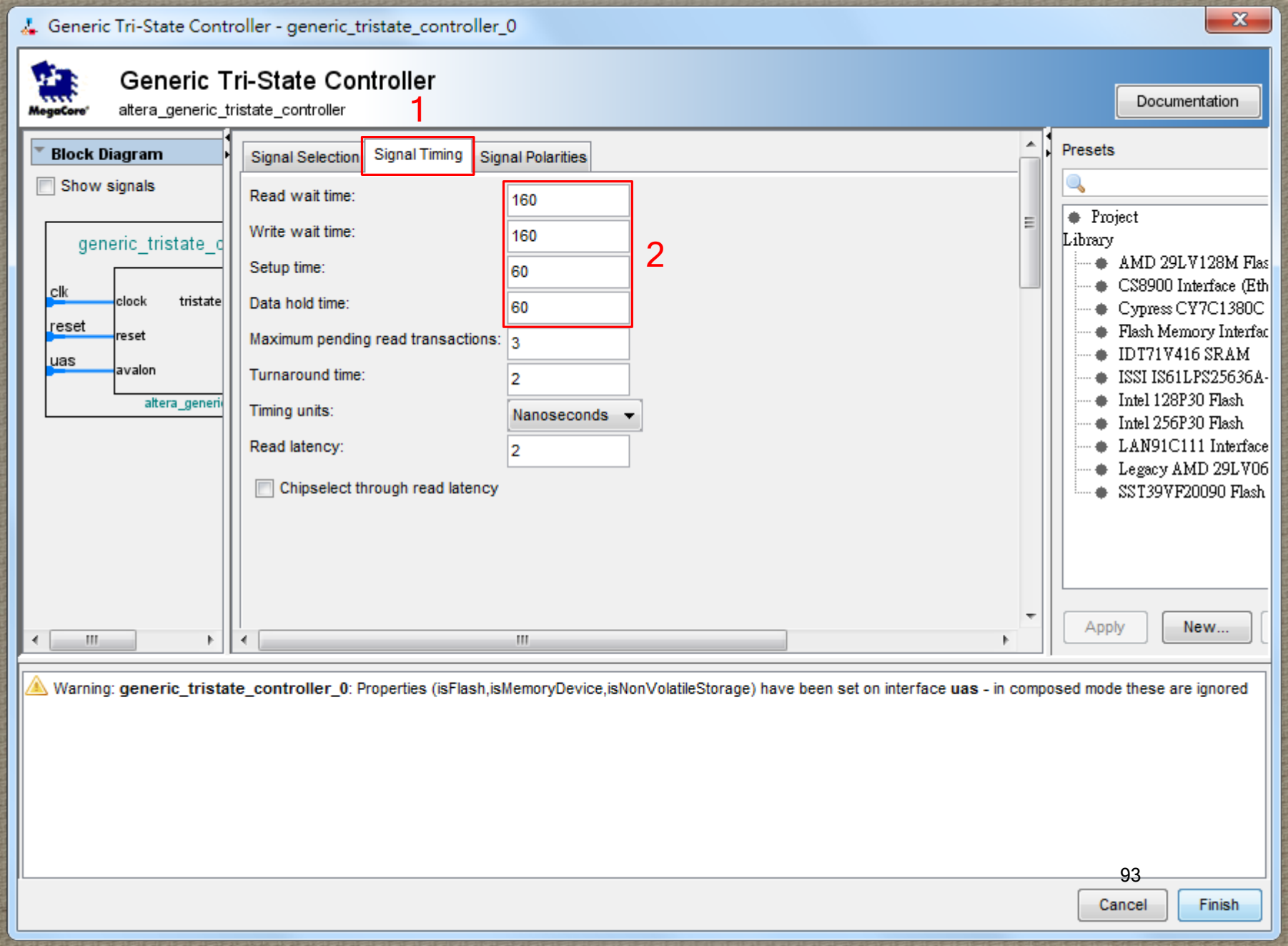

Generic Tri-State Controller - generic_tristate_controller_0
Generic Tri-State Controller
altera_generic_tristate_controller
Documentation
Block Diagram
Show signals
generic_tristate_controller_0
clk
reset
uas
clock
reset
avalon
tristate_conduit
tcm
altera_generic_tristate_controller
Signal Selection
Signal Timing
Signal Polarities
Address width: 30
Data width: 32
Byteenable width: 4
Bytes per word: 4
Enable the following signals:
Refer to the Avalon Interface Specifications for definitions
readdata
writedata
read
write
begintransfer
byteenable
chipselect
Presets
Project
Library
AMD 29LV128M Flash with Legacy SDK support
CS8900 Interface (Ethernet)
Cypress CY7C1380C SSRAM
Flash Memory Interface (CFI)
IDT71V416 SRAM
ISSI IS61LPS25636A-200TQL1 SSRAM
Intel 128P30 Flash
Intel 256P30 Flash
LAN91C111 Interface
Legacy AMD 29LV065D Flash
SST39VF20090 Flash
1
Apply
2
New...
Update...
Delete
Cancel
Finish

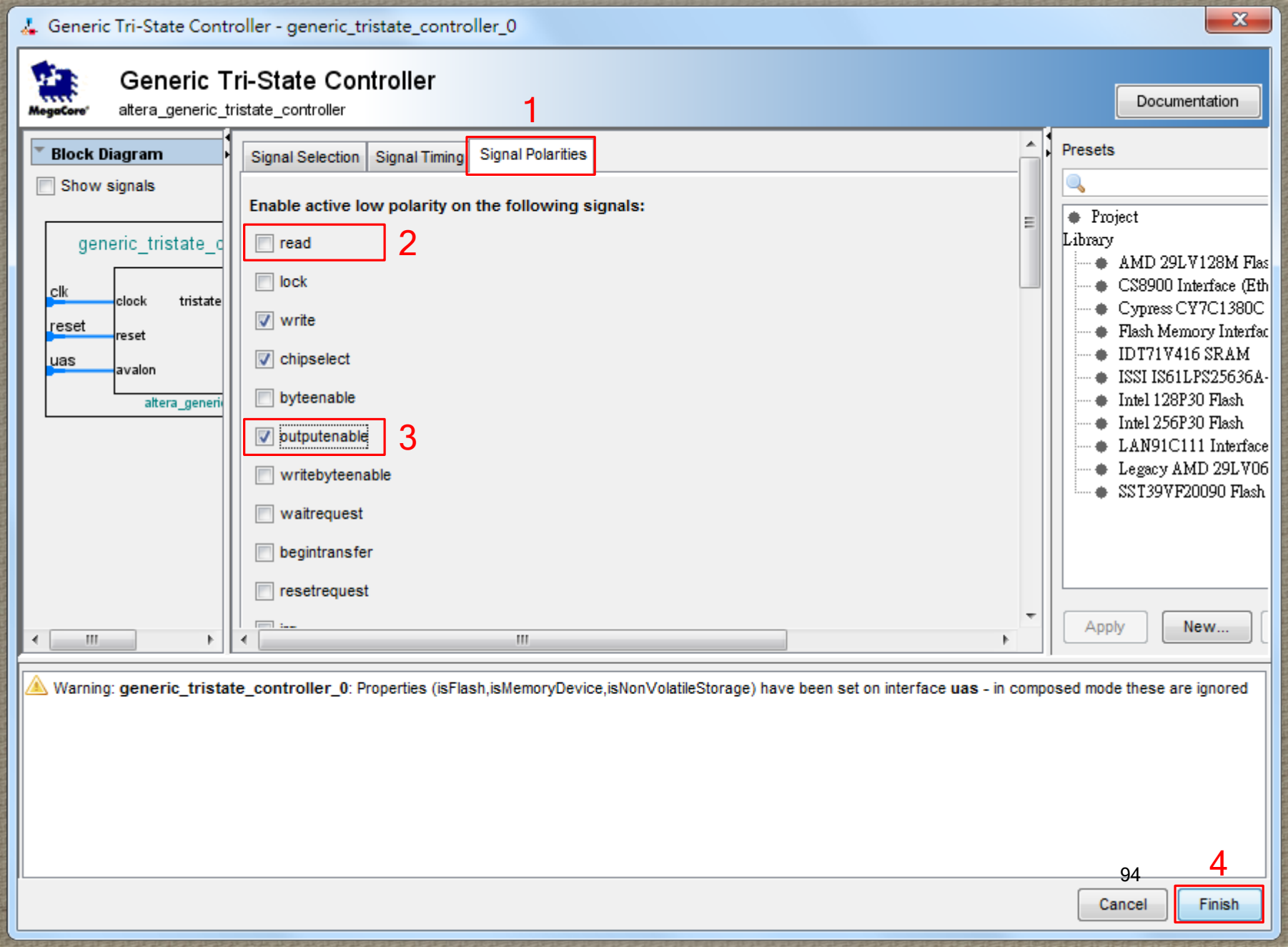

Generic Tri-State Controller - generic_tristate_controller_0
Generic Tri-State Controller
altera_generic_tristate_controller
Documentation
Block Diagram
Show signals
generic_tristate_controller_0
clk
reset
uas
clock
reset
avalon
tristate_conduit
tcm
altera_generic_tristate_controller
Signal Selection
Signal Timing
Signal Polarities
Address width: 23
1
Data width: 8
Byteenable width: 1
Bytes per word: 1
Enable the following signals:
Refer to the Avalon Interface Specifications for definitions
readdata
writedata
read
2
write
begintransfer
byteenable
chipselect
Presets
Project
Library
AMD 29LV128M Flash with Legacy SDK support
CS8900 Interface (Ethernet)
Cypress CY7C1380C SSRAM
Flash Memory Interface (CFI)
IDT71V416 SRAM
ISSI IS61LPS25636A-200TQL1 SSRAM
Intel 128P30 Flash
Intel 256P30 Flash
LAN91C111 Interface
Legacy AMD 29LV065D Flash
SST39VF20090 Flash
Apply
New...
Update...
Delete
Warning: generic_tristate_controller_0: Properties (isFlash,isMemoryDevice,isNonVolatileStorage) have been set on interface uas - in composed mode these are ignored
Cancel
Finish

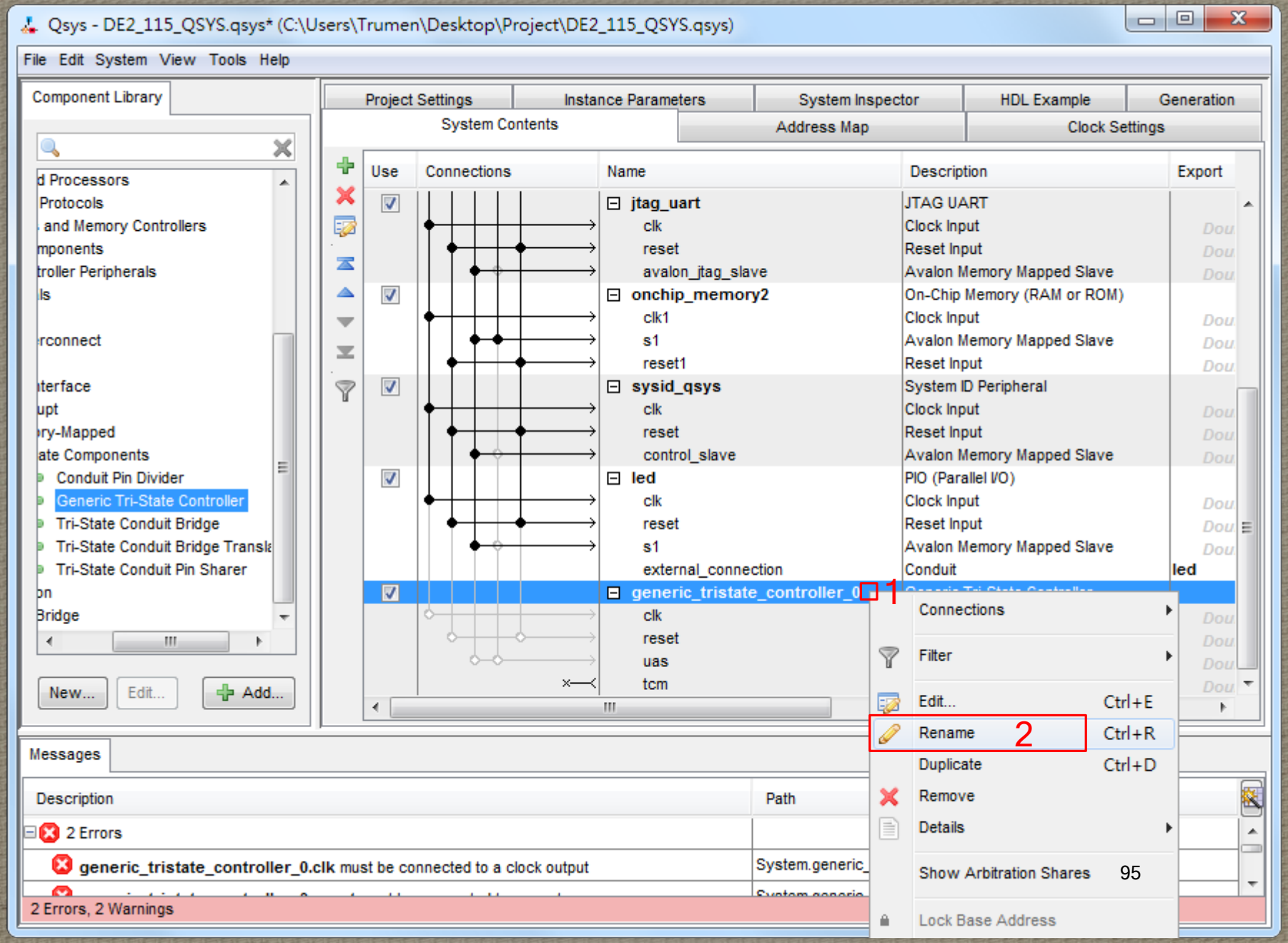

Generic Tri-State Controller - generic_tristate_controller_0
Generic Tri-State Controller
altera_generic_tristate_controller
Documentation
Block Diagram
Show signals
generic_tristate_controller_0
clk
reset
uas
clock
reset
avalon
tristate_conduit
tcm
altera_generic_tristate_controller
address
waitrequest
writebyteenable
outputenable
1
resetrequest
irq
reset output
Parameters
Is memory device
Module Assignments
Parameter
embeddedsw.configuration.hwClassnameDriverS
Presets
Project
Library
AMD 29LV128M Flash with Legacy SDK support
CS8900 Interface (Ethernet)
Cypress CY7C1380C SSRAM
Flash Memory Interface (CFI)
IDT71V416 SRAM
ISSI IS61LPS25636A-200TQL1 SSRAM
Intel 128P30 Flash
Intel 256P30 Flash
LAN91C111 Interface
Legacy AMD 29LV065D Flash
SST39VF20090 Flash
Apply
New...
Update...
Delete
Warning: generic_tristate_controller_0: Properties (isFlash,isMemoryDevice,isNonVolatileStorage) have been set on interface uas - in composed mode these are ignored
Cancel
Finish

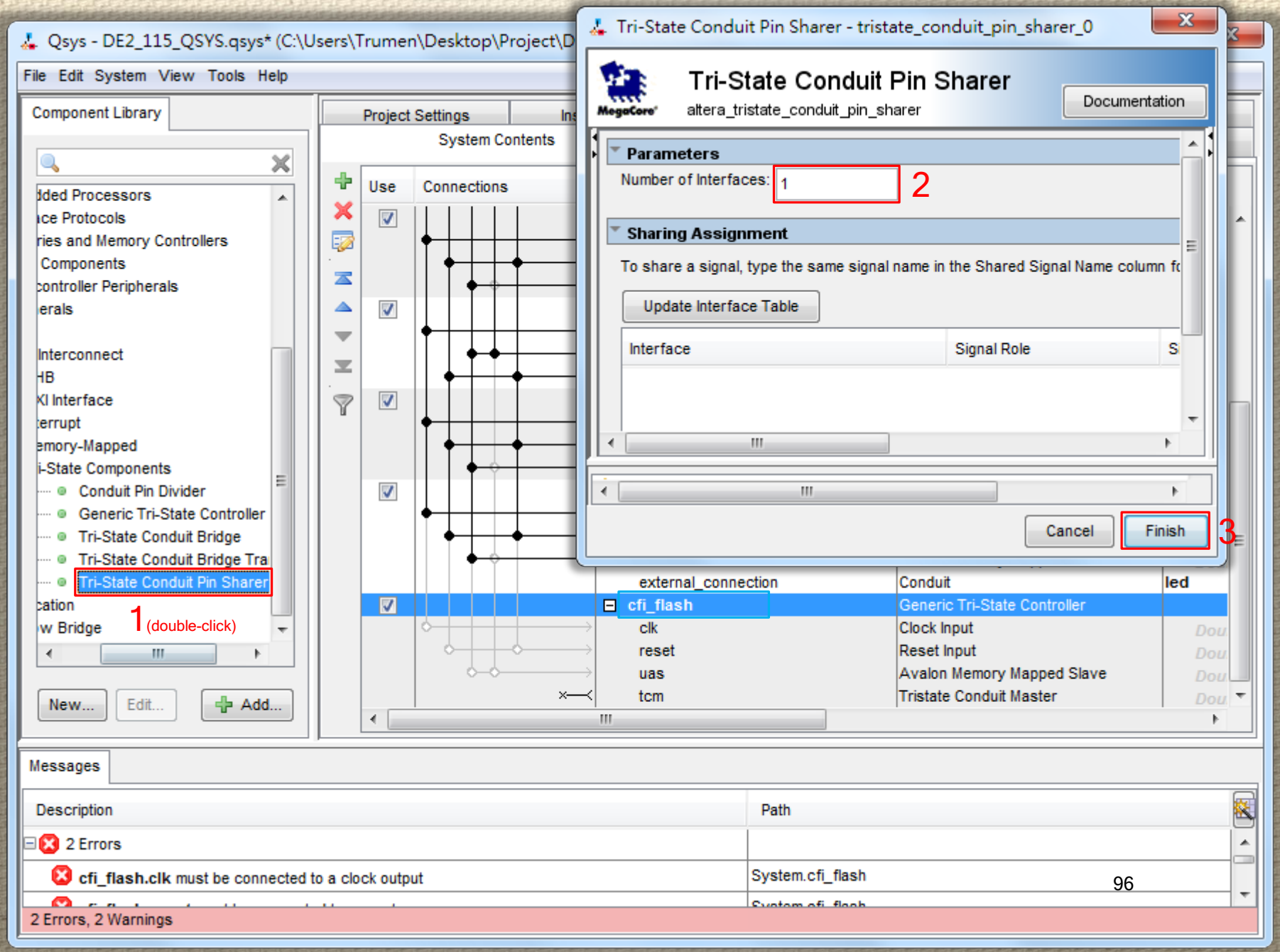

Generic Tri-State Controller - generic_tristate_controller_0
Generic Tri-State Controller
altera_generic_tristate_controller
Documentation
Block Diagram
Show signals
generic_tristate_c
clk
reset
uas
clock
reset
avalon
tristate
altera_generi
resetrequest
irq
reset output
Parameters
Is memory device
Module Assignments
Parameter
Value
embeddedsw.configuration.hwClassnameDriverSupportList
altera_avalon_lan91c111:altera_
embeddedsw.configuration.hwClassnameDriverSupportDefault
altera_avalon_cfi_flash
embeddedsw.CMacro.SETUP_VALUE
60
embeddedsw.CMacro.WAIT_VALUE
160
embeddedsw.CMacro.HOLD_VALUE
60
1
+
-
Presets
Project
Library
AMD 29LV128M Flas
CS8900 Interface (Eth
Cypress CY7C1380C
Flash Memory Interfac
IDT71V416 SRAM
ISSI IS61LPS25636A-
Intel 128P30 Flash
Intel 256P30 Flash
LAN91C111 Interface
Legacy AMD 29LV06
SST39VF20090 Flash
Apply
New...
Warning: generic_tristate_controller_0: Properties (isFlash,isMemoryDevice,isNonVolatileStorage) have been set on interface uas - in composed mode these are ignored
91
Cancel
Finish

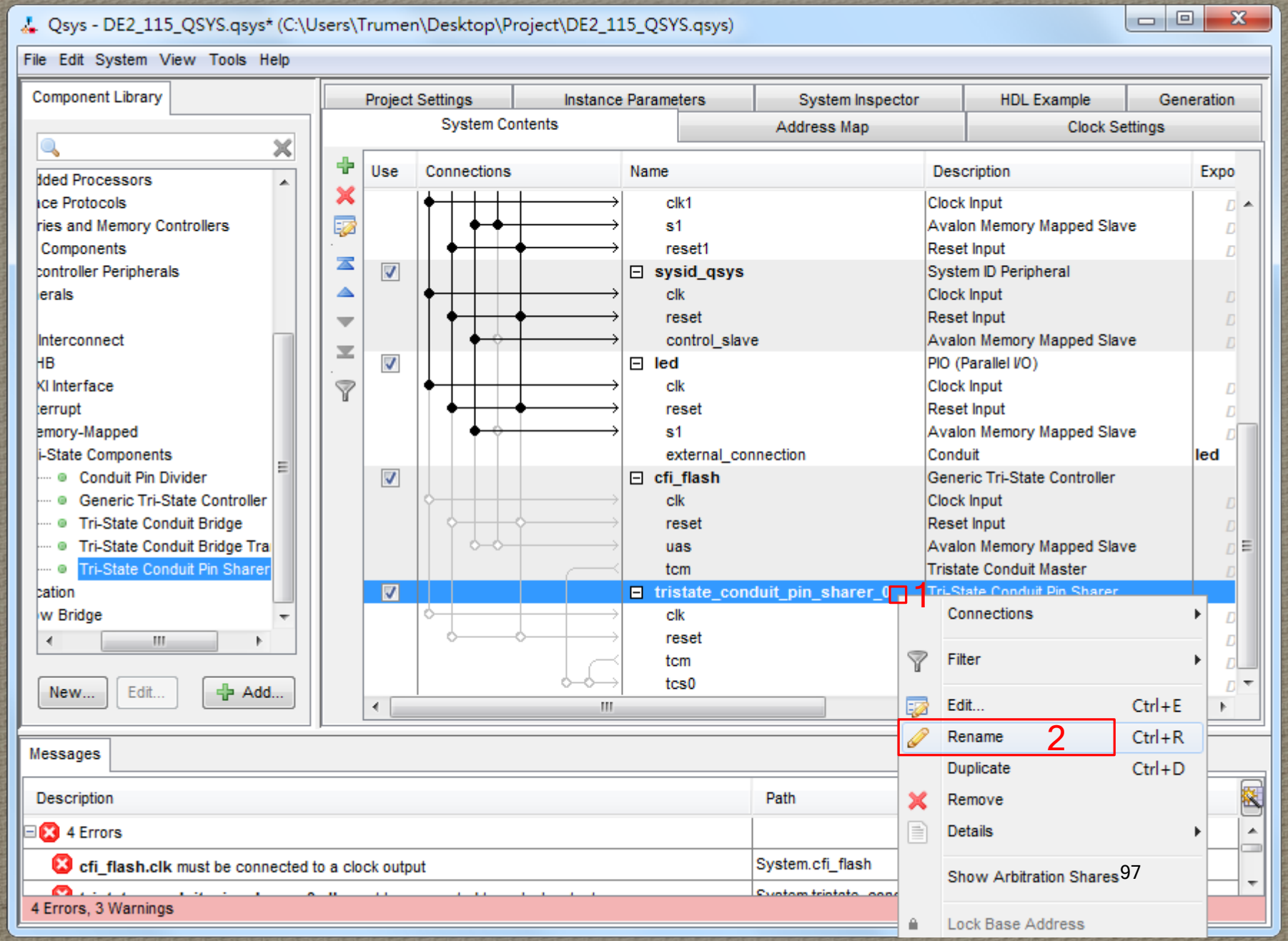

Generic Tri-State Controller - generic_tristate_controller_0
Generic Tri-State Controller
altera_generic_tristate_controller
Documentation
Block Diagram
Show signals
generic_tristate_c
clk
reset
uas
clock
reset
avalon
tristate
altera_generi
irq
reset output
Parameters
Is memory device
Module Assignments
Parameter
Value
embeddedsw.CMacro.HOLD_VALUE
60
embeddedsw.CMacro.TIMING_UNITS
ns
embeddedsw.CMacro.SIZE
8388608u
1
embeddedsw.memoryInfo.MEM_INIT_DATA_WIDTH
8
embeddedsw.memoryInfo.HAS_BYTE_LANE
1
2
embeddedsw.memoryInfo.IS_FLASH
1
+
-
Parameters
Presets
Project
Library
AMD 29LV128M Flas
CS8900 Interface (Eth
Cypress CY7C1380C
Flash Memory Interfac
IDT71V416 SRAM
ISSI IS61LPS25636A-
Intel 128P30 Flash
Intel 256P30 Flash
LAN91C111 Interface
Legacy AMD 29LV06
SST39VF20090 Flash
Apply
New...
Warning: generic_tristate_controller_0: Properties (isFlash,isMemoryDevice,isNonVolatileStorage) have been set on interface uas - in composed mode these are ignored
92
Cancel
Finish

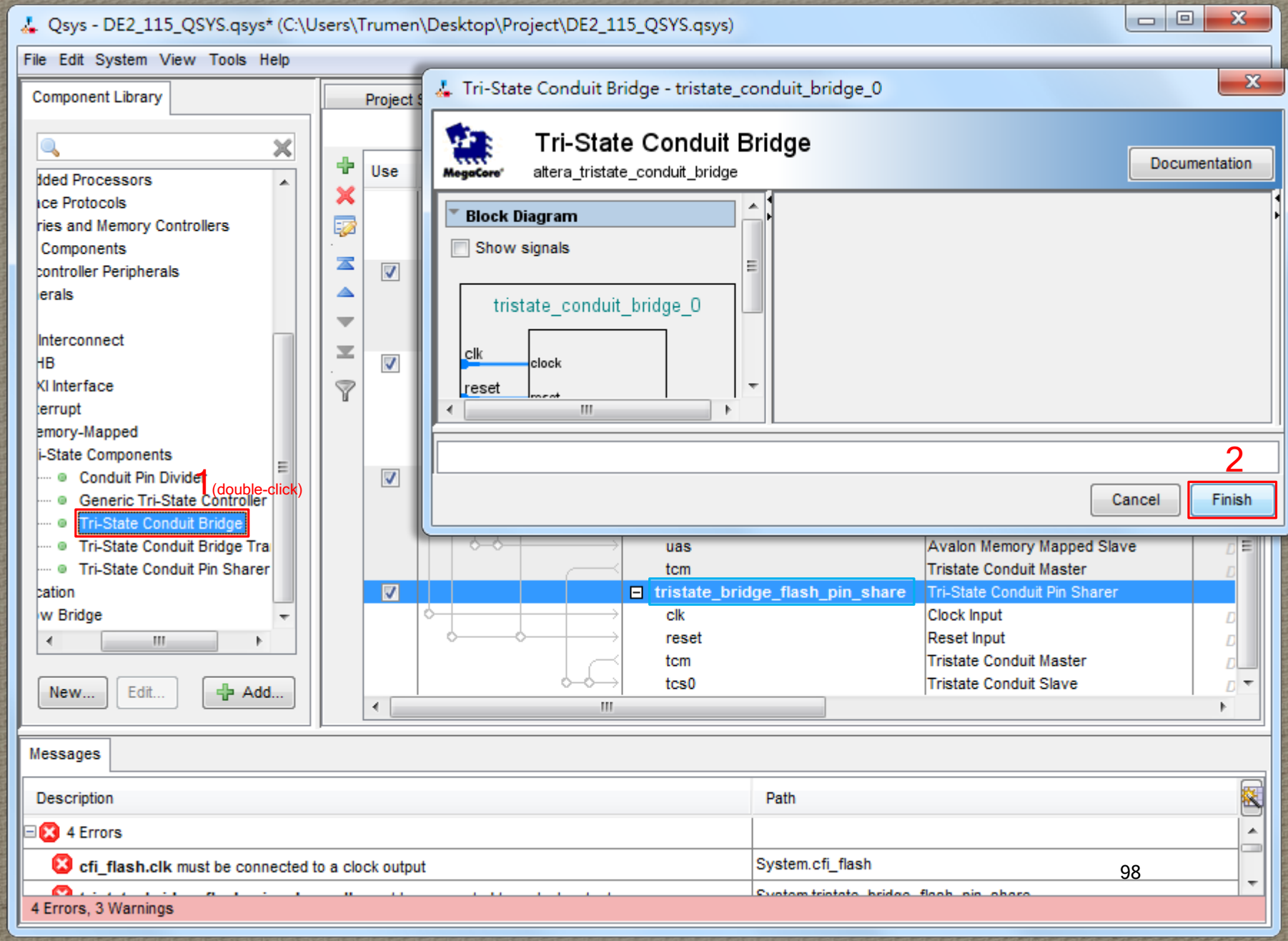

Generic Tri-State Controller - generic_tristate_controller_0
Generic Tri-State Controller
altera_generic_tristate_controller
1
Documentation
Block Diagram
Show signals
generic_tristate_c
clk
reset
uas
clock
reset
avalon
tristate
altera_generi
Signal Selection
Signal Timing
Signal Polarities
Read wait time: 160
Write wait time: 160
Setup time: 60
Data hold time: 60
2
Maximum pending read transactions: 3
Turnaround time: 2
Timing units: Nanoseconds
Read latency: 2
Chipselect through read latency
Presets
Project
Library
AMD 29LV128M Flas
CS8900 Interface (Eth
Cypress CY7C1380C
Flash Memory Interfac
IDT71V416 SRAM
ISSI IS61LPS25636A-
Intel 128P30 Flash
Intel 256P30 Flash
LAN91C111 Interface
Legacy AMD 29LV06
SST39VF20090 Flash
Apply
New...
Warning: generic_tristate_controller_0: Properties (isFlash,isMemoryDevice,isNonVolatileStorage) have been set on interface uas - in composed mode these are ignored
Cancel
Finish

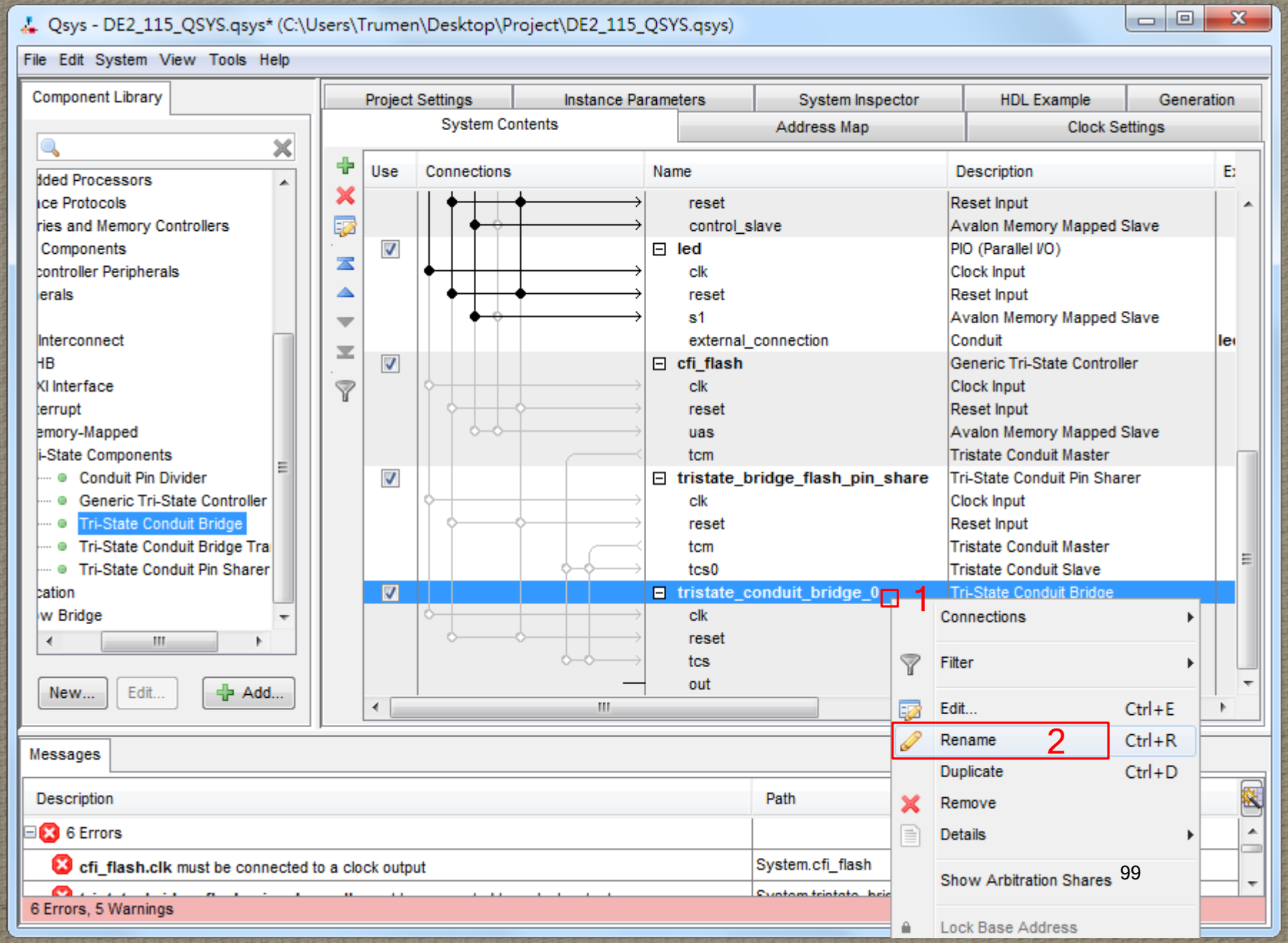

Generic Tri-State Controller - generic_tristate_controller_0
Generic Tri-State Controller
altera_generic_tristate_controller
Documentation
1
Block Diagram
Show signals
generic_tristate_c
clk
reset
uas
clock
reset
avalon
tristate
altera_generi
Signal Selection
Signal Timing
Signal Polarities
Enable active low polarity on the following signals:
read
2
lock
write
chipselect
byteenable
outputenable
3
writebyteenable
waitrequest
begintransfer
resetrequest
Presets
Project
Library
AMD 29LV128M Flas
CS8900 Interface (Eth
Cypress CY7C1380C
Flash Memory Interfac
IDT71V416 SRAM
ISSI IS61LPS25636A-
Intel 128P30 Flash
Intel 256P30 Flash
LAN91C111 Interface
Legacy AMD 29LV06
SST39VF20090 Flash
Apply
New...
Warning: generic_tristate_controller_0: Properties (isFlash,isMemoryDevice,isNonVolatileStorage) have been set on interface uas - in composed mode these are ignored
94
4
Cancel
Finish

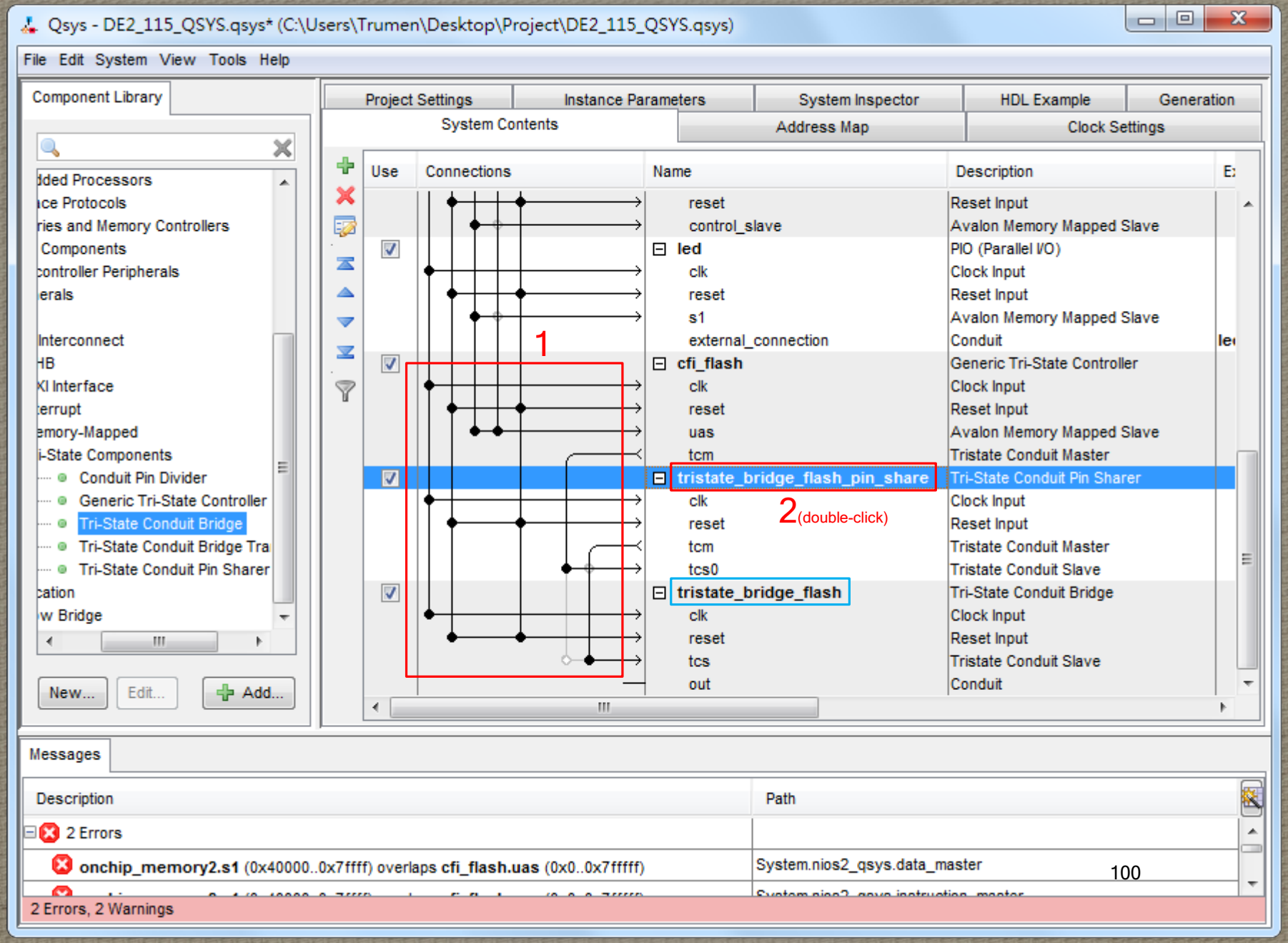

Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
File Edit System View Tools Help
Component Library
Conduit Pin Divider
Generic Tri-State Controller
Tri-State Conduit Bridge
Tri-State Conduit Bridge Transl
Tri-State Conduit Pin Sharer
New...
Edit...
Add...
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
System Contents
Address Map
Clock Settings
Use
Connections
Name
Description
Export
jtag_uart
JTAG UART
clk
Clock Input
reset
Reset Input
avalon_jtag_slave
Avalon Memory Mapped Slave
onchip_memory2
On-Chip Memory (RAM or ROM)
clk1
Clock Input
s1
Avalon Memory Mapped Slave
reset1
Reset Input
sysid_qsys
System ID Peripheral
clk
Clock Input
reset
Reset Input
control_slave
Avalon Memory Mapped Slave
led
PIO (Parallel I/O)
clk
Clock Input
reset
Reset Input
s1
Avalon Memory Mapped Slave
external_connection
Conduit
led
generic_tristate_controller_0
clk
reset
uas
tcm
1
Connections
Filter
Edit...
Ctrl+E
Rename
2
Ctrl+R
Duplicate
Ctrl+D
Remove
Details
Show Arbitration Shares
95
Lock Base Address
Messages
Description
Path
2 Errors
generic_tristate_controller_0.clk must be connected to a clock output
System.generic_
2 Errors, 2 Warnings


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\D
File Edit System View Tools Help
Component Library
Project Settings
System Contents
Use
Connections
Interconnect
Conduit Pin Divider
Generic Tri-State Controller
Tri-State Conduit Bridge
Tri-State Conduit Bridge Tra
Tri-State Conduit Pin Sharer
1 (double-click)
New...
Edit...
Add...
Tri-State Conduit Pin Sharer - tristate_conduit_pin_sharer_0
Tri-State Conduit Pin Sharer
altera_tristate_conduit_pin_sharer
Documentation
Parameters
Number of Interfaces: 1
2
Sharing Assignment
To share a signal, type the same signal name in the Shared Signal Name column fo
Update Interface Table
Interface
Signal Role
Cancel
Finish
3
external_connection
Conduit
cfi_flash
Generic Tri-State Controller
clk
Clock Input
reset
Reset Input
uas
Avalon Memory Mapped Slave
tcm
Tristate Conduit Master
Messages
Description
Path
2 Errors
cfi_flash.clk must be connected to a clock output
System.cfi_flash
2 Errors, 2 Warnings


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
File Edit System View Tools Help
Component Library
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
System Contents
Address Map
Clock Settings
Use
Connections
Name
Description
Expo
clk1
Clock Input
s1
Avalon Memory Mapped Slave
reset1
Reset Input
sysid_qsys
System ID Peripheral
clk
Clock Input
reset
Reset Input
control_slave
Avalon Memory Mapped Slave
led
PIO (Parallel I/O)
clk
Clock Input
reset
Reset Input
s1
Avalon Memory Mapped Slave
external_connection
Conduit
led
cfi_flash
Generic Tri-State Controller
clk
Clock Input
reset
Reset Input
uas
Avalon Memory Mapped Slave
tcm
Tristate Conduit Master
tristate_conduit_pin_sharer_0
clk
reset
tcm
tcs0
Conduit Pin Divider
Generic Tri-State Controller
Tri-State Conduit Bridge
Tri-State Conduit Bridge Tra
Tri-State Conduit Pin Sharer
New...
Edit...
Add...
1
2
Connections
Filter
Edit... Ctrl+E
Rename Ctrl+R
Duplicate Ctrl+D
Remove
Details
Show Arbitration Shares
Lock Base Address
Messages
Description
Path
4 Errors
cfi_flash.clk must be connected to a clock output
System.cfi_flash
4 Errors, 3 Warnings


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
File Edit System View Tools Help
Component Library
Tri-State Conduit Bridge
Conduit Pin Divider
Generic Tri-State Controller
Tri-State Conduit Bridge
Tri-State Conduit Bridge Tra
Tri-State Conduit Pin Sharer
1 (double-click)
New...
Edit...
Add...
Tri-State Conduit Bridge - tristate_conduit_bridge_0
Tri-State Conduit Bridge
altera_tristate_conduit_bridge
Documentation
Block Diagram
Show signals
tristate_conduit_bridge_0
clk
clock
reset
2
Cancel
Finish
uas
Avalon Memory Mapped Slave
tcm
Tristate Conduit Master
tristate_bridge_flash_pin_share
Tri-State Conduit Pin Sharer
clk
Clock Input
reset
Reset Input
tcm
Tristate Conduit Master
tcs0
Tristate Conduit Slave
Messages
Description
Path
4 Errors
cfi_flash.clk must be connected to a clock output
System.cfi_flash
4 Errors, 3 Warnings


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
File Edit System View Tools Help
Component Library
Conduit Pin Divider
Generic Tri-State Controller
Tri-State Conduit Bridge
Tri-State Conduit Bridge Tra
Tri-State Conduit Pin Sharer
New...
Edit...
Add...
Project Settings
Instance Parameters
System Inspector
HDL Example
Generation
System Contents
Address Map
Clock Settings
Use
Connections
Name
Description
reset
Reset Input
control_slave
Avalon Memory Mapped Slave
led
PIO (Parallel I/O)
clk
Clock Input
reset
Reset Input
s1
Avalon Memory Mapped Slave
external_connection
Conduit
cfi_flash
Generic Tri-State Controller
clk
Clock Input
reset
Reset Input
uas
Avalon Memory Mapped Slave
tcm
Tristate Conduit Master
tristate_bridge_flash_pin_share
Tri-State Conduit Pin Sharer
clk
Clock Input
reset
Reset Input
tcm
Tristate Conduit Master
tcs0
Tristate Conduit Slave
tristate_conduit_bridge_0
Tri-State Conduit Bridge
clk
reset
tcs
out
1
Connections
Filter
Edit... Ctrl+E
Rename 2 Ctrl+R
Duplicate Ctrl+D
Remove
Details
Show Arbitration Shares 99
Lock Base Address
Messages
Description
Path
6 Errors
cfi_flash.clk must be connected to a clock output
System.cfi_flash
6 Errors, 5 Warnings


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
File Edit System View Tools Help
Component Library
Project Settings
Instance Parameters
System Inspector
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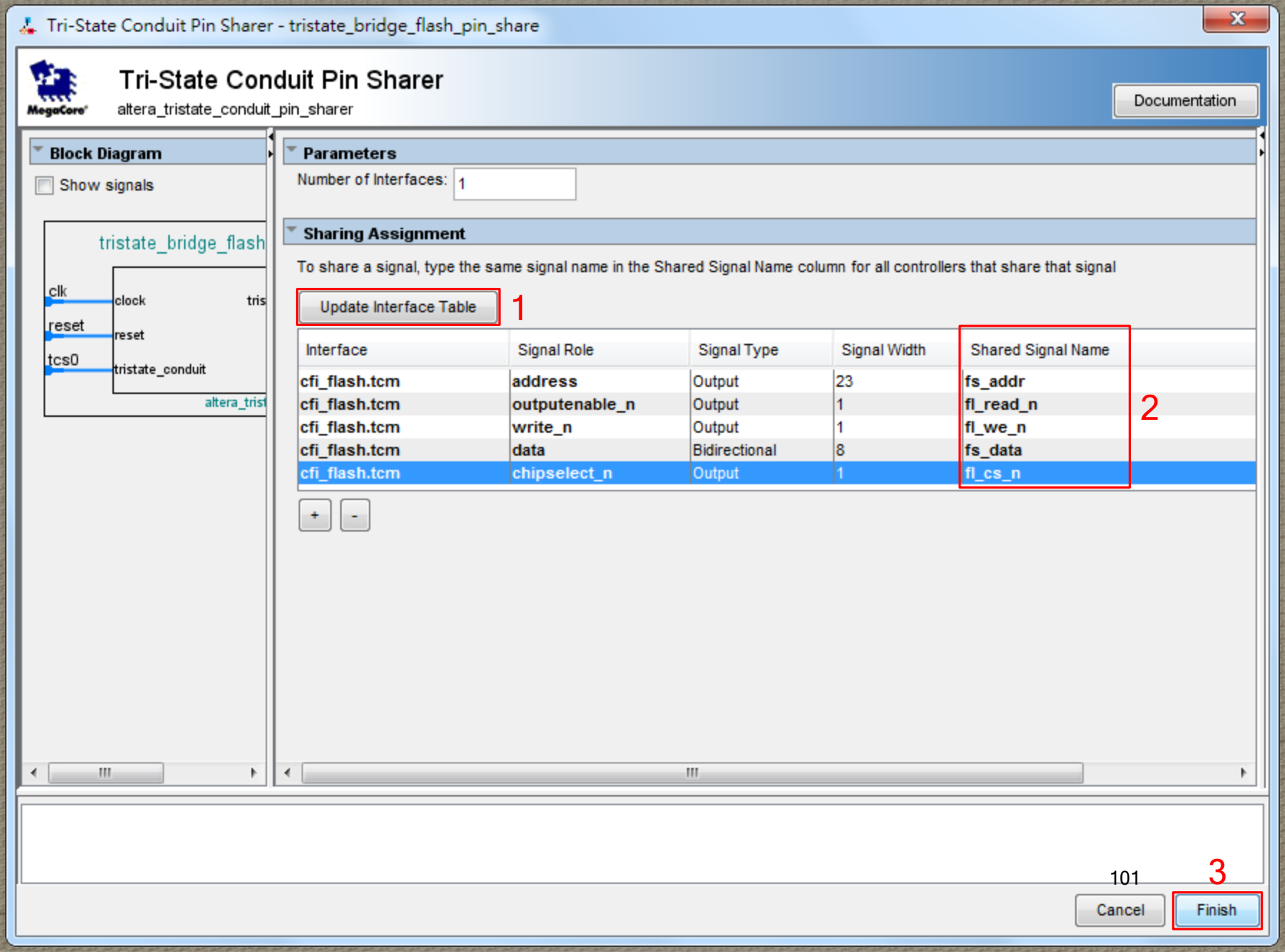
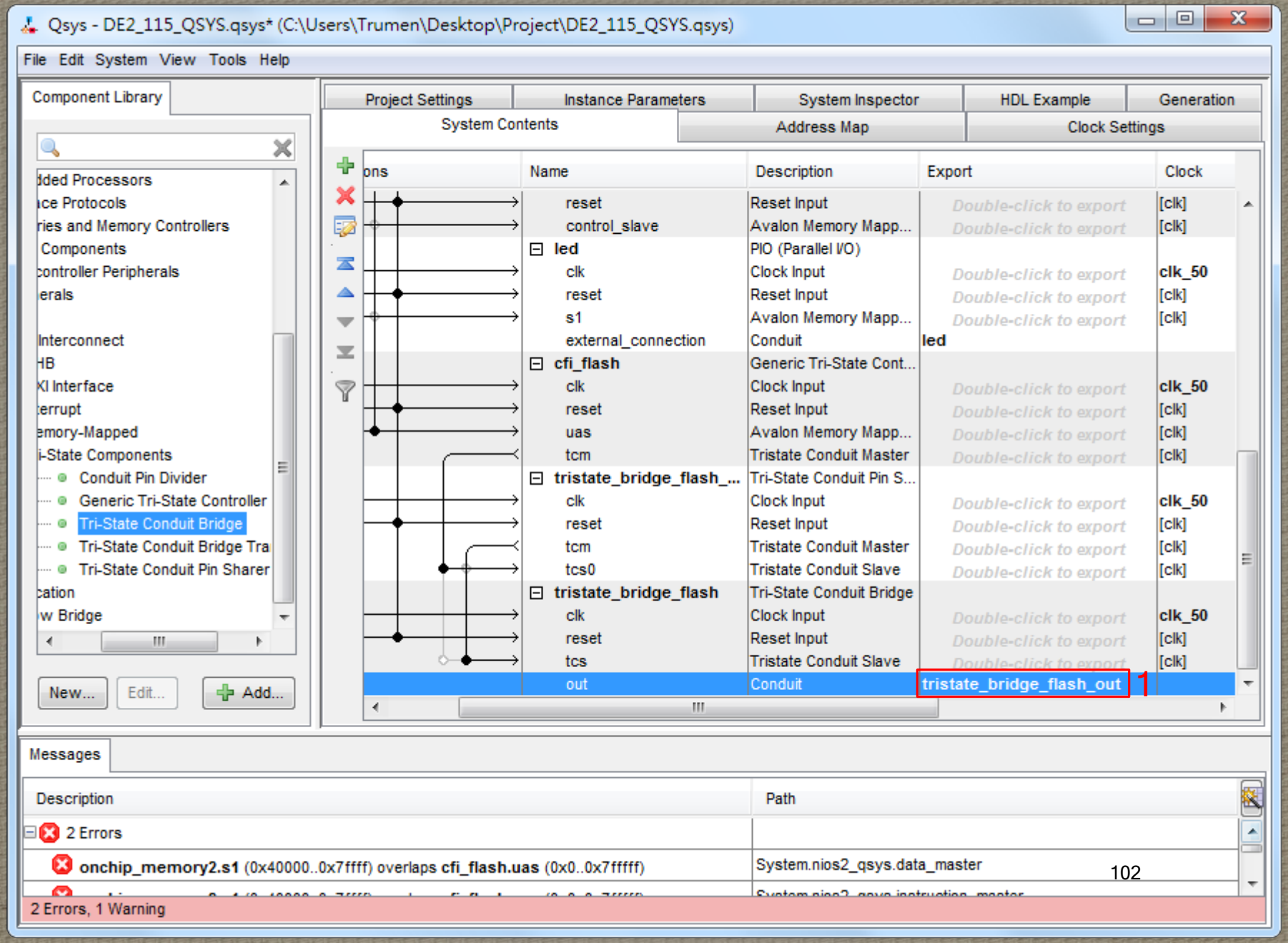
System Contents
Address Map
Clock Settings
Use
Connections
Name
Description
reset
Reset Input
control_slave
Avalon Memory Mapped Slave
led
PIO (Parallel I/O)
clk
Clock Input
reset
Reset Input
s1
Avalon Memory Mapped Slave
external_connection
Conduit
cfi_flash
Generic Tri-State Controller
clk
Clock Input
reset
Reset Input
uas
Avalon Memory Mapped Slave
tcm
Tristate Conduit Master
tristate_bridge_flash_pin_share
Tri-State Conduit Pin Sharer
clk
Clock Input
reset
Reset Input
tcm
Tristate Conduit Master
tcs0
Tristate Conduit Slave
tristate_bridge_flash
Tri-State Conduit Bridge
clk
Clock Input
reset
Reset Input
tcs
Tristate Conduit Slave
out
Conduit
1
2(double-click)
Interconnect
Conduit Pin Divider
Generic Tri-State Controller
Tri-State Conduit Bridge
Tri-State Conduit Bridge Tra
Tri-State Conduit Pin Sharer
New...
Edit...
Add...
Messages
Description
Path
2 Errors
onchip_memory2.s1 (0x40000..0x7ffff) overlaps cfi_flash.uas (0x0..0x7fffff)
System.nios2_qsys.data_master
2 Errors, 2 Warnings
100


Tri-State Conduit Pin Sharer - tristate_bridge_flash_pin_share
Tri-State Conduit Pin Sharer
altera_tristate_conduit_pin_sharer
Documentation
Block Diagram
Show signals
tristate_bridge_flash
clk
clock
reset
reset
tcs0
tristate_conduit
Parameters
Number of Interfaces: 1
Sharing Assignment
To share a signal, type the same signal name in the Shared Signal Name column for all controllers that share that signal
Update Interface Table
1
Interface
Signal Role
Signal Type
Signal Width
Shared Signal Name
cfi_flash.tcm address Output 23 fs_addr
cfi_flash.tcm outputenable_n Output 1 fl_read_n
cfi_flash.tcm write_n Output 1 fl_we_n
cfi_flash.tcm data Bidirectional 8 fs_data
cfi_flash.tcm chipselect_n Output 1 fl_cs_n
2
+
-
101
3
Cancel
Finish


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
File Edit System View Tools Help
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Conduit Pin Divider
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Tri-State Conduit Bridge Tra
Tri-State Conduit Pin Sharer
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Add...
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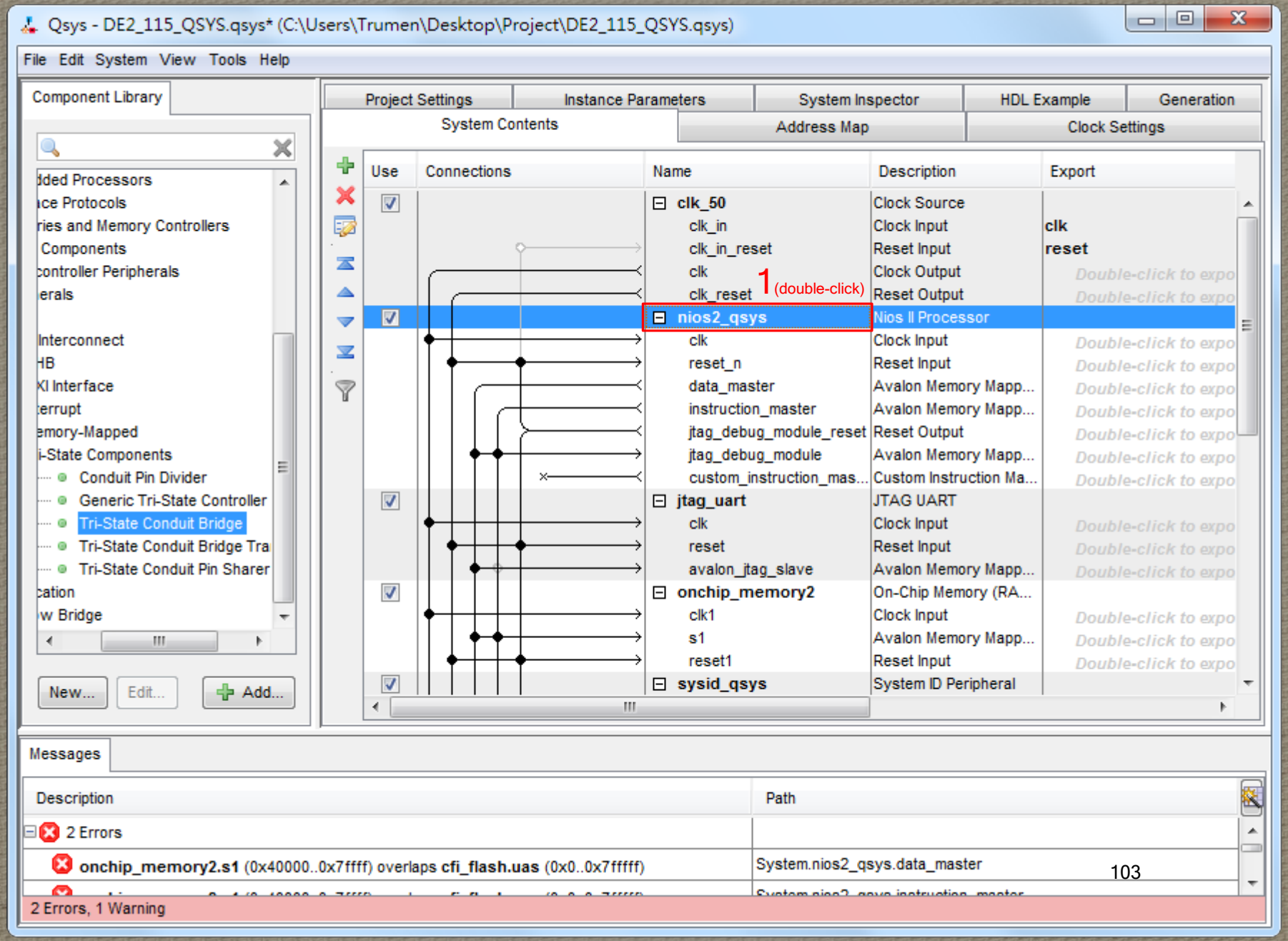
Export
Clock
reset
Reset Input
control_slave
Avalon Memory Mapp...
led
PIO (Parallel I/O)
clk
Clock Input
clk_50
reset
Reset Input
s1
Avalon Memory Mapp...
external_connection
Conduit
cfi_flash
Generic Tri-State Cont...
uas
tcm
Tristate Conduit Master
tristate_bridge_flash_...
Tri-State Conduit Pin S...
tcs0
Tristate Conduit Slave
tristate_bridge_flash
Tri-State Conduit Bridge
tcs
out
tristate_bridge_flash_out
Double-click to export
[clk]
Messages
Description
Path
2 Errors
onchip_memory2.s1 (0x40000..0x7ffff) overlaps cfi_flash.uas (0x0..0x7fffff)
System.nios2_qsys.data_master
2 Errors, 1 Warning


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
File Edit System View Tools Help
Component Library
Conduit Pin Divider
Generic Tri-State Controller
Tri-State Conduit Bridge
Tri-State Conduit Bridge Tra
Tri-State Conduit Pin Sharer
New...
Edit...
Add...
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System Inspector
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Clock Settings
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Connections
Name
Description
Export
clk_50
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
reset
clk
Clock Output
clk_reset
Reset Output
1 (double-click)
nios2_qsys
Nios II Processor
clk
Clock Input
reset_n
Reset Input
data_master
Avalon Memory Mapp...
instruction_master
Avalon Memory Mapp...
jtag_debug_module_reset
Reset Output
jtag_debug_module
Avalon Memory Mapp...
custom_instruction_mas...
Custom Instruction Ma...
jtag_uart
JTAG UART
clk
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reset
Reset Input
avalon_jtag_slave
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onchip_memory2
On-Chip Memory (RA...
clk1
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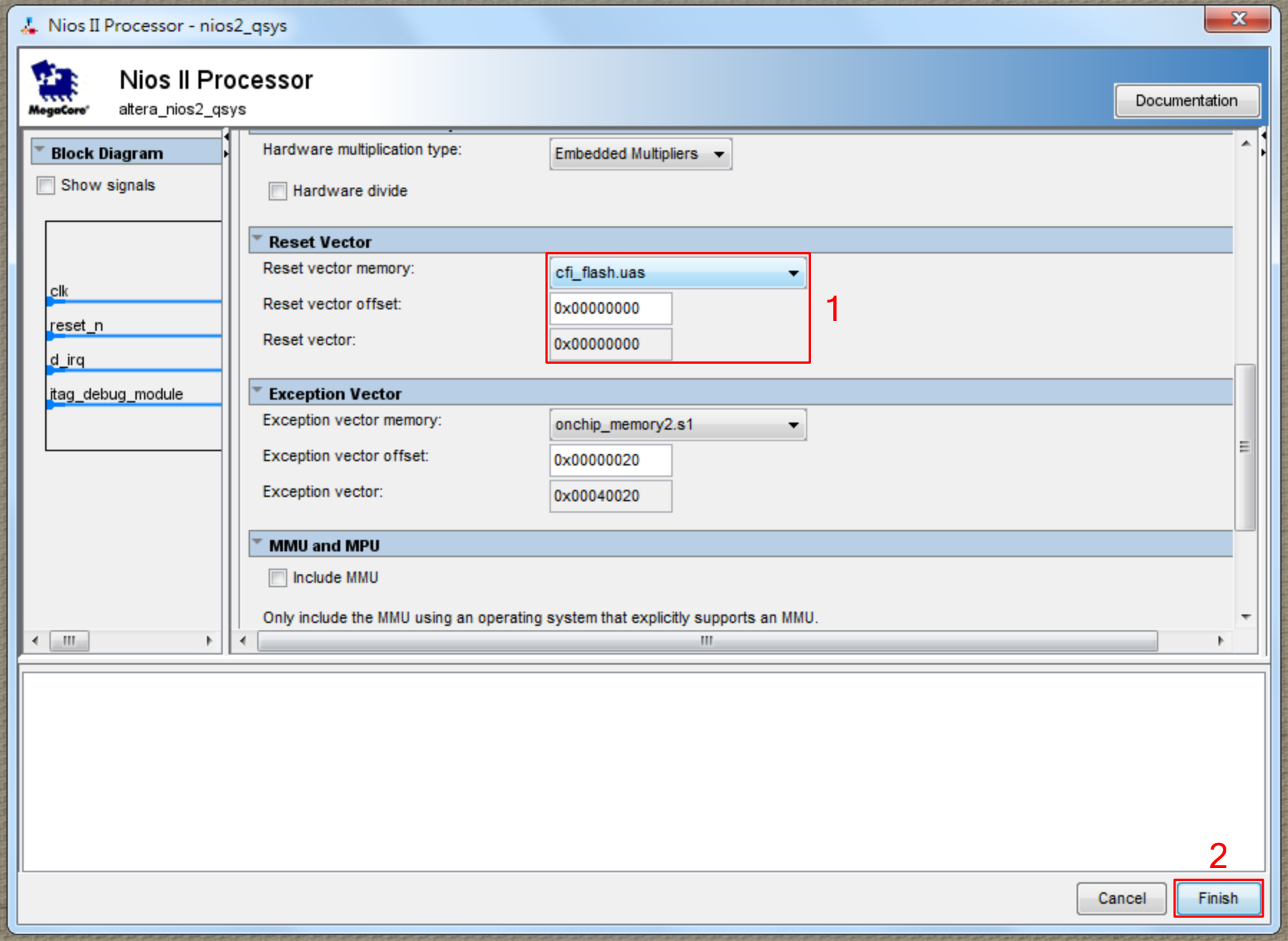
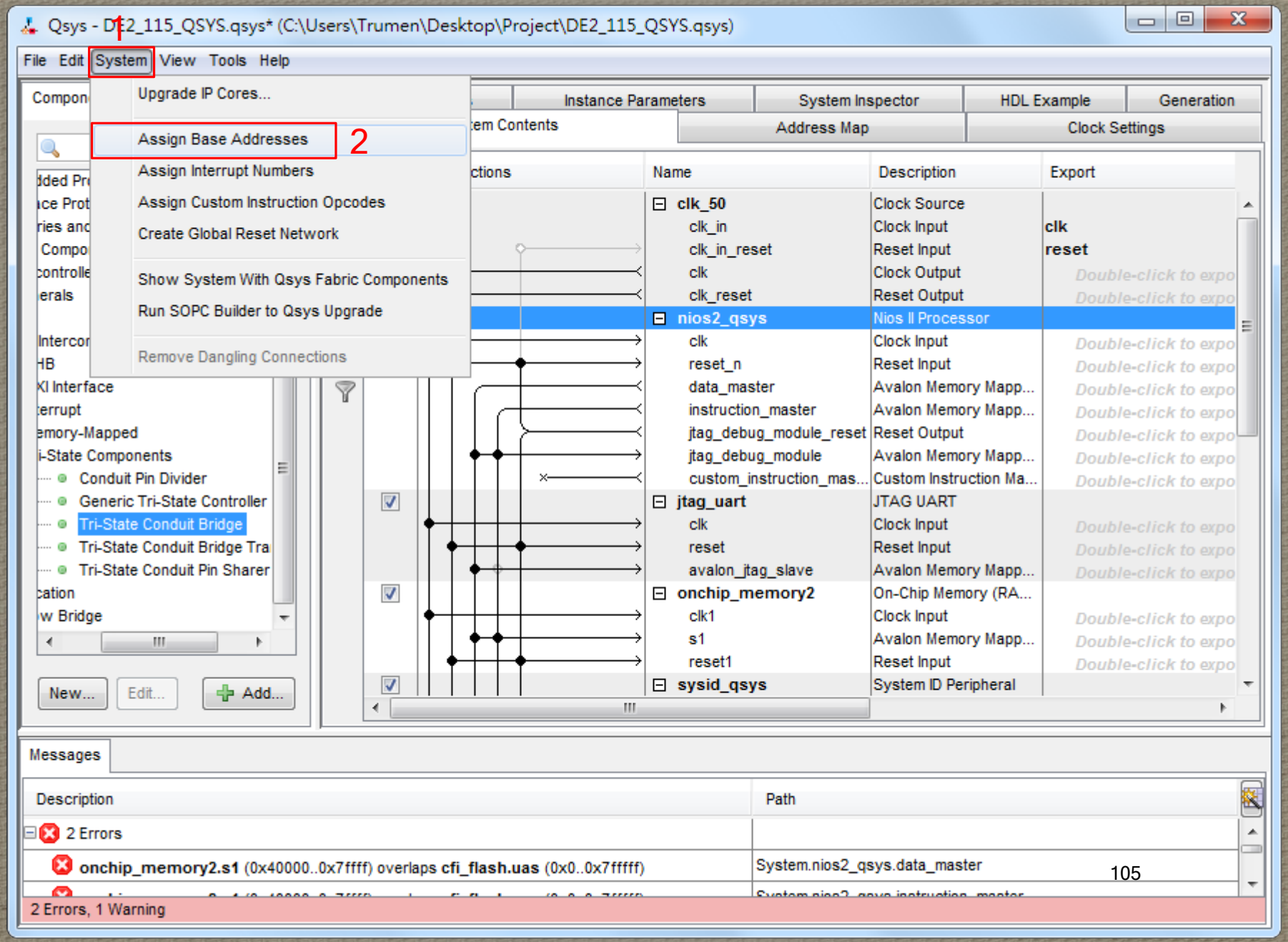
s1
Avalon Memory Mapp...
reset1
Reset Input
sysid_qsys
System ID Peripheral
Double-click to expo
Messages
Description
Path
2 Errors
onchip_memory2.s1 (0x40000..0x7ffff) overlaps cfi_flash.uas (0x0..0x7fffff)
System.nios2_qsys.data_master
2 Errors, 1 Warning


Nios II Processor - nios2_qsys
Nios II Processor
altera_nios2_qsys
Documentation
Block Diagram
Show signals
clk
reset_n
d_irq
jtag_debug_module
Hardware multiplication type:
Embedded Multipliers
Hardware divide
Reset Vector
Reset vector memory:
cfi_flash.uas
Reset vector offset:
0x00000000
Reset vector:
0x00000000
1
Exception Vector
Exception vector memory:
onchip_memory2.s1
Exception vector offset:
0x00000020
Exception vector:
0x00040020
MMU and MPU
Include MMU
Only include the MMU using an operating system that explicitly supports an MMU.
2
Cancel
Finish


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
File Edit System View Tools Help
1
Upgrade IP Cores...
Assign Base Addresses
2
Assign Interrupt Numbers
Assign Custom Instruction Opcodes
Create Global Reset Network
Show System With Qsys Fabric Components
Run SOPC Builder to Qsys Upgrade
Remove Dangling Connections
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Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
reset
clk_reset
Reset Output
nios2_qsys
Nios II Processor
reset_n
data_master
instruction_master
jtag_debug_module_reset
jtag_debug_module
custom_instruction_mas...
jtag_uart
avalon_jtag_slave
onchip_memory2
clk1
s1
reset1
sysid_qsys
System ID Peripheral
Double-click to expo
Conduit Pin Divider
Generic Tri-State Controller
Tri-State Conduit Bridge
Tri-State Conduit Bridge Tra
Tri-State Conduit Pin Sharer
New...
Edit...
Add...
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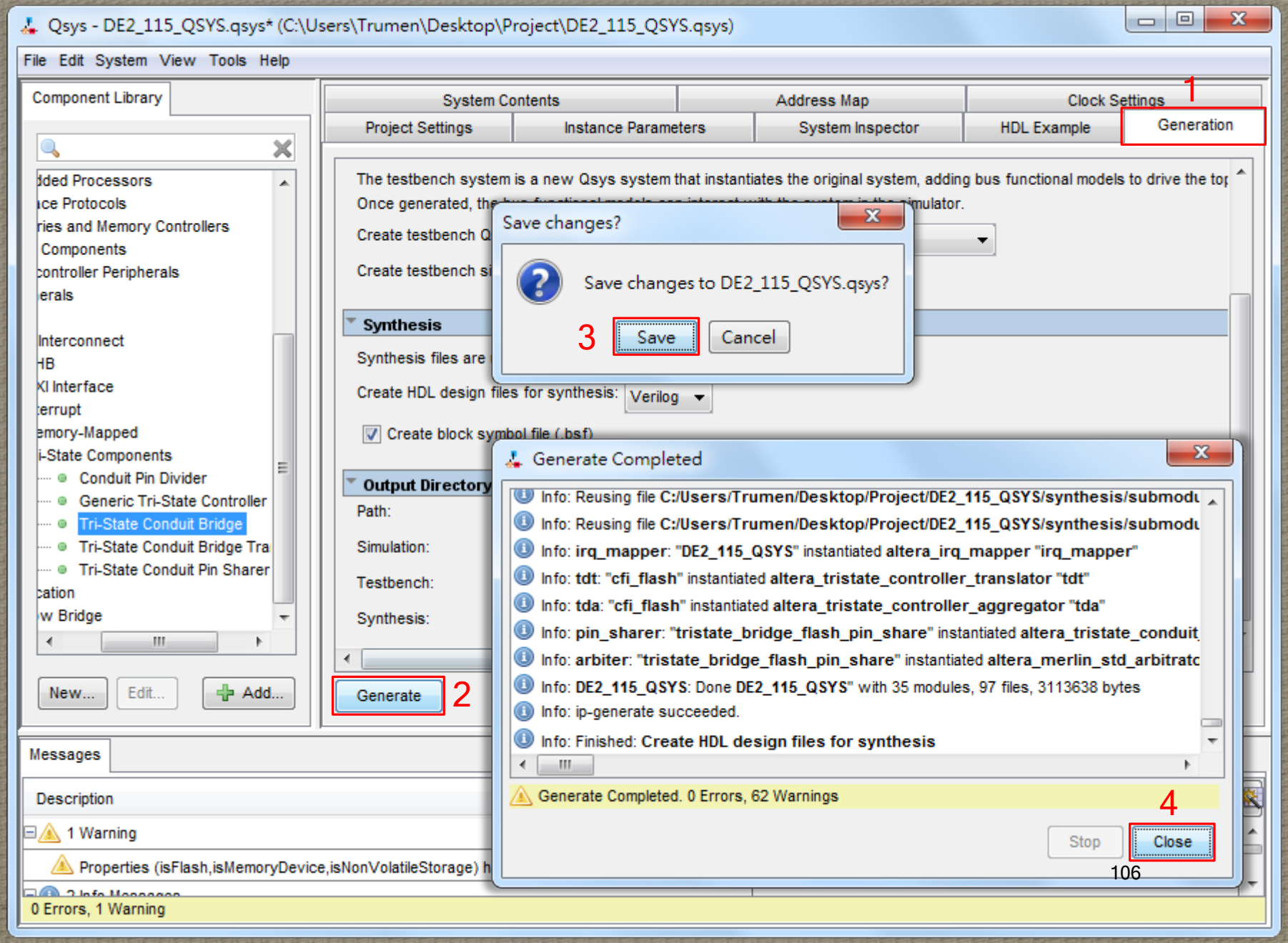
Description
Path
2 Errors
onchip_memory2.s1 (0x40000..0x7ffff) overlaps cfi_flash.uas (0x0..0x7fffff)
System.nios2_qsys.data_master
2 Errors, 1 Warning


Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)
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Component Library
Tri-State Conduit Bridge
New...
Edit...
Add...
System Contents
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Clock Settings
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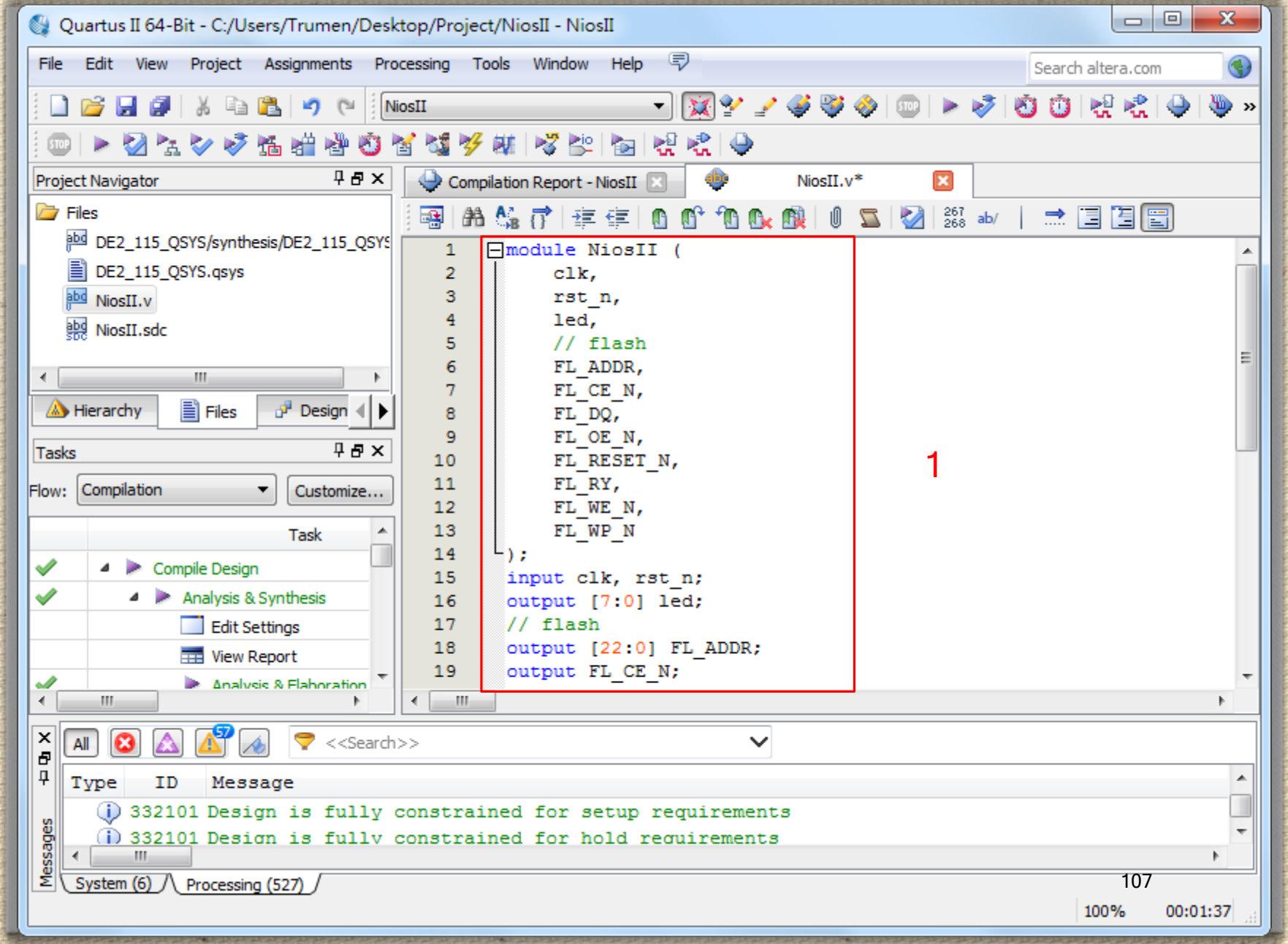
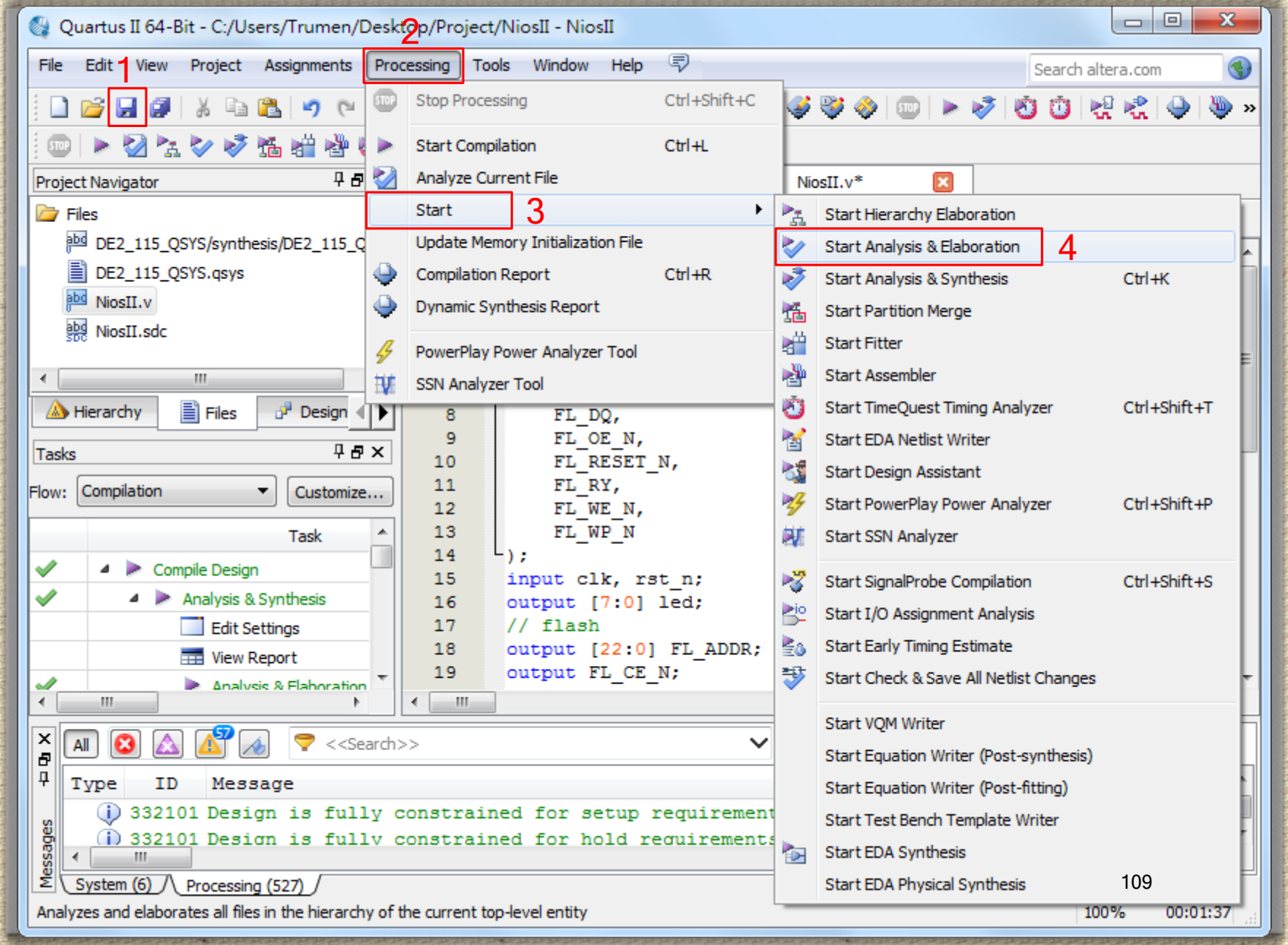
System Inspector
HDL Example
Generation
1
The testbench system is a new Qsys system that instantiates the original system, adding bus functional models to drive the top
Synthesis
Create HDL design files for synthesis:
Verilog
Create block symbol file (.bsf)
Output Directory
Path:
Simulation:
Testbench:
Synthesis:
Generate
2
Save changes?
Save changes to DE2_115_QSYS.qsys?
3
Save
Cancel
Generate Completed
Info: Reusing file C:/Users/Trumen/Desktop/Project/DE2_115_QSYS/synthesis/submodu
Info: Reusing file C:/Users/Trumen/Desktop/Project/DE2_115_QSYS/synthesis/submodu
Info: irq_mapper: "DE2_115_QSYS" instantiated altera_irq_mapper "irq_mapper"
Info: tdt: "cfi_flash" instantiated altera_tristate_controller_translator "tdt"
Info: tda: "cfi_flash" instantiated altera_tristate_controller_aggregator "tda"
Info: pin_sharer: "tristate_bridge_flash_pin_share" instantiated altera_tristate_conduit
Info: arbiter: "tristate_bridge_flash_pin_share" instantiated altera_merlin_std_arbitratc
Info: DE2_115_QSYS: Done DE2_115_QSYS" with 35 modules, 97 files, 3113638 bytes
Info: ip-generate succeeded.
Info: Finished: Create HDL design files for synthesis
Generate Completed. 0 Errors, 62 Warnings
4
Stop
Close
Messages
Description
1 Warning
Properties (isFlash,isMemoryDevice,isNonVolatileStorage) h
0 Errors, 1 Warning
106


Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
NiosII
Project Navigator
Files
DE2_115_QSYS/synthesis/DE2_115_QSYS
DE2_115_QSYS.qsys
NiosII.v
NiosII.sdc
Hierarchy Files Design
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Compilation Report - NiosII
NiosII.v*
1 module NiosII (
2 clk,
3 rst_n,
4 led,
5 // flash
6 FL_ADDR,
7 FL_CE_N,
8 FL_DQ,
9 FL_OE_N,
10 FL_RESET_N,
11 FL_RY,
12 FL_WE_N,
13 FL_WP_N
14);
15 input clk, rst_n;
16 output [7:0] led;
17 // flash
18 output [22:0] FL_ADDR;
19 output FL_CE_N;
1
All
<<Search>>
Type ID Message
332101 Design is fully constrained for setup requirements
332101 Design is fully constrained for hold requirements
Messages
System (6)
Processing (527)
100%
00:01:37

```
module NiosII (
    clk,
    rst_n,
    led,
    // flash
    FL_ADDR,
    FL_CE_N,
    FL_DQ,
    FL_OE_N,
    FL_RESET_N,
    FL_RY,
    FL_WE_N,
    FL_WP_N
);
input clk, rst_n;
output [7:0] led;
// flash
output [22:0] FL_ADDR;
output FL_CE_N;
inout [7:0] FL_DQ;
output FL_OE_N;
output FL_RESET_N;
input FL_RY;
output FL_WE_N;
output FL_WP_N;
DE2_115_QSYS DE2_115_QSYS_inst (
    .clk_clk(clk),
    .reset_reset_n(rst_n),
    .led_export(led),
    // flash
    .tristate_bridge_flash_out_fs_addr(FL_ADDR),
    .tristate_bridge_flash_out_fl_read_n(FL_OE_N),
    .tristate_bridge_flash_out_fl_cs_n(FL_CE_N),
    .tristate_bridge_flash_out_fs_data(FL_DQ),
    .tristate_bridge_flash_out_fl_we_n(FL_WE_N),
);
// flash config
assign FL_RESET_N = 1'b1;
assign FL_WP_N = 1'b1;
endmodule
```


Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
File
Edit
View
Project
Assignments
Processing
Tools
Window
Help
1
2
3
4
Stop Processing Ctrl+Shift+C
Start Compilation Ctrl+L
Analyze Current File
Start
Update Memory Initialization File
Compilation Report Ctrl+R
Dynamic Synthesis Report
PowerPlay Power Analyzer Tool
SSN Analyzer Tool
Start Hierarchy Elaboration
Start Analysis & Elaboration
Start Analysis & Synthesis Ctrl+K
Start Partition Merge
Start Fitter
Start Assembler
Start TimeQuest Timing Analyzer Ctrl+Shift+T
Start EDA Netlist Writer
Start Design Assistant
Start PowerPlay Power Analyzer Ctrl+Shift+P
Start SSN Analyzer
Start SignalProbe Compilation Ctrl+Shift+S
Start I/O Assignment Analysis
Start Early Timing Estimate
Start Check & Save All Netlist Changes
Start VQM Writer
Start Equation Writer (Post-synthesis)
Start Equation Writer (Post-fitting)
Start Test Bench Template Writer
Start EDA Synthesis
Start EDA Physical Synthesis
Project Navigator
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DE2_115_QSYS.qsys
NiosII.v
NiosII.sdc
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Compile Design
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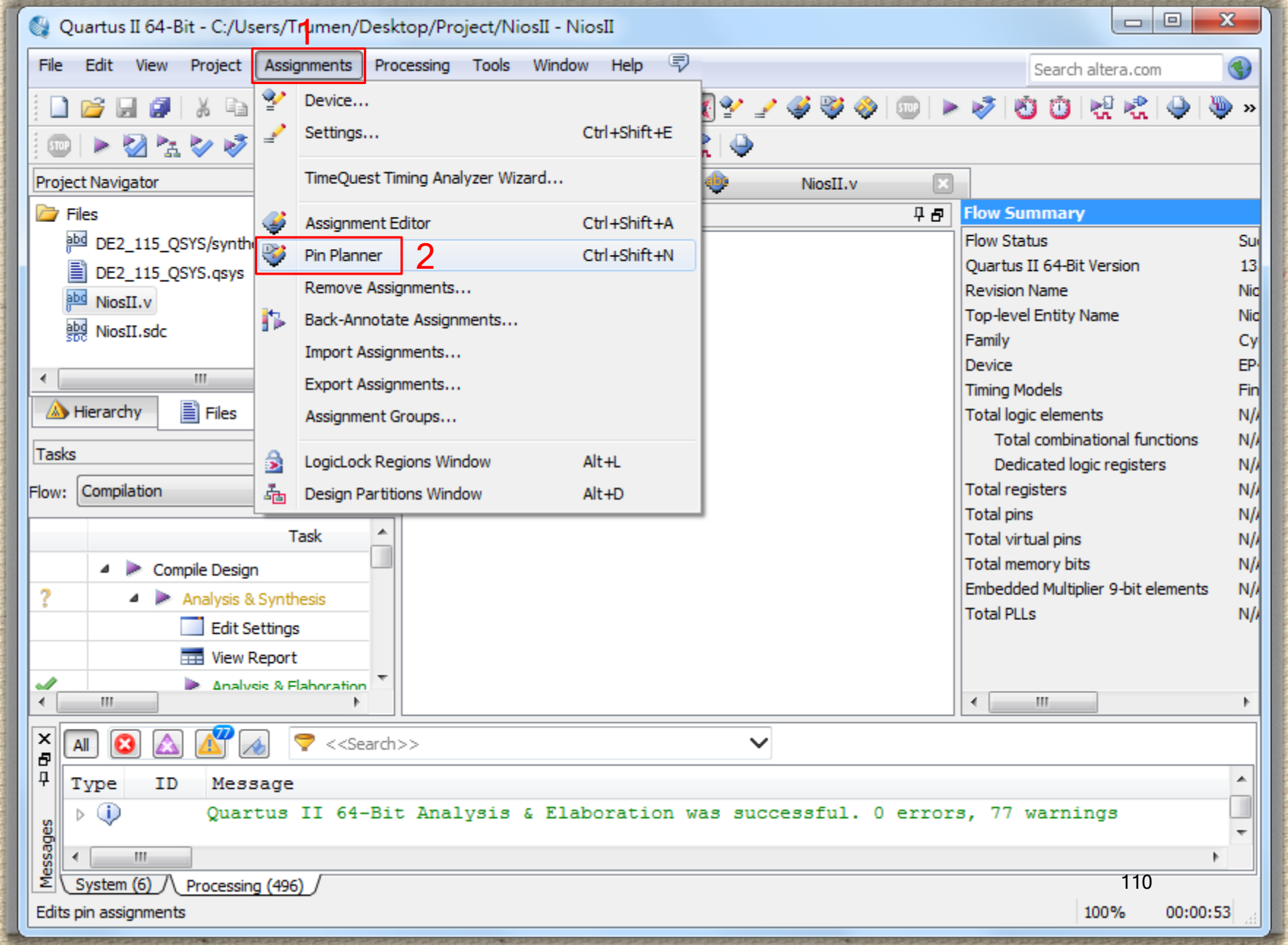
Edit Settings
View Report
NiosII.v*
FL_DQ,
FL_OE_N,
FL_RESET_N,
FL_RY,
FL_WE_N,
FL_WP_N
);
input clk, rst_n;
output [7:0] led;
// flash
output [22:0] FL_ADDR;
output FL_CE_N;
All
<<Search>>
Type ID Message
332101 Design is fully constrained for setup requirement
332101 Design is fully constrained for hold requirements
Messages
System (6)
Processing (527)
Analyzes and elaborates all files in the hierarchy of the current top-level entity
100%
00:01:37
109


Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
1
File
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Search altera.com
Device...
Settings... Ctrl+Shift+E
TimeQuest Timing Analyzer Wizard...
Assignment Editor Ctrl+Shift+A
Pin Planner Ctrl+Shift+N
2
Remove Assignments...
Back-Annotate Assignments...
Import Assignments...
Export Assignments...
Assignment Groups...
LogicLock Regions Window Alt+L
Design Partitions Window Alt+D
Project Navigator
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DE2_115_QSYS.qsys
NiosII.v
NiosII.sdc
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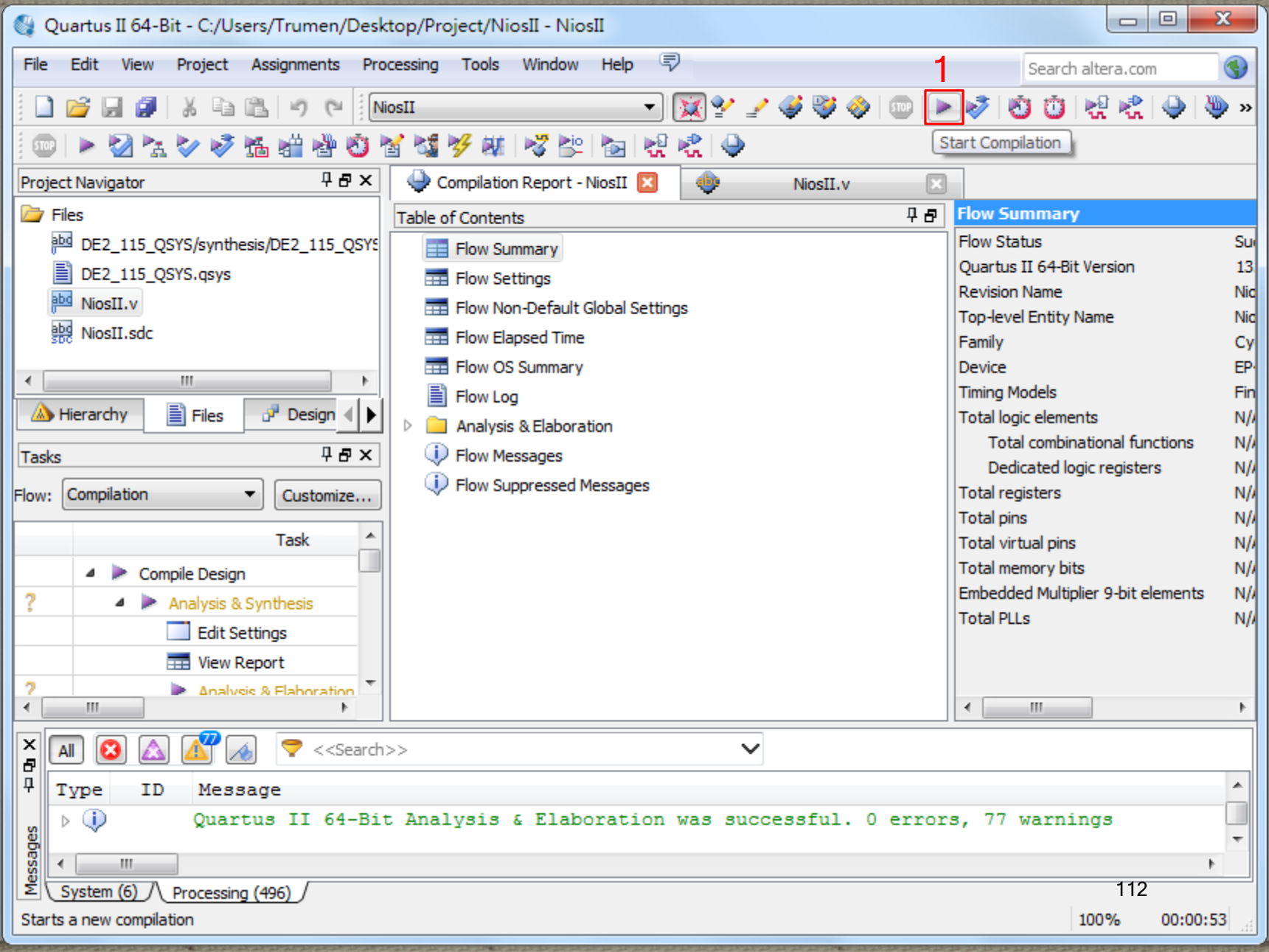
Flow Status
Quartus II 64-Bit Version 13
Revision Name
Top-level Entity Name
Family
Device
Timing Models
Total logic elements
Total combinational functions
Dedicated logic registers
Total registers
Total pins
Total virtual pins
Total memory bits
Embedded Multiplier 9-bit elements
Total PLLs
All
77
<<Search>>
Type ID Message
Quartus II 64-Bit Analysis & Elaboration was successful. 0 errors, 77 warnings
Messages
System (6)
Processing (496)
Edits pin assignments
100%
00:00:53

Node Name	Direction	Location
FL_ADDR[0]	Output	PIN_AG12
FL_ADDR[1]	Output	PIN_AH7
FL_ADDR[2]	Output	PIN_Y13
FL_ADDR[3]	Output	PIN_Y14
FL_ADDR[4]	Output	PIN_Y12
FL_ADDR[5]	Output	PIN_AA13
FL_ADDR[6]	Output	PIN_AA12
FL_ADDR[7]	Output	PIN_AB13
FL_ADDR[8]	Output	PIN_AB12
FL_ADDR[9]	Output	PIN_AB10
FL_ADDR[10]	Output	PIN_AE9
FL_ADDR[11]	Output	PIN_AF9
FL_ADDR[12]	Output	PIN_AA10
FL_ADDR[13]	Output	PIN_AD8
FL_ADDR[14]	Output	PIN_AC8
FL_ADDR[15]	Output	PIN_Y10
FL_ADDR[16]	Output	PIN_AA8
FL_ADDR[17]	Output	PIN_AH12
FL_ADDR[18]	Output	PIN_AC12
FL_ADDR[19]	Output	PIN_AD12
FL_ADDR[20]	Output	PIN_AE10
FL_ADDR[21]	Output	PIN_AD10
FL_ADDR[22]	Output	PIN_AD11
FL_CE_N	Output	PIN_AG7
FL_DQ[0]	Bidir	PIN_AH8

Node Name	Direction	Location
FL_CE_N	Output	PIN_AG7
FL_DQ[0]	Bidir	PIN_AH8
FL_DQ[1]	Bidir	PIN_AF10
FL_DQ[2]	Bidir	PIN_AG10
FL_DQ[3]	Bidir	PIN_AH10
FL_DQ[4]	Bidir	PIN_AF11
FL_DQ[5]	Bidir	PIN_AG11
FL_DQ[6]	Bidir	PIN_AH11
FL_DQ[7]	Bidir	PIN_AF12
FL_OE_N	Output	PIN_AG8
FL_RESET_N	Output	PIN_AE11
FL_RY	Input	PIN_Y1
FL_WE_N	Output	PIN_AC10
FL_WP_N	Output	PIN_AE12
clk	Input	PIN_Y2
led[0]	Output	PIN_E21
led[1]	Output	PIN_E22
led[2]	Output	PIN_E25
led[3]	Output	PIN_E24
led[4]	Output	PIN_H21
led[5]	Output	PIN_G20
led[6]	Output	PIN_G22
led[7]	Output	PIN_G21
rst_n	Input	PIN_M23
<<new node>>		


Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
1
NiosII
Start Compilation
Project Navigator
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DE2_115_QSYS.qsys
NiosII.v
NiosII.sdc
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Compilation Report - NiosII
NiosII.v
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Flow OS Summary
Flow Log
Analysis & Elaboration
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Flow Suppressed Messages
Flow Summary
Flow Status
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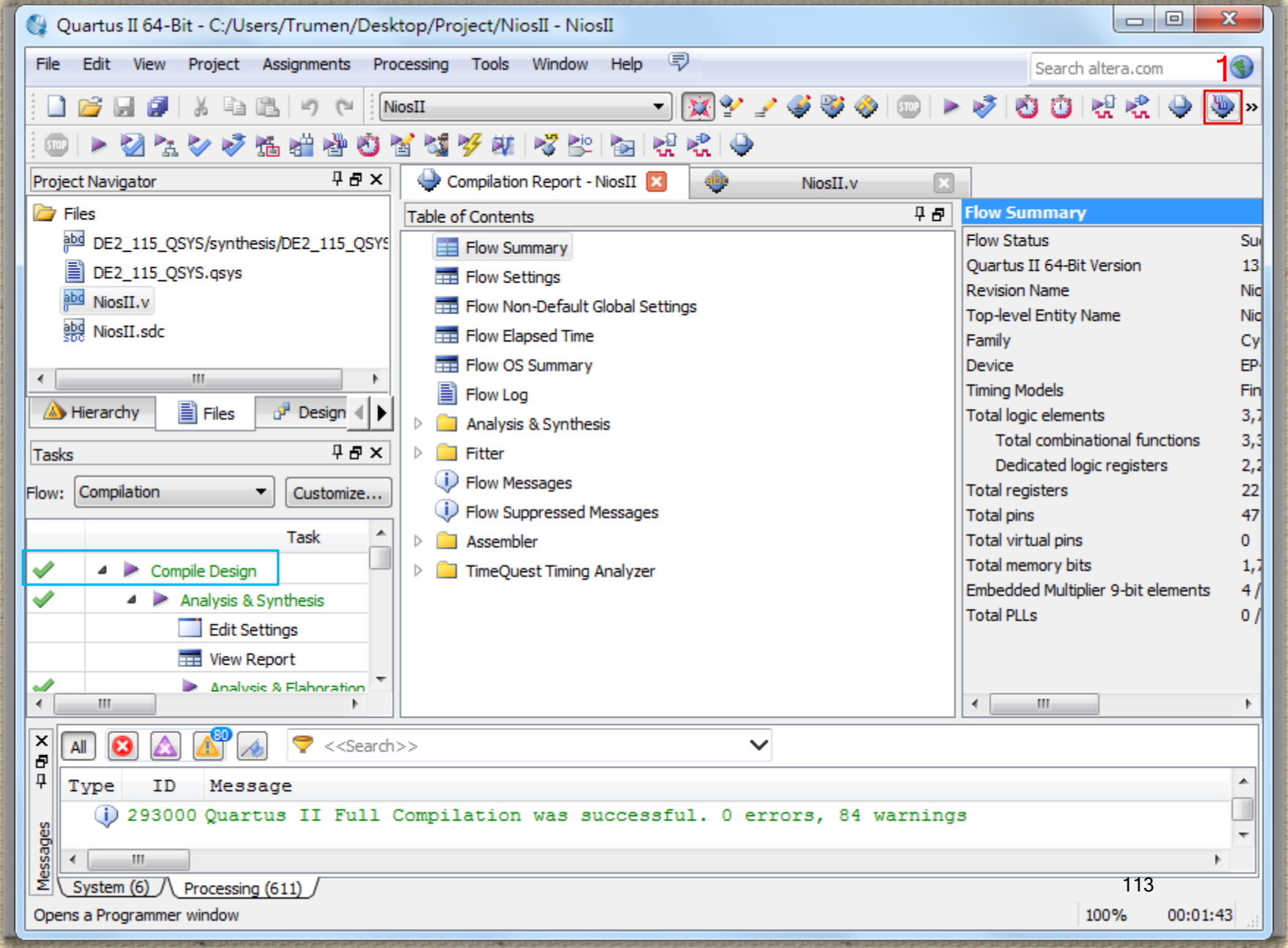
Device
Timing Models
Total logic elements
Total combinational functions
Dedicated logic registers
Total registers
Total pins
Total virtual pins
Total memory bits
Embedded Multiplier 9-bit elements
Total PLLs
All
<<Search>>
Type ID Message
Quartus II 64-Bit Analysis & Elaboration was successful. 0 errors, 77 warnings
Messages
System (6) Processing (496)
Starts a new compilation
100%
00:00:53


Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
File Edit View Project Assignments Processing Tools Window Help
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NiosII
Project Navigator
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DE2_115_QSYS/synthesis/DE2_115_QSYS
DE2_115_QSYS.qsys
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TimeQuest Timing Analyzer
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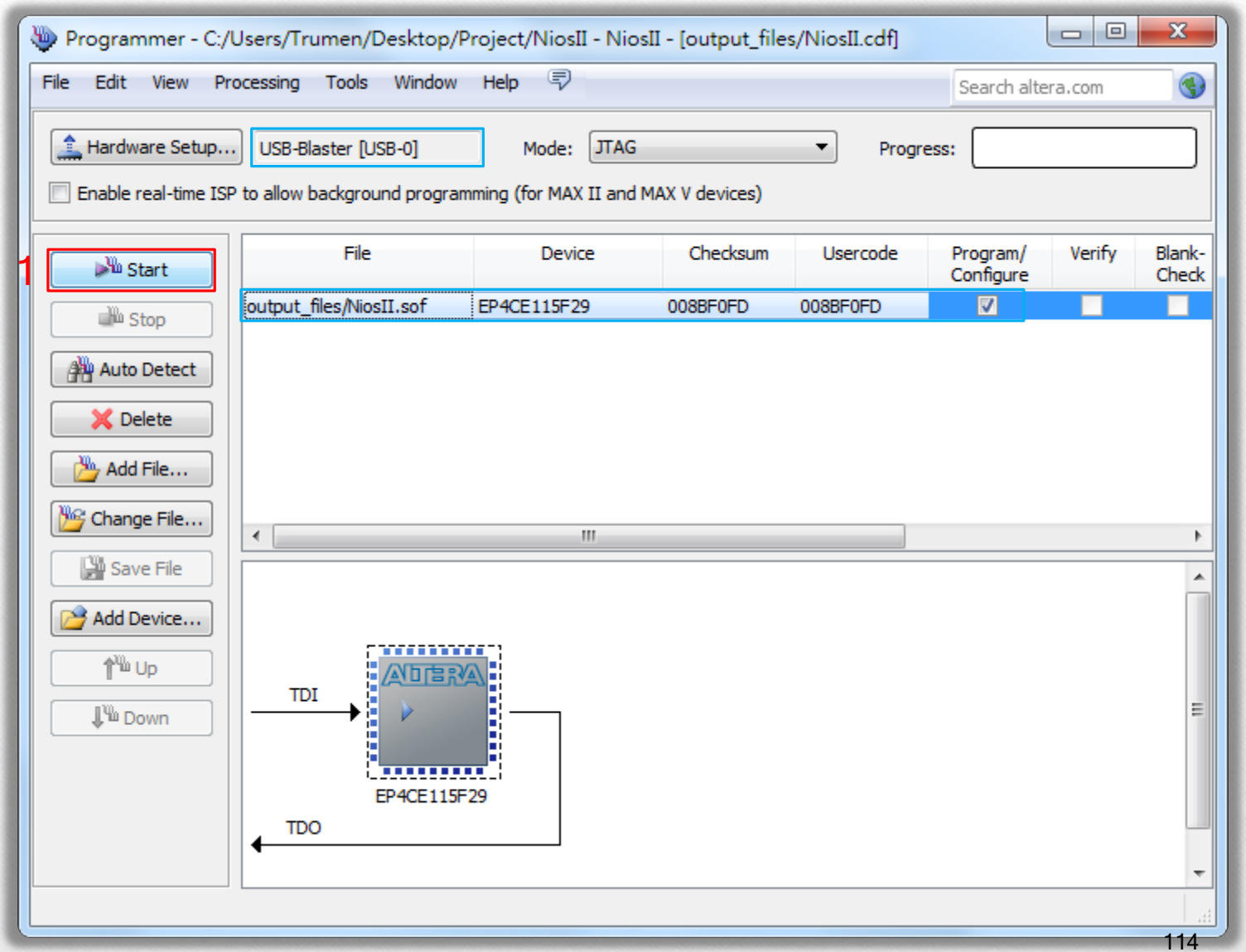
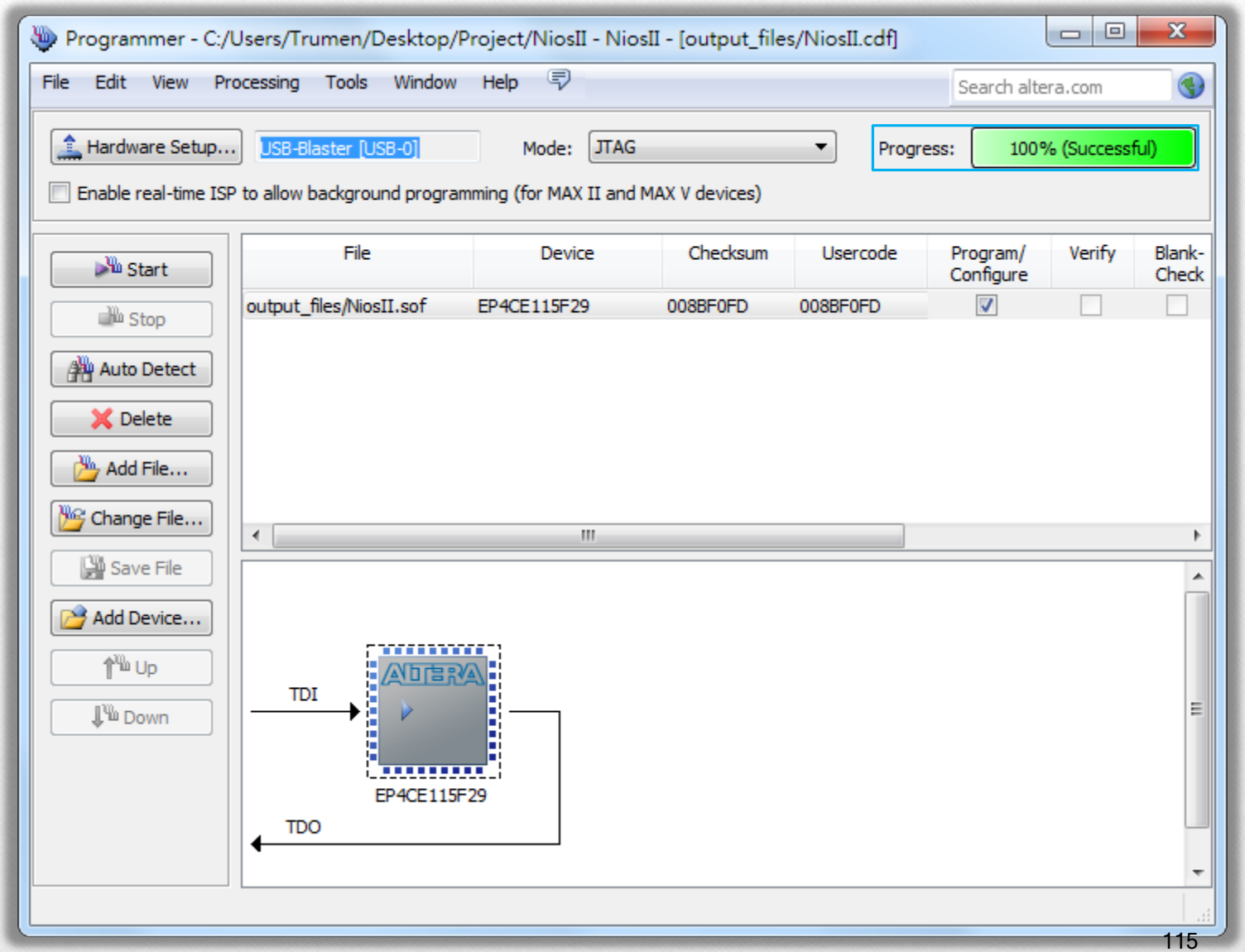
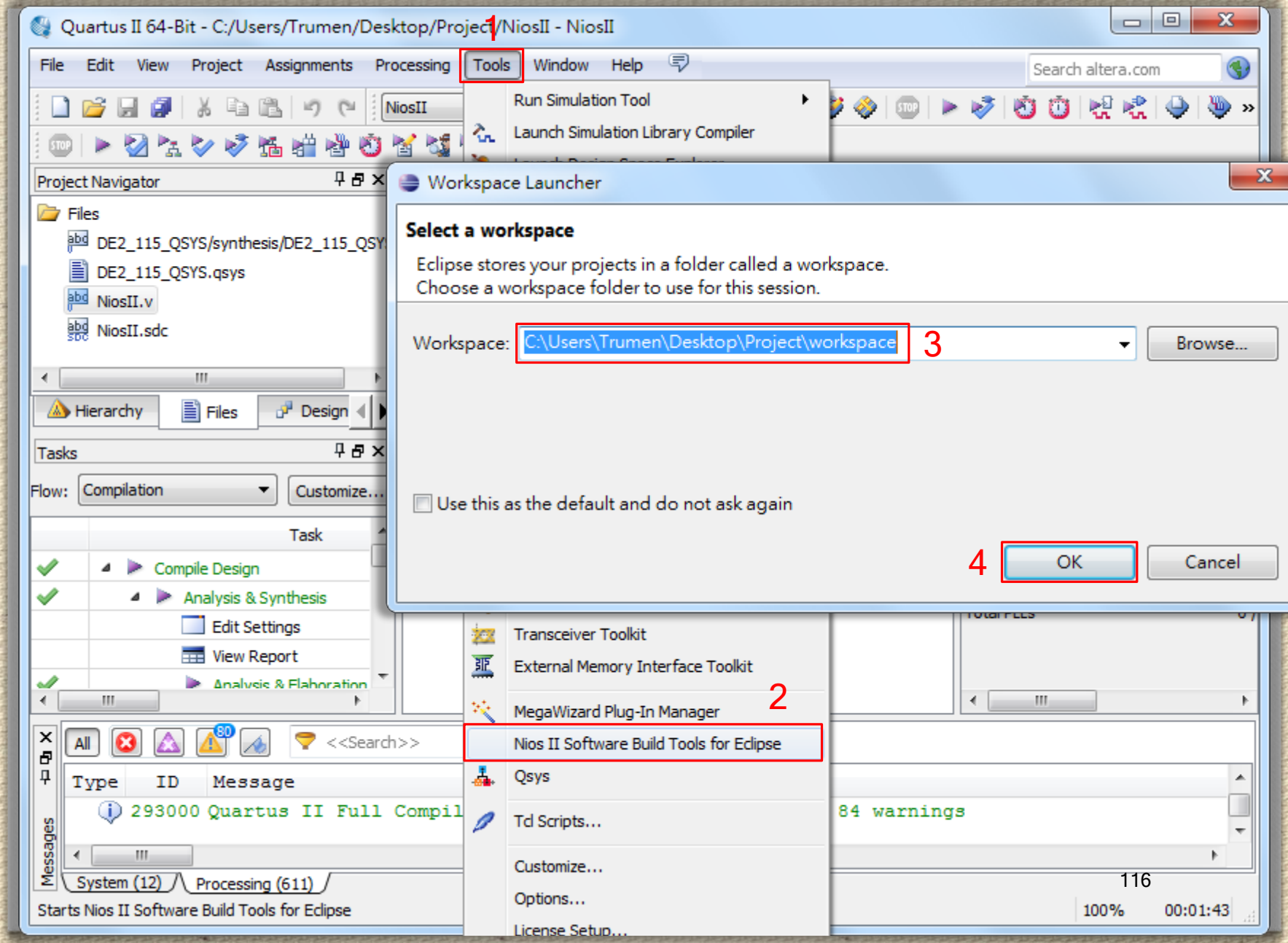
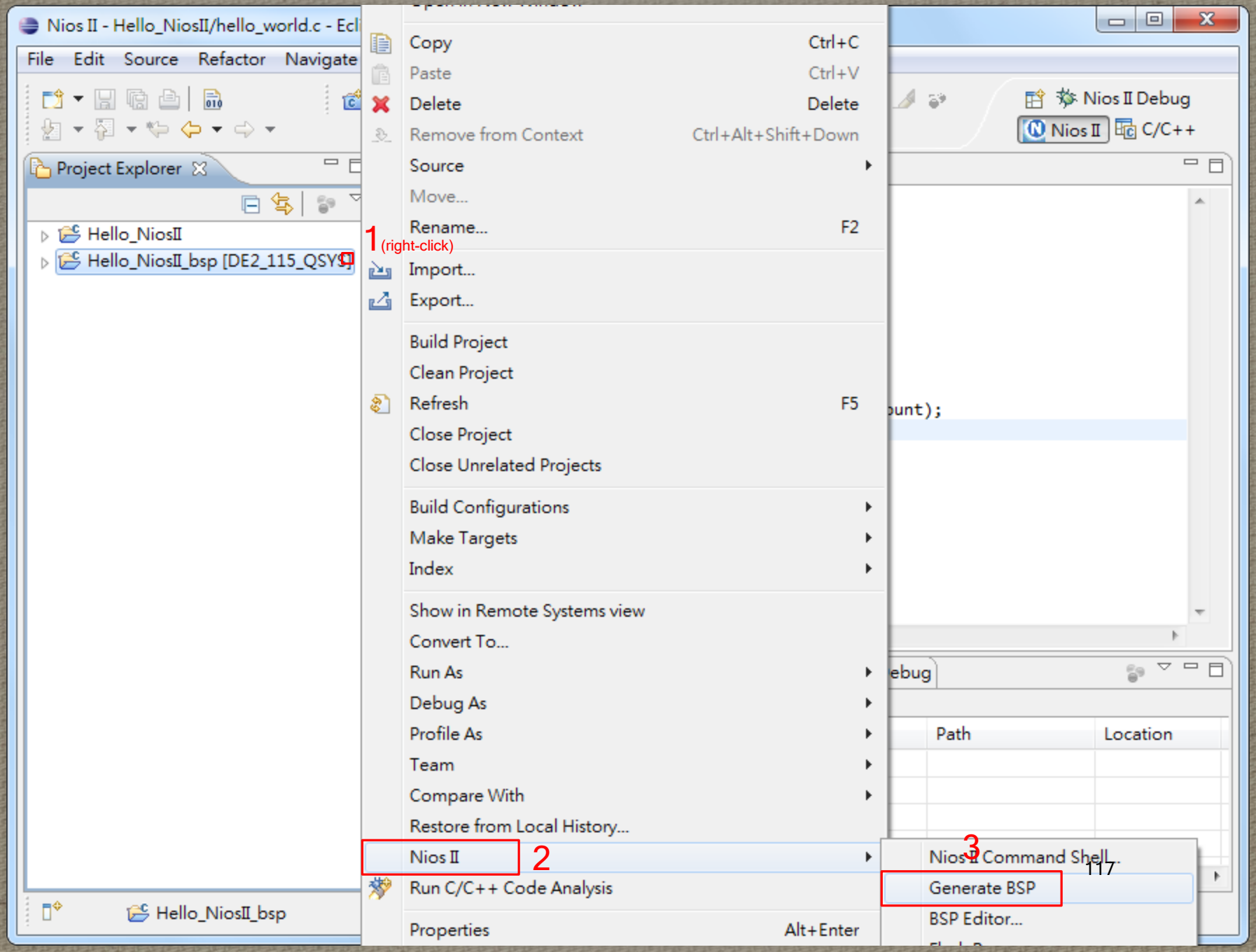
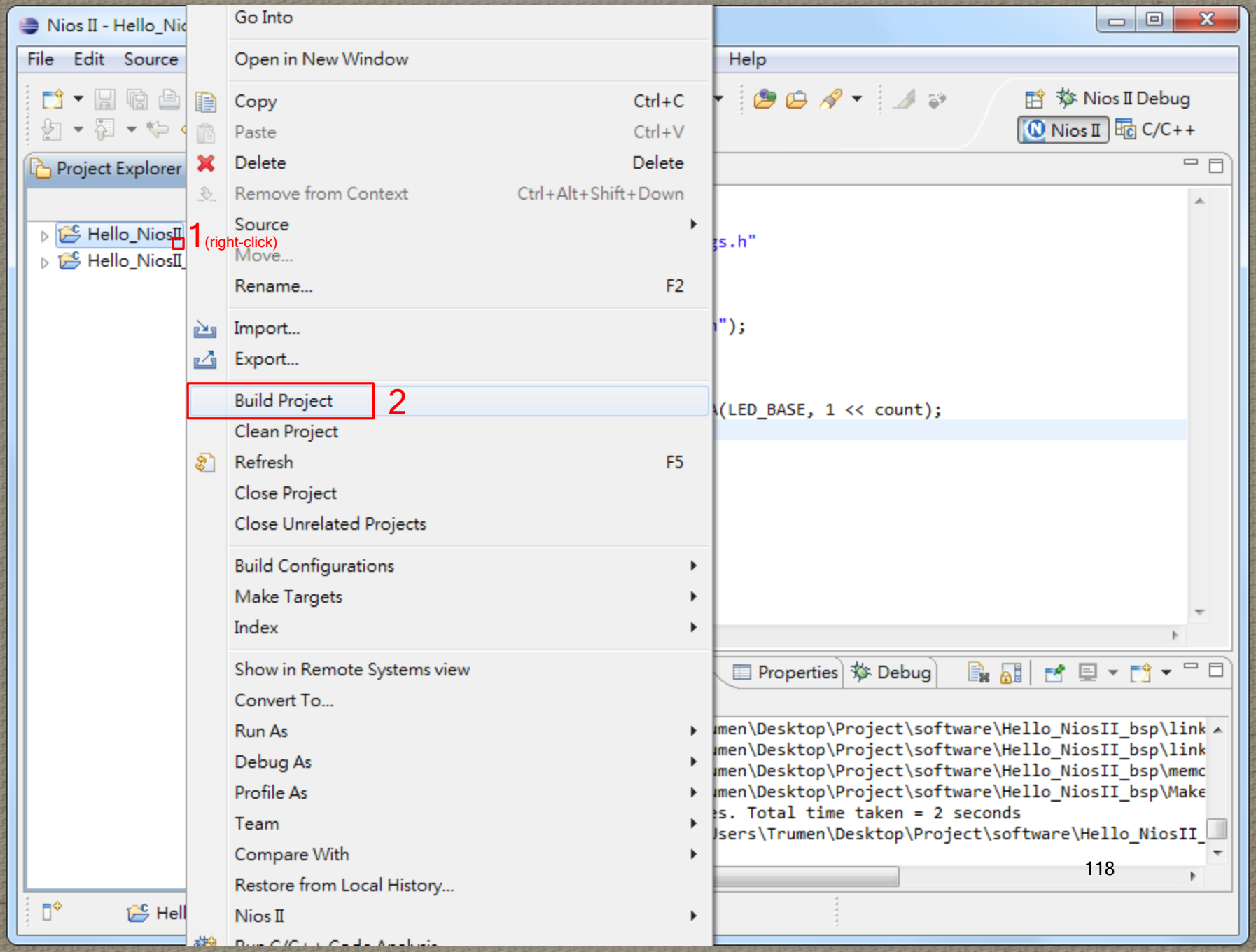
Quartus II 64-Bit Version
Revision Name
Top-level Entity Name
Family
Device
Timing Models
Total logic elements
Total combinational functions
Dedicated logic registers
Total registers
Total pins
Total virtual pins
Total memory bits
Embedded Multiplier 9-bit elements
Total PLLs
All
<<Search>>
Type ID Message
293000 Quartus II Full Compilation was successful. 0 errors, 84 warnings
Messages
System (6) Processing (611)
Opens a Programmer window
100%
00:01:43

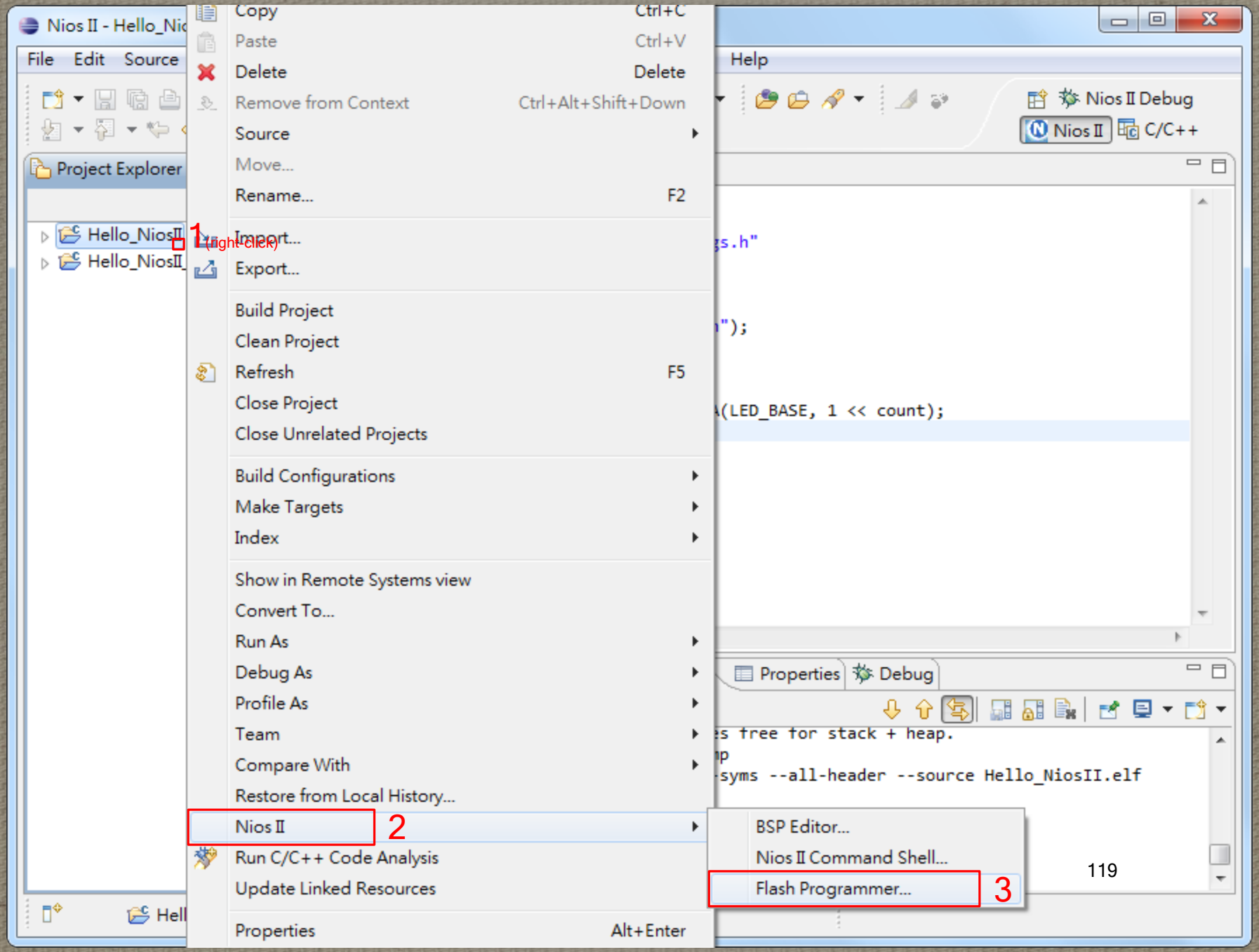

Programmer - C:/Users/Trumen/Desktop/Project/NiosII - NiosII - [output_files/NiosII.cdf]
File Edit View Processing Tools Window Help
Search altera.com
Hardware Setup...
USB-Blaster [USB-0]
Mode: JTAG
Progress:
Enable real-time ISP to allow background programming (for MAX II and MAX V devices)
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File
Device
Checksum
Usercode
Program/ Configure
Verify
Blank-Check
output_files/NiosII.sof
EP4CE115F29
008BF0FD
008BF0FD
TDI
TDO
EP4CE115F29

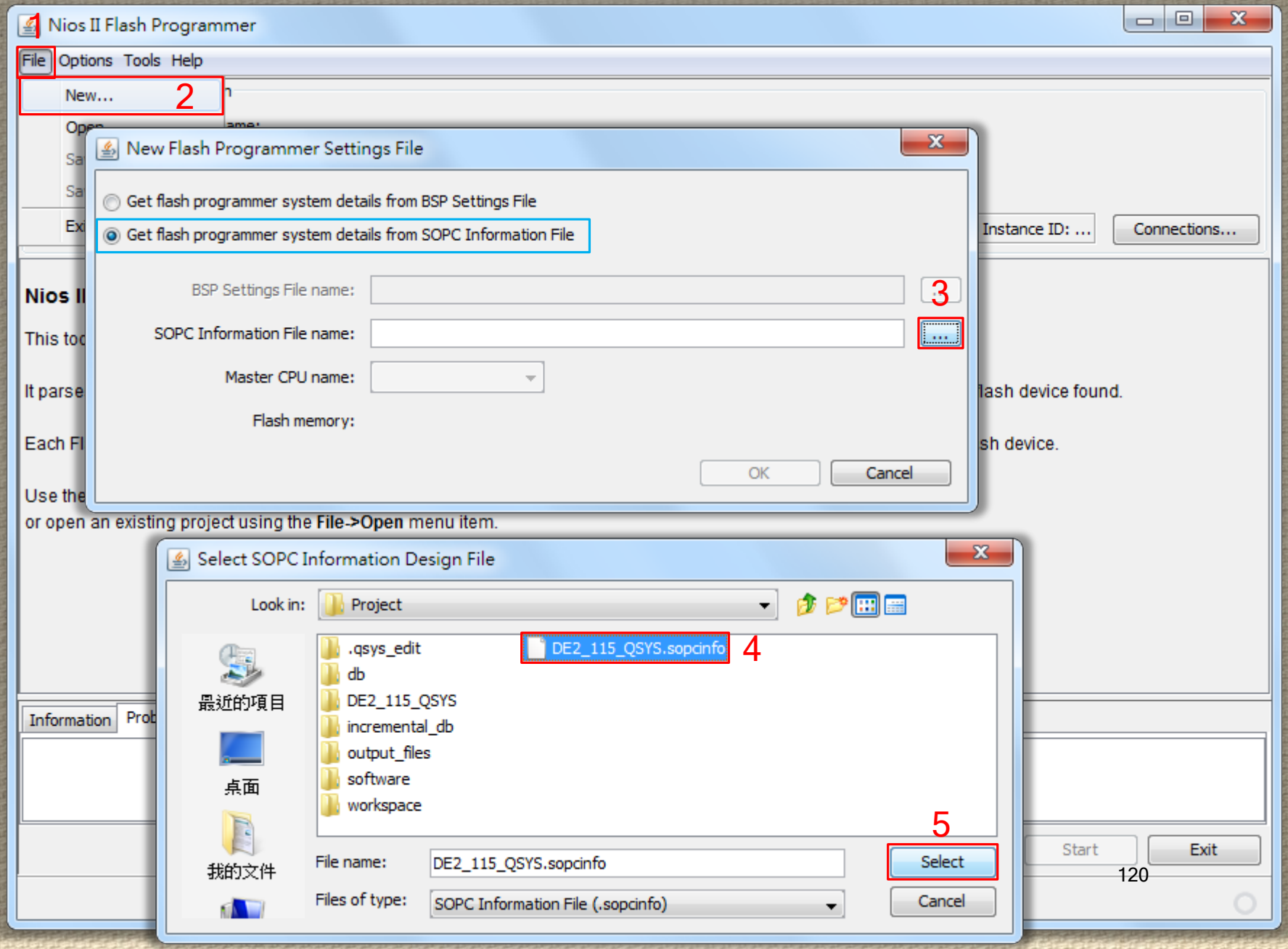

Programmer - C:/Users/Trumen/Desktop/Project/NiosII - NiosII - [output_files/NiosII.cdf]
File Edit View Processing Tools Window Help
Search altera.com
Hardware Setup...
USB-Blaster [USB-0]
Mode: JTAG
Progress: 100% (Successful)
Enable real-time ISP to allow background programming (for MAX II and MAX V devices)
Start
Stop
Auto Detect
Delete
Add File...
Change File...
Save File
Add Device...
Up
Down
File Device Checksum Usercode Program/ Configure Verify Blank-Check
output_files/NiosII.sof EP4CE115F29 008BF0FD 008BF0FD
TDI
TDO
EP4CE115F29

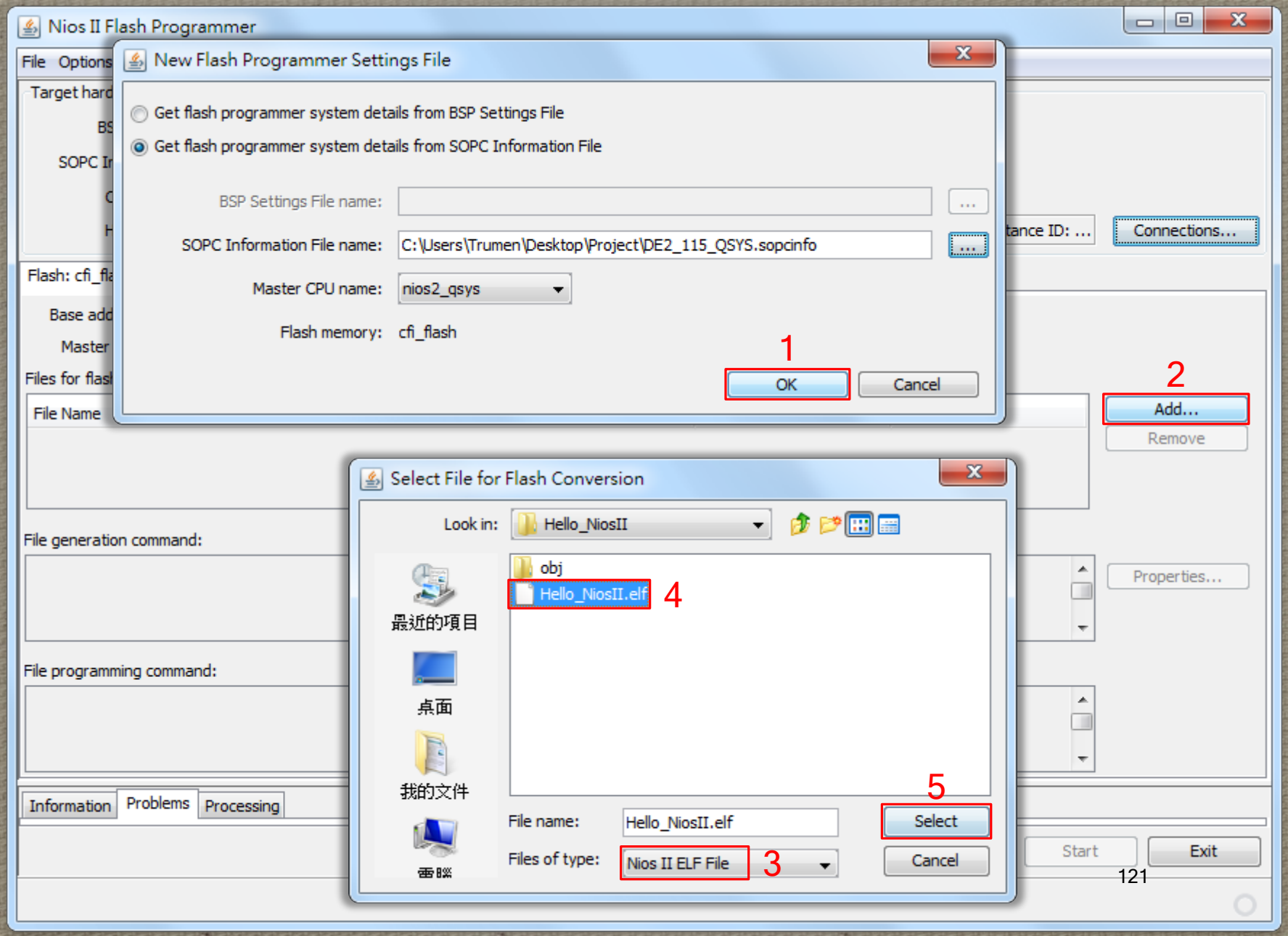

Quartus II 64-Bit - C:/Users/Trumen/Desktop/Project/NiosII - NiosII
1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Run Simulation Tool
Launch Simulation Library Compiler
Workspace Launcher
Select a workspace
Eclipse stores your projects in a folder called a workspace.
Choose a workspace folder to use for this session.
Workspace: C:\Users\Trumen\Desktop\Project\workspace
3
Browse...
Use this as the default and do not ask again
4
OK
Cancel
Project Navigator
Files
DE2_115_QSYS/synthesis/DE2_115_QSY
DE2_115_QSYS.qsys
NiosII.v
NiosII.sdc
Hierarchy
Files
Design
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Transceiver Toolkit
External Memory Interface Toolkit
2
MegaWizard Plug-In Manager
Nios II Software Build Tools for Eclipse
Qsys
Tcl Scripts...
Customize...
Options...
License Setup...
Type ID Message
293000 Quartus II Full Compil
84 warnings
System (12)
Processing (611)
Starts Nios II Software Build Tools for Eclipse
100%
00:01:43

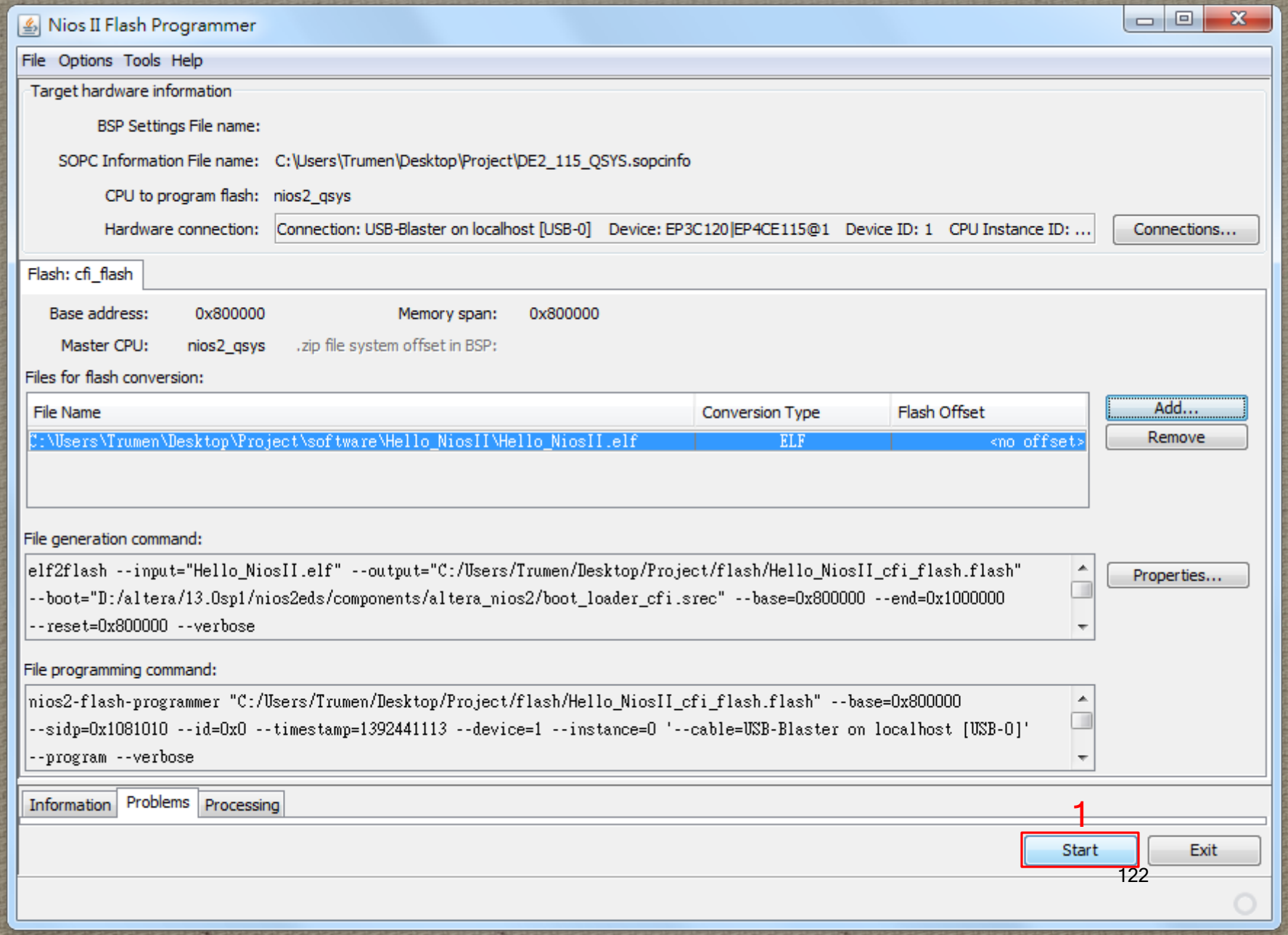

Nios II - Hello_NiosII/hello_world.c - Ecl
File Edit Source Refactor Navigate
Project Explorer
Hello_NiosII
Hello_NiosII_bsp [DE2_115_QSYS]
Hello_NiosII_bsp
Nios II Debug
Nios II
C/C++
1
(right-click)
Copy Ctrl+C
Paste Ctrl+V
Delete Delete
Remove from Context Ctrl+Alt+Shift+Down
Source
Move...
Rename... F2
Import...
Export...
Build Project
Clean Project
Refresh F5
Close Project
Close Unrelated Projects
Build Configurations
Make Targets
Index
Show in Remote Systems view
Convert To...
Run As
Debug As
Profile As
Team
Compare With
Restore from Local History...
Nios II
2
Run C/C++ Code Analysis
Properties Alt+Enter
3
Nios II Command Shell
Generate BSP
BSP Editor...
Path
Location

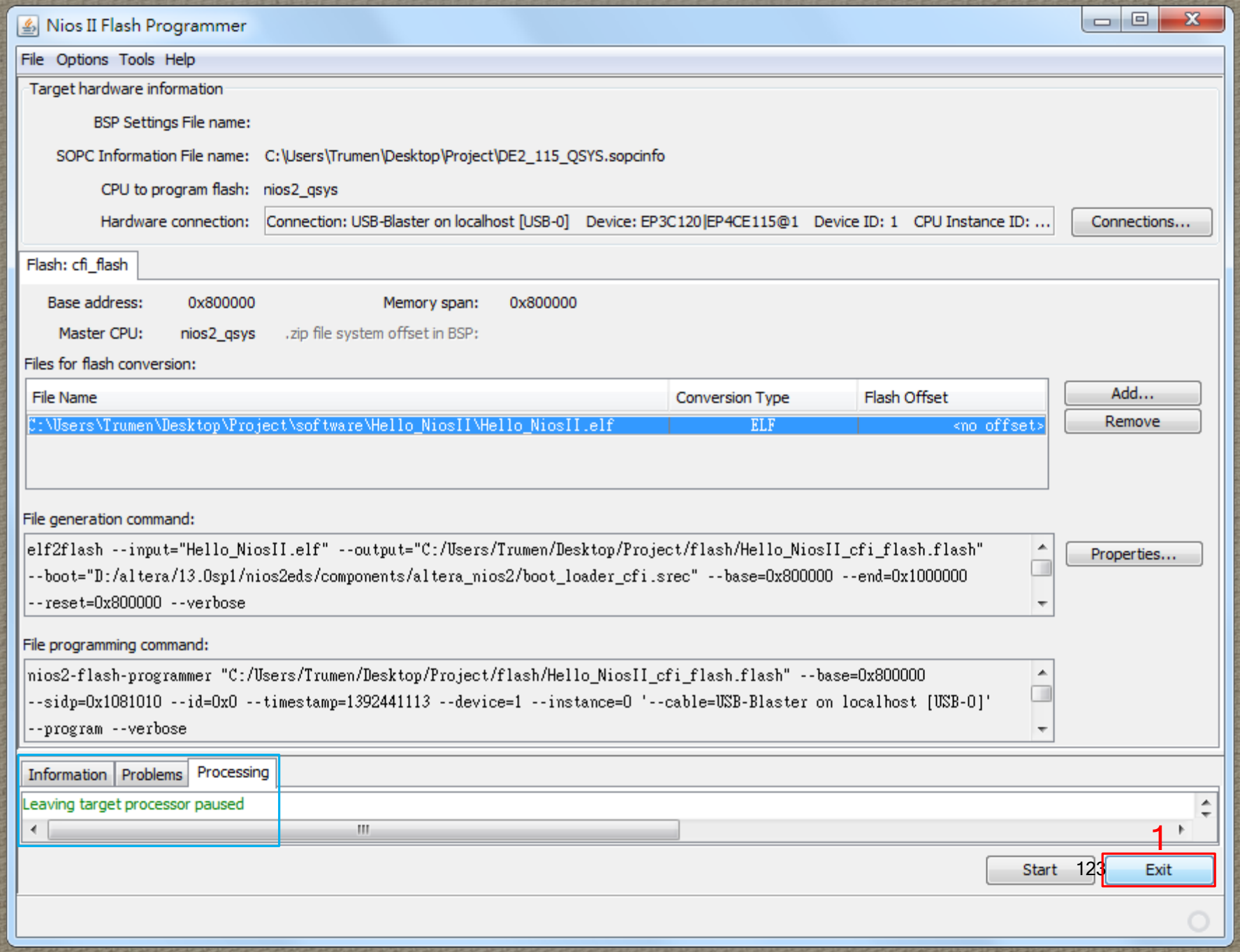

Nios II - Hello_Nic
File Edit Source
Project Explorer
Hello_NiosII
Hello_NiosII_
1
(right-click)
Go Into
Open in New Window
Copy Ctrl+C
Paste Ctrl+V
Delete Delete
Remove from Context Ctrl+Alt+Shift+Down
Source
Move...
Rename... F2
Import...
Export...
Build Project
2
Clean Project
Refresh F5
Close Project
Close Unrelated Projects
Build Configurations
Make Targets
Index
Show in Remote Systems view
Convert To...
Run As
Debug As
Profile As
Team
Compare With
Restore from Local History...
Nios II
Help
Nios II Debug
Nios II
C/C++
gs.h"
");
(LED_BASE, 1 << count);
Properties
Debug
umen\Desktop\Project\software\Hello_NiosII_bsp\link
umen\Desktop\Project\software\Hello_NiosII_bsp\link
umen\Desktop\Project\software\Hello_NiosII_bsp\memc
umen\Desktop\Project\software\Hello_NiosII_bsp\Make
es. Total time taken = 2 seconds
Users\Trumen\Desktop\Project\software\Hello_NiosII_


Nios II - Hello_Nic
File Edit Source
Project Explorer
Hello_NiosII
Hello_NiosII_
1
(right-click)
Copy Ctrl+C
Paste Ctrl+V
Delete Delete
Remove from Context Ctrl+Alt+Shift+Down
Source
Move...
Rename... F2
Import...
Export...
Build Project
Clean Project
Refresh F5
Close Project
Close Unrelated Projects
Build Configurations
Make Targets
Index
Show in Remote Systems view
Convert To...
Run As
Debug As
Profile As
Team
Compare With
Restore from Local History...
Nios II
2
Run C/C++ Code Analysis
Update Linked Resources
Properties Alt+Enter
BSP Editor...
Nios II Command Shell...
Flash Programmer...
3
Help
Nios II Debug
Nios II
C/C++
gs.h"
");
(LED_BASE, 1 << count);
Properties
Debug
s free for stack + heap.
-syms --all-header --source Hello_NiosII.elf
119


Nios II Flash Programmer
File
Options
Tools
Help
New...
1
2
New Flash Programmer Settings File
Get flash programmer system details from BSP Settings File
Get flash programmer system details from SOPC Information File
BSP Settings File name:
SOPC Information File name:
Master CPU name:
Flash memory:
OK
Cancel
3
...
Instance ID: ...
Connections...
Nios II
This too
It parse
Each Fl
Use the
or open an existing project using the File->Open menu item.
lash device found.
sh device.
Information
Prob
Start
Exit
Select SOPC Information Design File
Look in:
Project
.qsys_edit
db
DE2_115_QSYS
incremental_db
output_files
software
workspace
DE2_115_QSYS.sopcinfo
4
最近的項目
桌面
我的文件
File name:
DE2_115_QSYS.sopcinfo
Files of type:
SOPC Information File (.sopcinfo)
5
Select
Cancel


Nios II Flash Programmer
File Options
New Flash Programmer Settings File
Get flash programmer system details from BSP Settings File
Get flash programmer system details from SOPC Information File
BSP Settings File name:
SOPC Information File name:
C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.sopcinfo
Master CPU name:
nios2_qsys
Flash memory:
cfi_flash
1
OK
Cancel
2
Add...
Remove
Connections...
File Name
File generation command:
File programming command:
Properties...
Information
Problems
Processing
Start
Exit
Select File for Flash Conversion
Look in:
Hello_NiosII
obj
Hello_NiosII.elf
4
最近的項目
桌面
我的文件
File name:
Hello_NiosII.elf
Files of type:
Nios II ELF File
3
5
Select
Cancel


Nios II Flash Programmer
File Options Tools Help
Target hardware information
BSP Settings File name:
SOPC Information File name: C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.sopcinfo
CPU to program flash: nios2_qsys
Hardware connection: Connection: USB-Blaster on localhost [USB-0] Device: EP3C120|EP4CE115@1 Device ID: 1 CPU Instance ID: ...
Connections...
Flash: cfi_flash
Base address: 0x800000 Memory span: 0x800000
Master CPU: nios2_qsys .zip file system offset in BSP:
Files for flash conversion:
File Name
Conversion Type
Flash Offset
C:\Users\Trumen\Desktop\Project\software\Hello_NiosII\Hello_NiosII.elf
ELF
<no offset>
Add...
Remove
File generation command:
elf2flash --input="Hello_NiosII.elf" --output="C:/Users/Trumen/Desktop/Project/flash/Hello_NiosII_cfi_flash.flash"
--boot="D:/altera/13.0sp1/nios2eds/components/altera_nios2/boot_loader_cfi.srec" --base=0x800000 --end=0x1000000
--reset=0x800000 --verbose
Properties...
File programming command:
nios2-flash-programmer "C:/Users/Trumen/Desktop/Project/flash/Hello_NiosII_cfi_flash.flash" --base=0x800000
--sidp=0x1081010 --id=0x0 --timestamp=1392441113 --device=1 --instance=0 '--cable=USB-Blaster on localhost [USB-0]'
--program --verbose
Information
Problems
Processing
1
Start
Exit


Nios II Flash Programmer
File Options Tools Help
Target hardware information
BSP Settings File name:
SOPC Information File name: C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.sopcinfo
CPU to program flash: nios2_qsys
Hardware connection: Connection: USB-Blaster on localhost [USB-0] Device: EP3C120|EP4CE115@1 Device ID: 1 CPU Instance ID: ...
Connections...
Flash: cfi_flash
Base address: 0x800000 Memory span: 0x800000
Master CPU: nios2_qsys .zip file system offset in BSP:
Files for flash conversion:
File Name
Conversion Type
Flash Offset
C:\Users\Trumen\Desktop\Project\software\Hello_NiosII\Hello_NiosII.elf
ELF
<no offset>
Add...
Remove
File generation command:
elf2flash --input="Hello_NiosII.elf" --output="C:/Users/Trumen/Desktop/Project/flash/Hello_NiosII_cfi_flash.flash"
--boot="D:/altera/13.0sp1/nios2eds/components/altera_nios2/boot_loader_cfi.srec" --base=0x800000 --end=0x1000000
--reset=0x800000 --verbose
Properties...
File programming command:
nios2-flash-programmer "C:/Users/Trumen/Desktop/Project/flash/Hello_NiosII_cfi_flash.flash" --base=0x800000
--sidp=0x1081010 --id=0x0 --timestamp=1392441113 --device=1 --instance=0 '--cable=USB-Blaster on localhost [USB-0]'
--program --verbose
Information
Problems
Processing
Leaving target processor paused
Start
123
Exit
1

Finally...

- Restart power on the development board.
- Download NiosII.sof of your project “NiosII” to the board.
- You will see that the LEDs blink!

The End.

Any question?

Reference

1. "My First Nios II for Altera DE2-115 Board" by Terasic Technologies Inc.
2. "My First Nios II for Altera DE2i-150 Board" by Terasic Technologies Inc.
3. "DE2-115 User Manual" by Terasic Technologies Inc.