My First Nios II for Altera DE2-115 Board

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Digital Circuit Lab

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Outline

- Hardware Design
- Nios II IDE Build Flow
- Programming the CFI Flash

Hardware Design



Introduction

 This slides provides comprehensive information that will help you understand how to create a FPGA based SOPC system implementing on your FPGA development board and run software upon it.



Required Features (1/2)

- The Nios II processor core is a soft-core central processing unit (CPU) that you could program onto an Altera field programmable gate array (FPGA).
- This chapter illustrates you to the basic flow covering hardware creation and software building.



Required Features (2/2)

- The example NIOS II standard hardware system provides the following necessary components:
 - Nios II processor core, that's where the software will be executed.
 - On-chip memory to store and run the software.
 - JTAG link for communication between the host computer and target.
 - Hardware (typically using a USB-Blaster cable).
 - LED peripheral I/O (PIO), be used as indicators.



Creation of Hardware Design



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Directory, Name, Top-Level Entity [page 1 of 5]

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🚳 New Project Wizard

Add Files [page 2 of 5]

Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project. Note: you can always add design files to the project later.

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🍓 New Project Wizard

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation. You can install additional device support with the Install Devices command on the Tools menu.

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Companion device

HardCopy:

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```
module NiosII (
    clk,
    rst_n,
    led,
);
input clk, rst_n;
output [7:0] led;
DE2_115_QSYS DE2_115_QSYS_inst (
    .clk_clk(clk),
    .reset_reset_n(rst_n),
    .led_export(led),
);
endmodule
```





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NIOS II IDE Build Flow

This Chapter covers build flow of Nios II C coded software program.



Introduction

- The Nios II IDE build flow is an easy-to-use graphical user interface (GUI) that automates build and makefile management.
- In this section you will use the Nios II IDE to compile a simple C language example software program to run on the Nios II standard system configured onto the FPGA on your development board.





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Application project Project name: Hello_NiosII Use default location Project location: C:\Users\Trumen\Desktop\Project\software\Hello_NiosII Project template	
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Project Description

- When you create a new project, the NIOS II SBT for Eclipse creates two new projects in the NIOS II C/C++ Projects tab:
 - Hello_NiosII is your C/C++ application project. This project contains the source and header files for your application.
 - Hello_NiosII_bsp is a board support package that encapsulates the details of the Nios II system hardware.













Edit and Re-Run the Program

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<pre>#include <stdio.h> #include <stdio.h> #include "system.h" #include "system.h" #include "altera_avalon_pio_regs.h" #includes obj int main() { printf("Hello from Nios II!\n"); int count = 0; int delay; while(1) { reate-this-app Hello_NiosILobjdump Hello_NiosILobjdump Makefile readme.txt #includes count = (count+1) % 8; // Gelay < 2000000) { return 0; // ellay = 115_QSYS // ellay = 0; // ellay = 0; // ellay < 2000000) {</stdio.h></stdio.h></pre>

```
#include <stdio.h>
#include "system.h"
#include "altera_avalon_pio_regs.h"
int main()
  printf("Hello from Nios II!\n");
  int count = 0;
  int delay;
  while(1) {
    IOWR_ALTERA_AVALON_PIO_DATA(LED_BASE, 1 << count);</pre>
    delay = 0;
    while(delay < 2000000 ) {</pre>
      delay++;
    }
    count = (count+1) \% 8;
  return ∅;
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Why the LEDs Blink? (1/2)

- The Nios II system description header file, system.h, contains the software definitions, name, locations, base addresses, and settings for all of the components in the Nios II hardware system.
- The system.h file is located in the in the Hello_NiosII_bsp directory.





Why the LED Blinks? (2/2)

- The Nios II processor controls the PIO ports (and thereby the LED) by reading and writing to the register map.
- For the PIO, there are four registers: data, direction, interrupt mask, and edge capture.
- To turn the LED on and off, the application writes to the PIO data register.



Register Map File (1/2)

- The PIO core has an associated software file altera_avalon_pio_regs.h.
 - This file defines the core's register map, providing symbolic constants to access the low-level hardware.
 - This file is located in Project\software\Hello_NiosII_bsp\drivers\inc \.



Register Map File (2/2)

- When you include this file, several useful functions that manipulate the PIO core registers are available to your program.
- In particular, the function IOWR_ALTERA_AVALON_PIO_DATA (base, data) can write to the PIO data register, turning the LED on and off.
- The PIO is just one of many SOPC peripherals that you can use in a system.



Debugging the Application

 Before you can debug a project in the NIOS II SBT for Eclipse, you need to create a debug configuration that specifies how to run the software.




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Debugging Tips

 When debugging a project in the Nios II SBT for Eclipse, you can pause, stop or single step the program, set breakpoints, examine variables, and perform many other common debugging tasks.





Configure BSP Editor

- In this section you will learn how to configure some advanced options about the target memory or other things.
- By performing the following steps, you can charge all the available settings.



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Note

- If you make changes to the system properties or the Qsys properties or your hardware, you must rebuild your project
- To rebuild, right-click the Hello_NiosII_BSP->Nios II->Generate BSP and then Rebuild Hello_NiosII Project.



Programming the CFI Flash

Introduction

- With the density of FPGAs increasing, the need for larger configuration storage is also increasing.
- If your system contains a common flash interface (CFI) flash memory, you can use your system for FPGA configuration storage as well.





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🚣 Generic Tri-State Controller - generic_tristate_controller_0



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🚣 Generic Tri-State Controller - generic_tristate_controller_0



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🚣 Generic Tri-State Controller - generic_tristate_controller_0

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👃 Generic Tri-State Controller - generic_tristate_controller_0

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Component Library	Project \$	La Tri-State Conduit Bridge - tristate_conduit_bridge_0	X
Image: Control of the second secon	Use Use Use V V V V	Tri-State Conduit Bridge altera_tristate_conduit_bridge Block Diagram Show signals tristate_conduit_bridge_0 clk clk clk clk clk	Documentation
(double-click) ● Generic Tri-State Controller ● Tri-State Conduit Bridge ● Tri-State Conduit Pin Sharer ● Tri-State Conduit Pin Sharer ● Tri-State Conduit Pin Sharer ● Bridge ● Mew Edit		uas tcm tristate_bridge_flash_pin_sha clk reset tcm tcs0 III	Cancel Finish Avalon Memory Mapped Slave Image: Conduit Master Tristate Conduit Master Image: Conduit Pin Sharer Clock Input Image: Conduit Master Tristate Conduit Master Image: Conduit Master Tristate Conduit Master Image: Conduit Master Tristate Conduit Slave Image: Conduit Slave
Messages			
Description		Path	8
E 🔀 4 Errors			<u>^</u>
Cfi_flash.clk must be connected t	o a clock output	System.cfi_flash	98
4 Errors, 3 Warnings		Svotom triototo brid	lao flooh sin ohoro

👃 Qsys - DE2_115_QSYS.qsys* (C:\U	lsers\T	rume	n\Desktop\Pro	ject\DE2_115_(QSYS.qsys)					X
File Edit System View Tools Help										
Component Library	Project Settings Instance Parameters			System Inspe	System Inspector		Gene	ration		
·			System Cont	tents		Address Map		Clock	Settings	
S X									-	
Ided Processors	*	Use	Connections		Name			Description		E:
ice Protocols	×		↓ ↓ ↓	>	reset			Reset Input		
ries and Memory Controllers			♦ ↔	>	control_s	lave		Avalon Memory Mapp	ed Slave	
Components	· _	V			🖃 led			PIO (Parallel I/O)		
controller Peripherals			♦	>	clk			Clock Input		
erals			🔶 📘 🔶 🔶	>	reset			Reset Input		
			🔶 🔶	>	s1			Avalon Memory Mapp	ed Slave	
Interconnect					external_	connection		Conduit		le
нв		V			cfi_flash			Generic Tri-State Cont	troller	
KI Interface	8		\	\longrightarrow	clk			Clock Input		
errupt	-			\longrightarrow	reset			Reset Input		
emory-Mapped		uas uas					Avalon Memory Mapp	ed Slave		
i-State Components		tcm					Tristate Conduit Maste	r		
····· Conduit Pin Divider		✓ ☐ tristate_bridge_flash_pin_s			share	Tri-State Conduit Pin S	harer			
Generic Tri-State Controller					clk			Clock Input		
····· Tri-State Conduit Bridge					reset		Reset Input			
Tri-State Conduit Bridge Tra					tcm			Tristate Conduit Maste	F	=
In-State Conduit Pin Sharer				$\phi \rightarrow \phi \rightarrow \phi$	tcsu	and the balance of		Tristate Conduit Slave		
cation		V			tristate_c	conduit_bridge_v	71	Tri-State Conduit Bride	ie .	
w Bridge					CIK			Connections	•	
4 m					teset		0	F iller		
					out		Y	Filler	•	-
New Edit		•			our			Edit	Ctrl+E	•
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Description						Path	×	Remove		<u> </u>
Errors						Details	+	-		
Cfi_flash.clk must be connected t	to a clo	ck outp	ut			System.cfi_flash		Show Arbitration Share	99	
6 Errors, 5 Warnings						Suntam trintata brid	c		-	-
							A .	Lock Base Address		

👃 Qsys - DE2_115_QSYS.qsys* (C:\U	lsers\Ti	rumer	n\Desktop\F	Project\DE2_115	_QSYS.qsys)				x
File Edit System View Tools Help									
Component Library	Project Settings Instance Parameters		arameters	System Inspector	HDL Example	Generation	n		
			System C	ontents		Address Map	Clock Se	ettings	
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ice Protocols	×		+ + +	+	→ reset		Reset Input		
ries and Memory Controllers			🔶 🕂		control_s	slave	Avalon Memory Mapped	Slave	
Components	·	1			🗆 led		PIO (Parallel I/O)		
controller Peripherals			♦		≻ <mark>clk</mark>		Clock Input		
erals			+	+	reset		Reset Input		
	-		🔶 🕂		≻ s1		Avalon Memory Mapped	Slave	
Interconnect	-			1	external	_connection	Conduit	le	31
НВ	. –	V		+•	🗆 cfi_flash		Generic Tri-State Control	ler	
KI Interface	8		♦	+	≻ clk		Clock Input		
errupt	"		+	+	> reset		Reset Input		
emory-Mapped			🔶 🔶	+	uas		Avalon Memory Mapped	Slave	
i-State Components					< tcm		Tristate Conduit Master		
Conduit Pin Divider		\checkmark			tristate_l	bridge_flash_pin_share	Tri-State Conduit Pin Sha	rer	
···· Generic Tri-State Controller			•		→ clk	2	Clock Input		
Tri-State Conduit Bridge			♦	♦	reset	(double-click)	Reset Input		
···· Tri-State Conduit Bridge Tra					< tcm		Tristate Conduit Master		
···· Tri-State Conduit Pin Sharer				++	tcs0		Tristate Conduit Slave		=
cation		V			🗆 tristate_l	bridge_flash	Tri-State Conduit Bridge		
w Bridge 👻 👻			♦ -		→ clk		Clock Input		
4 III >			∣ ∔	↓ ↓ ↓	reset		Reset Input		
				↓_	→ tcs		Tristate Conduit Slave		
					out		Conduit		Ŧ
New		•							
Марралар	,								_
messayes						1			
Description						Path			
🗆 🔀 2 Errors									-
Sonchip_memory2.s1 (0x40000.	.0x7ffff) overla	aps cfi_flash	uas (0x00x7ffff	;)	System.nios2_qsys.data_	_master 10	00	
					n	Svotom pipo?	untion montor		

👃 Tri-State Conduit Pin Sharer - tristate_bridge_flash_pin_share

1	Tri-State Con	nduit Pin Sharer						
MegaCore'	altera_tristate_conduit	t_pin_sharer					Docume	ntation
- Block I	Diagram	Parameters						
Chow		Number of Interfaces: 1						
Show	signais							
	triototo bridgo floch	Sharing Assignment						
	instate_bridge_ilash	To share a signal, type the sa	me signal name in the S	hared Signal Name c	column for all control	ers that share that signa		
clk	alaali tiir							
reset	CIOCK UIS	Update Interface Table	1				_	
10001	reset	Interface	Signal Role	Signal Type	Signal Width	Shared Signal Name		
tcsu	tristate_conduit	cfi flash.tcm	address	Output	23	fs addr		
	altera_trist	cfi flash.tcm	outputenable n	Output	1	fl read n	2	
L		cfi_flash.tcm	write_n	Output	1	fl_we_n	14	
		cfi_flash.tcm	data	Bidirectional	8	fs_data		
		cfi_flash.tcm	chipselect_n	Output	1	fl_cs_n		
•	4 [1]	+ -		III				•
								2
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Qsys - DE2_115_QSYS.qsys* (C:\User	rs\Trumen\Desktop\P	roject\DE2_115_QSY	'S.qsys)			
File Edit System View Tools Help						
Component Library	Project Settings	Instance Parame	ters System Inspecto	or HDL Example	Generation	
	System Co	intents	Address Map	Clock Set	ttings	
	-		•		-	
Ided Processors	t ons	Name	Description	Export	Clock	
ice Protocols	╳╷╷╺┝╴╴╴╴╴	> reset	Reset Input	Double-click to export	[clk]	
ries and Memory Controllers	ਡ 🔶 🕂 🛁	control slave	Avalon Memory Mapp	Double-click to export	[clk]	
Components		⊡ led	PIO (Parallel VO)			
controller Peripherals	록	→ clk	Clock Input	Double-click to export	clk_50	
erals	▲	→ reset	Reset Input	Double-click to export	[clk]	
	↓ ↓	→ s1	Avalon Memory Mapp	Double-click to export	[clk]	
Interconnect		external_connect	ction Conduit	led		
нв	×	cfi_flash	Generic Tri-State Cont.			
KI Interface		→ clk	Clock Input	Double-click to export	clk_50	
errupt	" 	> reset	Reset Input	Double-click to export	[clk]	
emory-Mapped	↓	→ uas	Avalon Memory Mapp	Double-click to export	[clk]	
i-State Components		< tcm	Tristate Conduit Master	Double-click to export	[clk]	
Conduit Pin Divider		tristate_bridge_	flash Tri-State Conduit Pin S.			
@ Generic Tri-State Controller		→ clk	Clock Input	Double-click to export	clk_50	
Tri-State Conduit Bridge	• + · · · · ·	→ reset	Reset Input	Double-click to export	[clk]	
···· Tri-State Conduit Bridge Tra		< tcm	Tristate Conduit Master	Double-click to export	[clk]	
···· Tri-State Conduit Pin Sharer		> tcs0	Tristate Conduit Slave	Double-click to export	[clk]	
cation		tristate_bridge_	flash Tri-State Conduit Bridge	e		
w Bridge 👻		→ clk	Clock Input	Double-click to export	clk_50	
< III ►	• + ;	→ reset	Reset Input	Double-click to export	[clk]	
	· -	→ tcs	Tristate Conduit Slave	Double-click to export	[clk]	
New Edit 🕂 Add		out	Conduit	tristate_bridge_flash_out	1	
					۱.	
,						
messages						
Description			Path			
🗆 🔀 2 Errors						
Sonchip_memory2.s1 (0x400000x)	7ffff) overlaps cfi_flash.u	uas (0x00x7fffff)	System.nios2_qsys.da	ata_master 102	2	
2 Errore 1 Warning		(0 0 0 7 ////0	Suntam nina? anua in	otruction montor		

& Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)

File Edit System View Tools Help

Component Library		Project	Settings	Instance Pa	rameters	System In	System Inspector HDL Exam		xample	Generatio	n
			System Co	ontents		Address Map)		Clock Settings		
ded Processors	÷	Use	Connections		Name		Description		Export		
ce Protocols	×	V			□ clk_50		Clock Source				
ries and Memory Controllers					clk_in		Clock Input		clk		
Components	·			$\diamond \longrightarrow$	clk_in_re	eset	Reset Input		reset		
controller Peripherals					clk	1	Clock Output		Doubl	e-click to exp	0
erals					clk_rese	t (double-click)	Reset Output		Doubl	e-click to exp	0
	-	V			🗉 nios2_qs	sys	Nios II Proces	sor			Ξ
Interconnect			🛉 📘 👘	<u> </u>	clk		Clock Input		Doubl	e-click to exp	0
HB			•	∮ →	reset_n		Reset Input		Doubl	e-click to exp	0
XI Interface	8				data_ma	ster	Avalon Memo	ry Mapp	Doubl	e-click to exp	0
terrupt					instruction	on_master	Avalon Memo	гу Марр	Doubl	e-click to exp	0
emory-mapped					jtag_deb	ug_module_reset	Reset Output	n Mann	Doubl	e-click to exp	0
Conduit Din Divider					jiag_deb	instruction man	Avaion Menio	ry mapp	Doubl	e-click to exp	0
Generic Tri-State Controller					E itag uart	instruction_mas	ITAG HART	iction ma	Doubl	е-спск то ехр	°
			∣┫┥┥┥┥	<u> </u>	clk		Clock Input		Doubl	a aliak ta ava	
Tri-State Conduit Bridge Tra			•	↓ · · · ·	reset		Reset Input		Doubl	e-click to exp	
····· Tri-State Conduit Pin Sharer			🔶 🕂	\rightarrow	avalon i	tao slave	Avalon Memo	гу Марр	Doubl	e-click to exp	
cation		V			onchip n	nemory2	On-Chip Mem	ory (RA	DOUDT	c onon co cap	×
w Bridge 👻 👻			♦	$\downarrow \longrightarrow$	clk1		Clock Input	• •	Doubl	e-click to exp	0
۰ III ا			+ +	\rightarrow	s1		Avalon Memo	гу Марр	Doubl	e-click to exp	0
			+	$\bullet \longrightarrow$	reset1		Reset Input		Doubl	e-click to exp	0
New Edit Add		V			🗆 sysid_qs	sys	System ID Per	ripheral			Ŧ
)	,
Messages											
Description						Path					
🗆 🔀 2 Errors											-
Sonchip_memory2.s1 (0x40000	0x7fff	f) overla	aps cfi_flash.u	uas (0x00x7fffff)		System.nios2_q	sys.data_mas	ter	1()3	
2 Errors, 1 Warning		<u> </u>	<i></i>			Svotom pipo?	ovo inotruction	montor			-

🚣 Nios II Processor - nios2_qsys

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megator	9

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Nios II Processor

gaCore altera_nios2_qs	sys		Documentat
Block Diagram	Hardware multiplication type:	Embedded Multipliers 👻	
Show signals	Hardware divide		
	TReset Vector		
	Reset vector memory:	cfi_flash.uas	
clk	Reset vector offset:	0x00000000 1	
reset_n	Reset vector:	0×0000000	
d_irq			
itag_debug_module	Exception Vector		
	Exception vector memory:	onchip_memory2.s1	
	Exception vector offset:	0x0000020	
	Exception vector:	0x00040020	
	MMII and MDII		
	Only include the MMU using an operating	g system that explicitly supports an MMU.	
4	<		

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Documentation

Finish

Cancel

👃 Qsys	Qsys - DE2_115_QSYS.qsys* (C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.qsys)								
File Edit	Syste	m View Tools Help							
Compon		Upgrade IP Cores		Instance	Parameters	System In	spector	HDL Example	e Generation
				em Contents		Address Map		Clo	ock Settings
<u> </u>		Assign base Addresses Z]					
Ided Pro		Assign Interrupt Numbers		ctions	Name	Name		Expo	rt
Ice Prot		Assign Custom Instruction Opcodes	÷		□ clk_50		Clock Source		•
ries and		Create Global Reset Network			clk_in		Clock Input	clk	
Compo				Υ <u></u>	→ clk_in_re	set	Reset Input	reset	t 👘
controlle		Show System With Qsys Fabric Cor	mponents		≺ clk		Clock Output	D	ouble-click to expo
erals		Run SOBC Builder to Onve Ungrade			≺ clk_reset		Reset Output	D	ouble-click to expo
		Run SOPC Builder to usys opgrade			□ nios2_qs	ys	Nios II Process	or	E
Intercor		Remove Depairs Connections			→ clk		Clock Input	D	ouble-click to expo
HB		Remove Dangling Connections		├ ── † ────	reset_n		Reset Input	D	ouble-click to expo
KI Interfa	ice				≺ data_mas	ster	Avalon Memory	у Марр 🛛 🛛	ouble-click to expo
terrupt				1 d	✓ instructio	n_master	Avalon Memory	у Марр 🛛 🛛	ouble-click to expo
emory-N	appe	d			≺ jtag_debι	.ig_module_reset	Reset Output	D	ouble-click to expo
i-State (Compo	nents		+ +	→ jtag_debι	.g_module	Avalon Memory	у Марр 🛛 🛛	ouble-click to expo
© C	onduit	Pin Divider		×	≺ custom_i	nstruction_mas	Custom Instruc	ction Ma D	ouble-click to expo
@ G	enerio	Tri-State Controller	V		🖃 jtag_uart		JTAG UART		
···· @ 👖	i-Stat	e Conduit Bridge	♦		→ clk		Clock Input	D	ouble-click to expo
© Ti	i-Stat	e Conduit Bridge Tra	- ♦-	┤│ ♦ ────	→ reset	reset		D	ouble-click to expo
© Ti	i-Stat	e Conduit Pin Sharer		• • · · · · · · · · · · · · · · · · · ·	→ avalon_jt	ag_slave	Avalon Memory	у Марр 🛛 🖉	ouble-click to expo
cation			V		🗆 🖸 onchip_m	emory2	On-Chip Memo	ry (RA	
w Bridg	e	-	♦		→ clk1		Clock Input	D	ouble-click to expo
•				+ +	→ s1		Avalon Memory	у Марр 🛛 🛛	ouble-click to expo
			♦-		→ reset1		Reset Input	D	ouble-click to expo
New		dit dbA db	V		🗆 sysid_qs	ys	System ID Peri	pheral	T
				1	1				F.
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Message	s								
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(3) o	nchip	_memory2.s1 (0x400000x7ffff) o	verlaps cfi_	_flash.uas (0x00x7fff	ff)	System.nios2_q	sys.data_maste	er	105
0		0 1 /0 10000 0 T///D				Suntam nina? a	ave instruction	mantar	
2 Errors,	1 Wa	rning							

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👃 Qsys - DE2_115_QSYS.qsys* (C:\U	sers\Trumen\Desktop\P	roject\DE2_115_QSV	/S.qsys)			
File Edit System View Tools Help						
Component Library	System Co	ontents		Address Map	Clock Settings	
	Project Settings	Instance Parame	eters	System Inspector	HDL Example	Generation
dded Processors ice Protocols ries and Memory Controllers Components controller Peripherals erals Interconnect HB KI Interface terrupt	The testbench system Once generated, the Create testbench Q Create testbench si Synthesis Synthesis files are Create HDL design files	is a new Qsys system ave changes? Save chang 3 Save s for synthesis: Verilog	that instanti	ates the original system, adding	g bus functional models	to drive the top
emory-Mapped i-State Components 	Create block symbols Output Directory Path: Simulation: Testbench: Synthesis: Generate 2	 Info: Reusing file C: Info: Reusing file C: Info: Reusing file C: Info: irq_mapper: Info: tdt: "cfi_flash Info: tda: "cfi_flash Info: pin_sharer: " Info: arbiter: "trist Info: DE2_115_QSY Info: ip-generate su 	ted /Users/Tru /Users/Tru "DE2_115_(" instantiate " instantiate tristate_bri ate_bridge 'S: Done DE cceeded.	Imen/Desktop/Project/DE2_ Imen/Desktop/Project/DE2_ QSYS" instantiated altera_irq_ ed altera_tristate_controller ed altera_tristate_controller ridge_flash_pin_share" insta e_flash_pin_share" instantiat 2_115_QSYS" with 35 modules	115_QSYS/synthesis 115_QSYS/synthesis mapper "irq_mappe _translator "tdt" r_aggregator "tda" antiated altera_tristate ed altera_merlin_std s, 97 files, 3113638 byt	/submodi /submodi r" e_conduit I_arbitratc es
Messages		Info: Finished: Creater of the second sec	ate HDL de	sign files for synthesis		-
Description A Warning Properties (isFlash,isMemoryDevice O Errors, 1 Warning	e,isNonVolatileStorage) h	▲ Generate Completed	1. 0 Errors, (62 Warnings	Stop 10	4 Close



	module NiosII (
	clk,	
	rst_n,	
	led,	
	// flash	S- B-
	FL_ADDR,	ALC: N
	FL_CE_N,	
	FL_DQ,	
	FL_OE_N,	
	FL_RESET_N,	
	FL_RY,	
	FL_WE_N,	
	FL_WP_N	
);	
	<pre>input clk, rst_n;</pre>	
	<pre>output [7:0] led;</pre>	Control of
	// flash	No.
	<pre>output [22:0] FL_ADDR;</pre>	1110
	output FL_CE_N;	- ANA
	<pre>inout [7:0] FL_DQ;</pre>	The second
	output FL_OE_N;	
	<pre>output FL_RESET_N;</pre>	CHICA D
	<pre>input FL_RY;</pre>	
	output FL_WE_N;	
1000	output FL_WP_N;	City of
	DE2_115_QSYS_DE2_115_QSYS_inst (ALL A
	.clk_clk(clk),	日日
	.reset_reset_n(rst_n),	ALC: N
	.led_export(led),	A.M.
	// flash	
	.tristate_bridge_flash_out_fs_addr(FL_ADDR),	
	.tristate_bridge_flash_out_fl_read_n(FL_OE_N),	Tar Ba
	.tristate bridge flash out fl cs n(FL CE N),	
	.tristate bridge flash out fs data(FL DQ),	CHUR I
	.tristate_bridge_flash_out_fl_we_n(FL_WE_N),	
);	1111
	// flash config	144
	assign FL RESET N = $1'b1;$	
	assign FL WP N = $1'b1$;	 ALC: NO
并并 并不 于于不不	endmodule	H-H
distin		Si a




NodeName	Direction	Location
FL_ADDR[0]	Output	PIN_AG12
Put FL_ADDR[1]	Output	PIN_AH7
Strain FL_ADDR[2]	Output	PIN_Y13
Put FL_ADDR[3]	Output	PIN_Y14
Put FL_ADDR[4]	Output	PIN_Y12
Put FL_ADDR[5]	Output	PIN_AA13
Put FL_ADDR[6]	Output	PIN_AA12
Put FL_ADDR[7]	Output	PIN_AB13
Put FL_ADDR[8]	Output	PIN_AB12
Put FL_ADDR[9]	Output	PIN_AB10
Put FL_ADDR[10]	Output	PIN_AE9
Put FL_ADDR[11]	Output	PIN_AF9
Price FL_ADDR[12]	Output	PIN_AA10
Put FL_ADDR[13]	Output	PIN_AD8
Put FL_ADDR[14]	Output	PIN_AC8
STL_ADDR[15]	Output	PIN_Y10
Put FL_ADDR[16]	Output	PIN_AA8
Put FL_ADDR[17]	Output	PIN_AH12
Strain FL_ADDR[18]	Output	PIN_AC12
Put FL_ADDR[19]	Output	PIN_AD12
Put FL_ADDR[20]	Output	PIN_AE10
Strain FL_ADDR[21]	Output	PIN_AD10
Set FL_ADDR[22]	Output	PIN_AD11
Set FL_CE_N	Output	PIN_AG7
FL_DQ[0]	Bidir	PIN_AH8

Node Name	Direction	Location
PUT FL_CE_N	Output	PIN_AG7
FL_DQ[0]	Bidir	PIN_AH8
FL_DQ[1]	Bidir	PIN_AF10
FL_DQ[2]	Bidir	PIN_AG10
🖳 FL_DQ[3]	Bidir	PIN_AH10
FL_DQ[4]	Bidir	PIN_AF11
FL_DQ[5]	Bidir	PIN_AG11
FL_DQ[6]	Bidir	PIN_AH11
FL_DQ[7]	Bidir	PIN_AF12
PUS FL_OE_N	Output	PIN_AG8
STATEST N	Output	PIN_AE11
EL_RY	Input	PIN_Y1
STL_WE_N	Output	PIN_AC10
ST FL_WP_N	Output	PIN_AE12
in_ clk	Input	PIN_Y2
º ^{ut} led[0]	Output	PIN_E21
º ^{ut} led[1]	Output	PIN_E22
º ^{ut} led[2]	Output	PIN_E25
º ^{ut} led[3]	Output	PIN_E24
º ^{ut} led[4]	Output	PIN_H21
º ^{ut} led[5]	Output	PIN_G20
eut led[6]	Output	PIN_G22
eut led[7]	Output	PIN_G21
in_ rst_n	Input	PIN M23
< <new node="">></new>		





Edit View Proc	essing Tools Window	Help 💎			Search altera	.com 🔇
Hardware Setup	USB-Blaster [USB-0]	Mode: JTA	3	 Progr 	ess:	
Enable real-time ISP t	o allow background program	mming (for MAX II and	d MAX V devices)			
🎾 Start	File	Device	Checksum	Usercode	Program/ Configure	Verify Blank- Check
Ju Stop	output_files/NiosII.sof	EP4CE115F29	008BF0FD	008BF0FD		
Auto Detect						
Add File						
Change File	•					۴.
Save File						<u>^</u>
Add Device						
1 ¹⁰ Up						
J [™] Down						=
	EP4CE115F	29				
	↓ TDO					
						-

🔔 Hardware Setup	USB-Blaster [USB-0]	Mode: JTAC	3	▼ Progr	ess: 100%	% (Success	ful)
Enable real-time I	SP to allow background progra	amming (for MAX II and	d MAX V devices)				
Start	File	Device	Checksum	Usercode	Program/ Configure	Verify	Blank- Check
Stop	output_files/NiosII.sof	EP4CE115F29	008BF0FD	008BF0FD			
Auto Detect							
🔀 Delete							
Add File							
쌸 Change File							
Save File							
Add Device							
Dp							
Down							=
	EP4CE115	iF29					



Nios II - Hello Nios II/bello world c - Ec						
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🔬 Nios II Flash Programmer	
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Target hardware information	
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SOPC Information File name: C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.sopcinfo	
CPU to program flash: nios2_gsys	
Hardware connection: Connection: USB-Blaster on localhost [USB-0] Device: EP3C120 [EP4CE115@1 Device ID: 1 CPU Instance ID:	Connections
Flash: cfi_flash	
Base address: 0x800000 Memory span: 0x800000	
Master CPU: nios2_qsys .zip file system offset in BSP:	
Files for flash conversion:	
File Name Conversion Type Flash Offset	Add
<pre>C:\Users\Trumen\Desktop\Project\software\Hello_NiosII\Hello_NiosII.elf ELF <no offset=""></no></pre>	Remove
File generation command:	
elf2flashinput="Hello_NiosII.elf"output="C:/Users/Trumen/Desktop/Project/flash/Hello_NiosII_cfi_flash.flash"	Properties
boot="D:/altera/13.0sp1/nios2eds/components/altera_nios2/boot_loader_cfi.srec"base=0x800000end=0x1000000	
reset=UX8UUUUUverbose	
File programming command:	
nios2-flash-programmer "C:/Users/Trumen/Desktop/Project/flash/Hello_NiosII_cfi_flash.flash"base=Ox800000	
sidp=Ox1081010id=OxOtimestamp=1392441113device=1instance=O 'cable=USB-Blaster on localhost [USB-O]'	
programveroose	
Information Problems Processing	
Start	Exit
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File Options Tools Help								
Target hardware information]							
BSP Settings File name:								
SOPC Information File name: C:\Users\Trumen\Desktop\Project\DE2_115_QSYS.sopcinfo								
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Flash: cfi_flash								
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Files for flash conversion:								
File Name Conversion Type Flash Offset	Add							
C:\Users\Trumen\Desktop\Project\software\Hello_NiosII\Hello_NiosII.elf ELF <no offset=""></no>	Remove							
File generation command:								
elf2flashinput="Hello_NiosIl.elf"output="C:/Users/Irumen/Desktop/Project/flash/Hello_NiosIl_cfl_flash.flash"	Properties							
reset=0x800000verbose								
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nios2-flash-programmer "C:/Users/Trumen/Desktop/Project/flash/Hello NiosII cfi flash.flash"base=0x800000								
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Information Problems Processing								
Leaving target processor paused	÷							
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Start 1.	2 Exit							
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Finally...

- Restart power on the development board.
- Download NiosII.sof of your project "NiosII" to the board.
- You will see that the LEDs blink!





Reference

- 1. "My First Nios II for Altera DE2-115 Board" by Terasic Technologies Inc.
- 2. "My First Nios II for Altera DE2i-150 Board" by Terasic Technologies Inc.
- 3. "DE2-115 User Manual" by Terasic Technologies Inc.

