Introduction to VGA

Digital Circuit Lab

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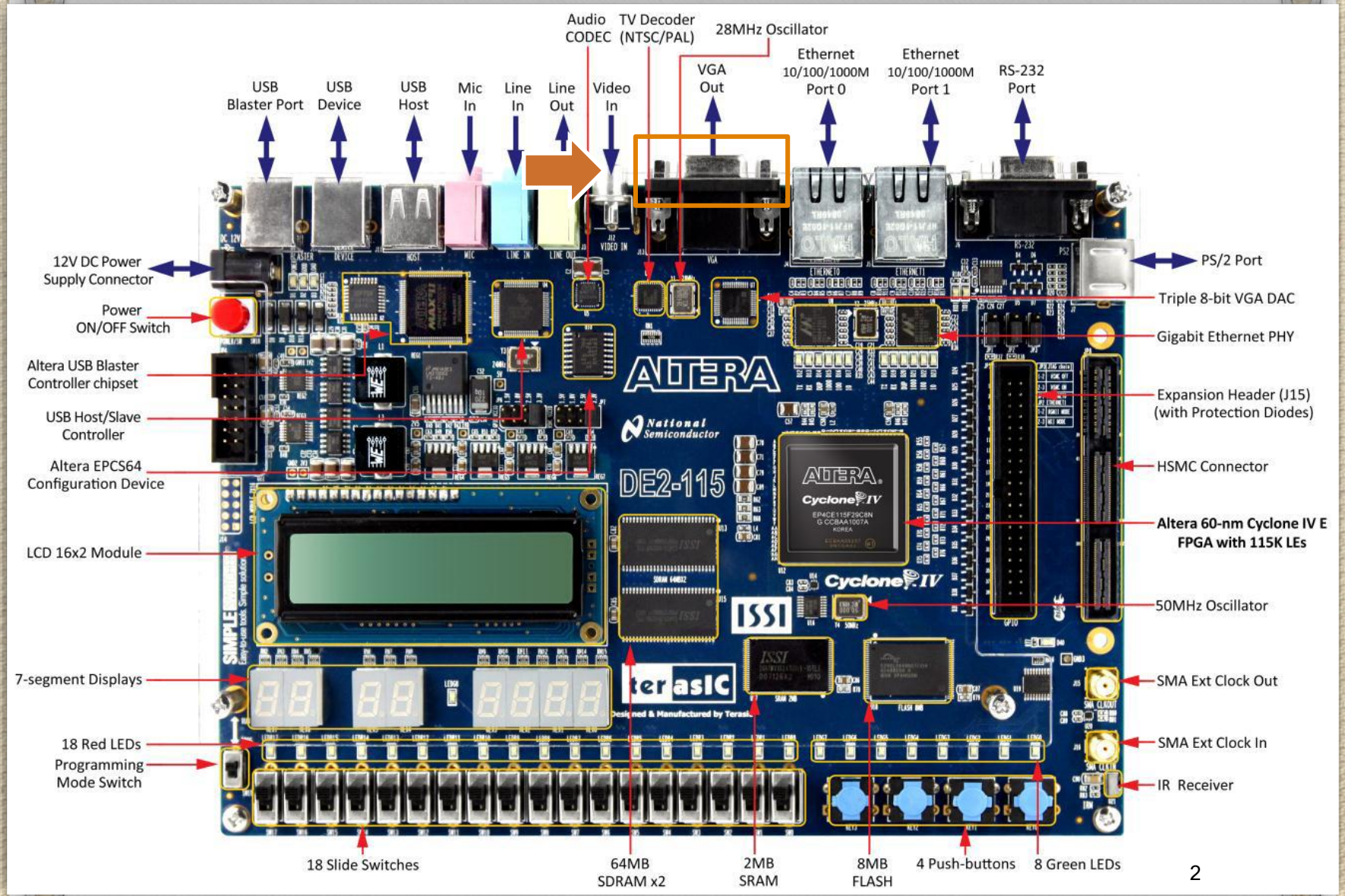
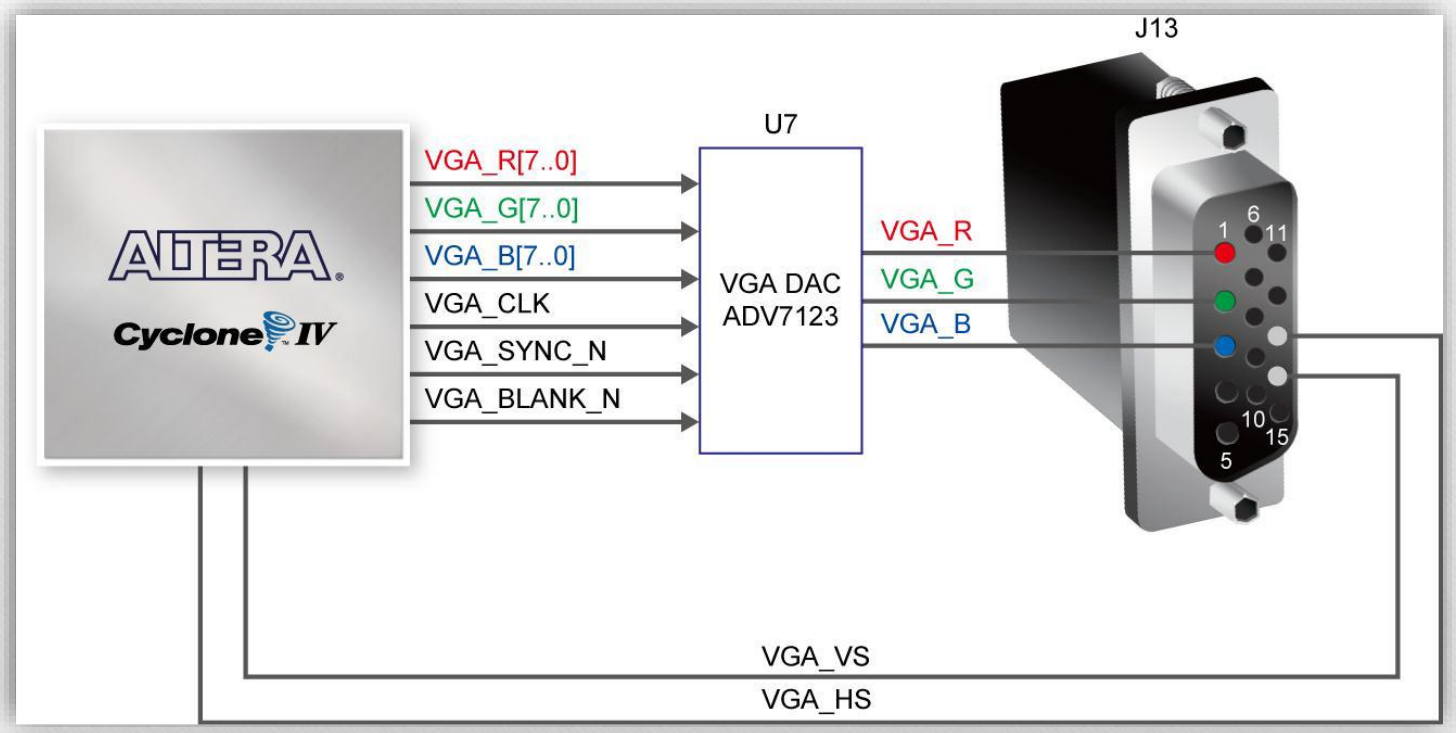


Introduction

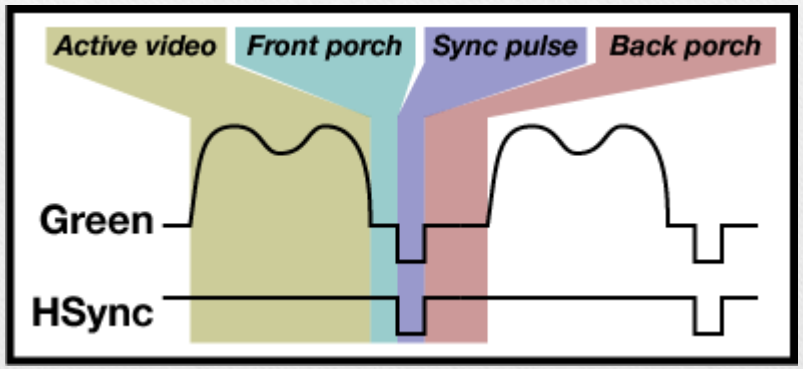
- The DE2-115 board includes a 15-pin D-SUB connector for VGA (Video Graphics Array) output.
- The VGA synchronization signals are provided directly from the Cyclone IV E FPGA
- The Analog Devices ADV7123 triple 10-bit high-speed video DAC (only the higher 8-bit are used) is used to produce the analog data signals (red, green, and blue).

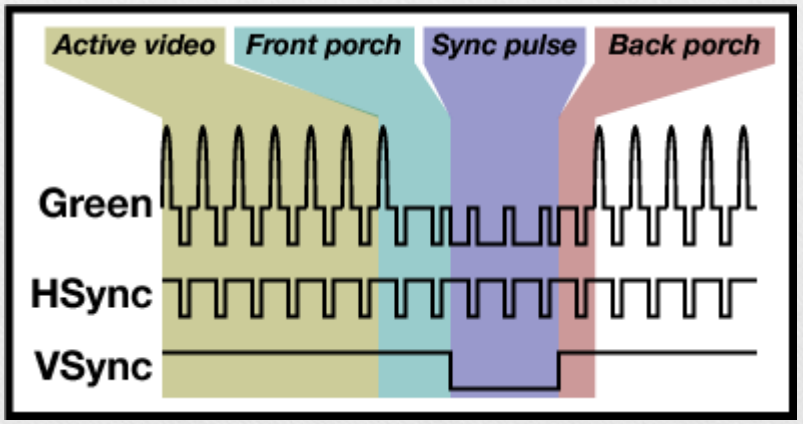
Introduction



Timing Specification (1/2)

- This figure illustrates the basic timing requirements for each row (horizontal) and frame (vertical) that is displayed on a VGA monitor.





Timing Specification (2/2)

- During active video interval the RGB data drives each pixel in turn across the row being displayed.
- The data output to the monitor must be off (driven to 0 V) for a time period called the front porch before HSync pulse can occur.
- Then an active-low sync. pulse of specific duration in applied to the horizontal synchronization input of the monitor, which signifies the end of one row of data and the start of the next.
- Finally, there is a time period called the back porch after the HSync pulse occurs, which is followed by the next active video interval.

VGA Signal 640 x 480 @ 60 Hz

General timing

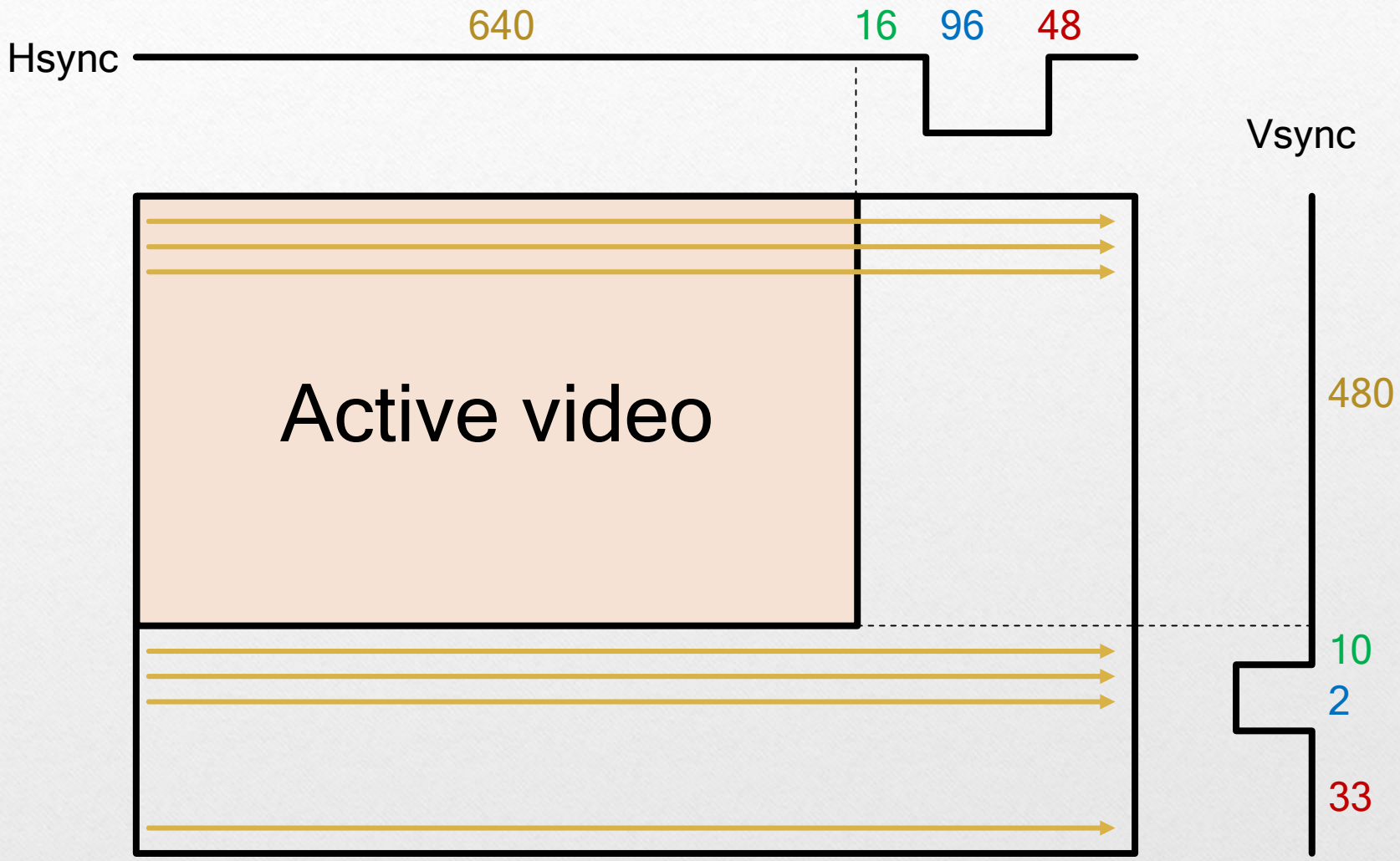
Screen refresh rate	60 Hz
Vertical refresh	31.469 kHz
Pixel freq.	25.175 MHz

Horizontal timing (line)

Scanline part	Pixels	Time [µs]
Active video	640	25.422
Front porch	16	0.636
Sync pulse	96	3.813
Back porch	48	1.907
Whole line	800	31.778

Vertical timing (frame)

Frame part	Pixels	Time [µs]
Active video	480	15.253
Front porch	10	0.318
Sync pulse	2	0.0636
Back porch	33	1.049
Whole frame	525	16.683



VGA Signal 640x480 @ 60 Hz

VGA Signal 800 x 600 @ 60 Hz

General timing

Screen refresh rate	60 Hz
Vertical refresh	37.879 kHz
Pixel freq.	40.0 MHz

Horizontal timing (line)

Scanline part	Pixels	Time [µs]
Active video	800	20
Front porch	40	1
Sync pulse	128	3.2
Back porch	88	2.2
Whole line	1056	26.4

Vertical timing (frame)

Frame part	Pixels	Time [µs]
Active video	600	15.84
Front porch	1	0.026
Sync pulse	4	0.106
Back porch	23	0.607
Whole frame	628	16.58

VGA Signal 1024x 768 @ 60 Hz

General timing

Screen refresh rate	60 Hz
Vertical refresh	48.363 kHz
Pixel freq.	65.0 MHz

Horizontal timing (line)

Scanline part	Pixels	Time [µs]
Active video	1024	15.753
Front porch	24	0.369
Sync pulse	136	2.092
Back porch	160	2.462
Whole line	1344	20.677

Vertical timing (frame)

Frame part	Pixels	Time [µs]
Active video	768	15.880
Front porch	3	0.062
Sync pulse	6	0.124
Back porch	29	0.600
Whole frame	806	16.666

VGA Signal 1280 x 1024 @ 60 Hz

General timing

Screen refresh rate	60 Hz
Vertical refresh	63.981 kHz
Pixel freq.	108.0 MHz

Horizontal timing (line)

Scanline part	Pixels	Time [µs]
Active video	1280	11.852
Front porch	48	0.444
Sync pulse	112	1.037
Back porch	248	2.296
Whole line	1688	15.630

Vertical timing (frame)

Frame part	Pixels	Time [µs]
Active video	1024	16.005
Front porch	1	0.016
Sync pulse	3	0.047
Back porch	38	0.594
Whole frame	1066	16.661

Pin Assignments

Signal Name	FPGA Pin No.	Description
VGA_R[0]~[7]	PIN_E12~H10	VGA Red[0]~[7]
VGA_G[0]~[7]	PIN_G8~C9	VGA Green[0]~[7]
VGA_B[0]~[7]	PIN_B10~D12	VGA Blue[0]~[7]
VGA_CLK	PIN_A12	VGA CLOCK
VGA_BLANK_N	PIN_F11	VGA BLANK
VGA_HS	PIN_G13	VGA HSync
VGA_VS	PIN_C13	VGA VSync
VGA_SYNC_N	PIN_C10	Unused. Just assign 1.

0: Blank
1: Active data

The End.

Any question?

Reference

1. http://www-mtl.mit.edu/Courses/6.111/labkit/vga.shtml
2. http://tinyvga.com/vga-timing
3. "DE2-115 User Manual" by Terasic.