24-bit Audio CODEC

Digital Circuit Lab

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Outline

- Introduction to Audio Signal
- Architecture Overview
- Device Initialization
- Device Operation

Introduction to Audio Signal

Introduction

- An audio signal is a representation of sound, typically as an electrical voltage.
- Audio signals have frequencies in the audio frequency range of roughly 20 to 20,000 Hz.
- Audio signals may be synthesized directly, or may originate at a transducer such as a microphone.
- Loudspeakers or headphones convert an electrical audio signal into sound.

Line Level (1/2)

- Line level is the specified strength of an audio signal used to transmit analog sound between audio components.
- As opposed to line level, there are weaker audio signals, such as those from microphones, and stronger signals, such as those used to drive headphones and loudspeakers.

Line Level (2/2)

- Consumer electronic devices concerned with audio (for example sound cards) often have a connector labeled "line in" and/or "line out."
- The line in/out connections on a consumer-oriented computer sound card are unbalanced, with a 3.5 mm (1/8") 3-conductor TRS minijack connector providing ground, left channel, and right channel.
- Professional equipment commonly uses balanced connections on 6.35 mm (1/4") phone jacks or XLR connectors.

Line In V.S. Mic In

- A line input level signal typically has a voltage ranging from 0.3 to 2 Volts.
- A microphone input level signal is more often in the range from 5 to 50 mV (millivolts).
  - Need microphone input level boost.

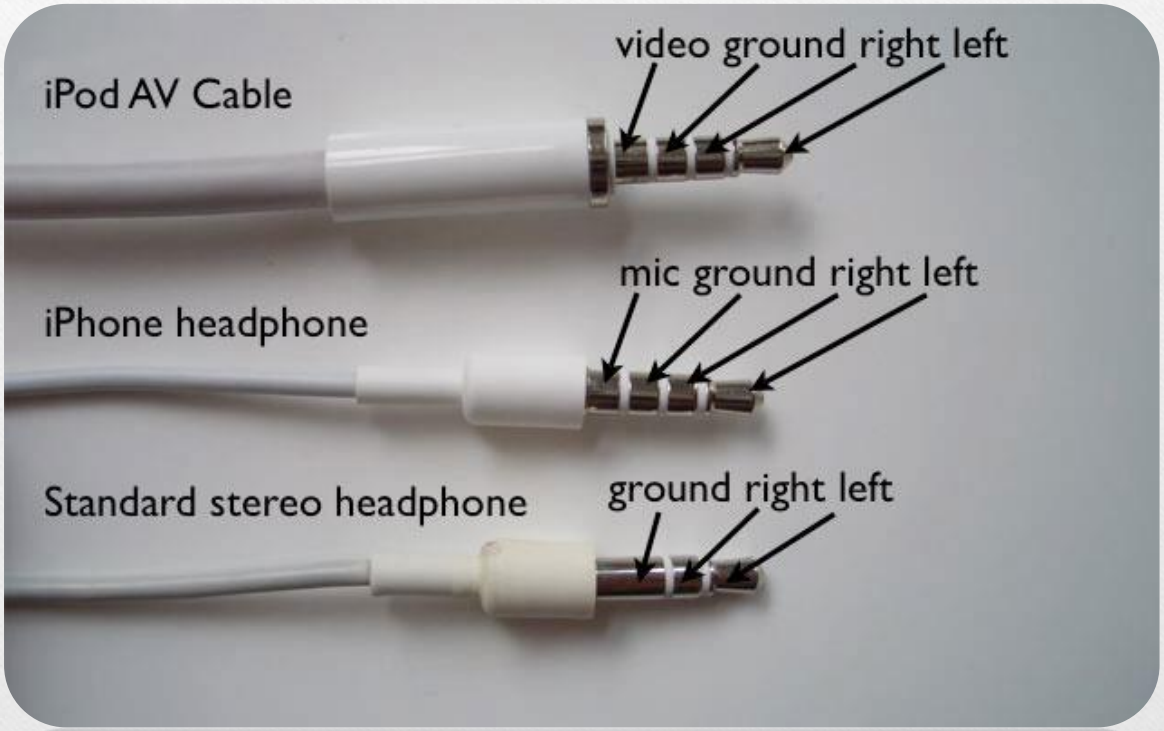
Phone Connector (1/3)

- In electronics, a phone connector is a common family of connector typically used for analog signals, primarily audio.
  - It is also termed an audio jack, phone jack, etc.
- It is cylindrical in shape, typically with two, three or four contacts.
- Three-contact versions are known as TRS connectors, where T stands for "tip", R stands for "ring" and S stands for "sleeve".
- Similarly, two- and four-contact versions are called TS and TRRS connectors respectively.

Phone Connector (2/3)

- Modern phone connectors are available in three standard sizes.
  - 2.5 mm mono (TS)
  - 3.5 mm mono (TS)
  - 3.5 mm stereo (TRS)
  - 6.35 mm (1⁄4 in) (TRS)

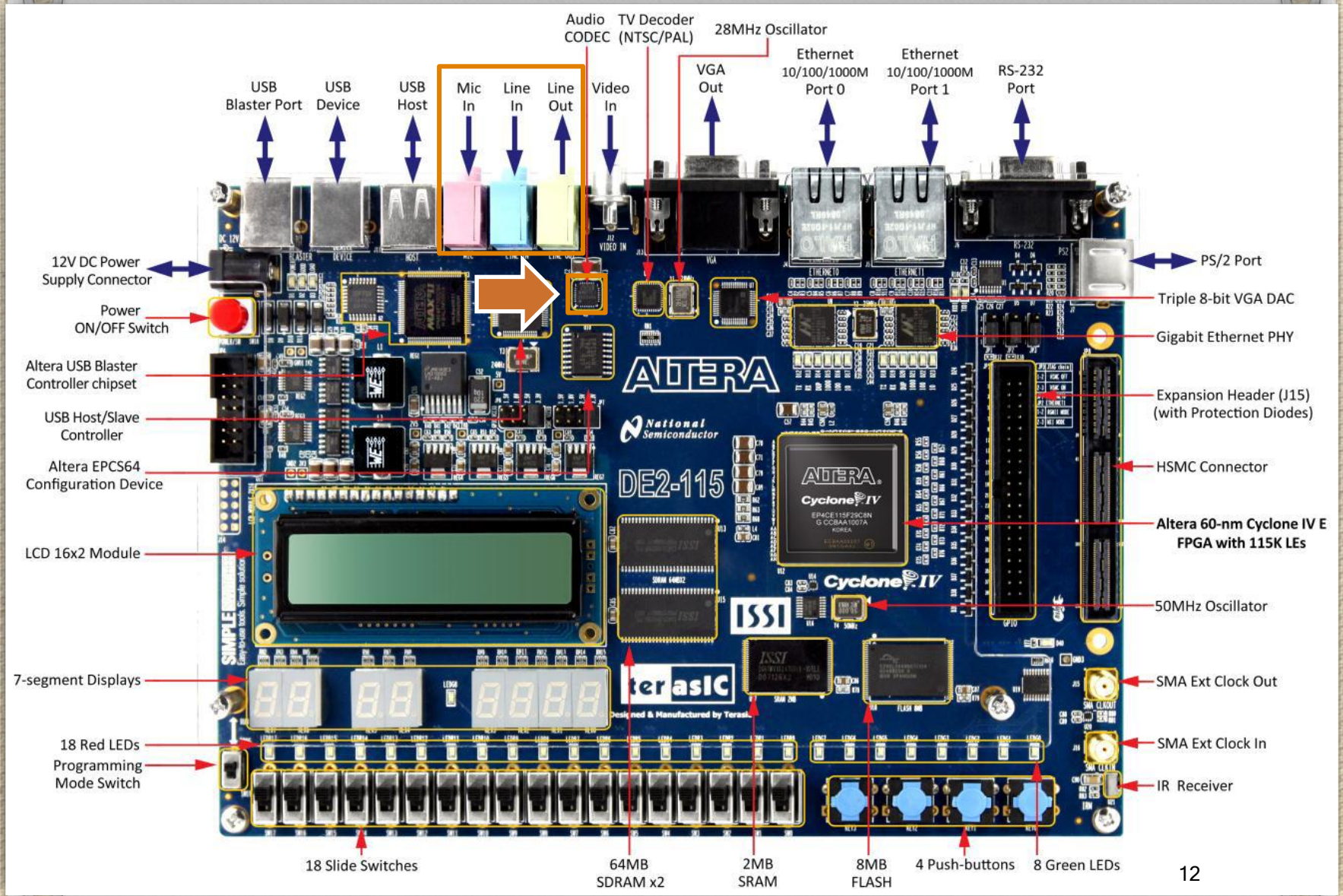
Phone Connector (3/3)



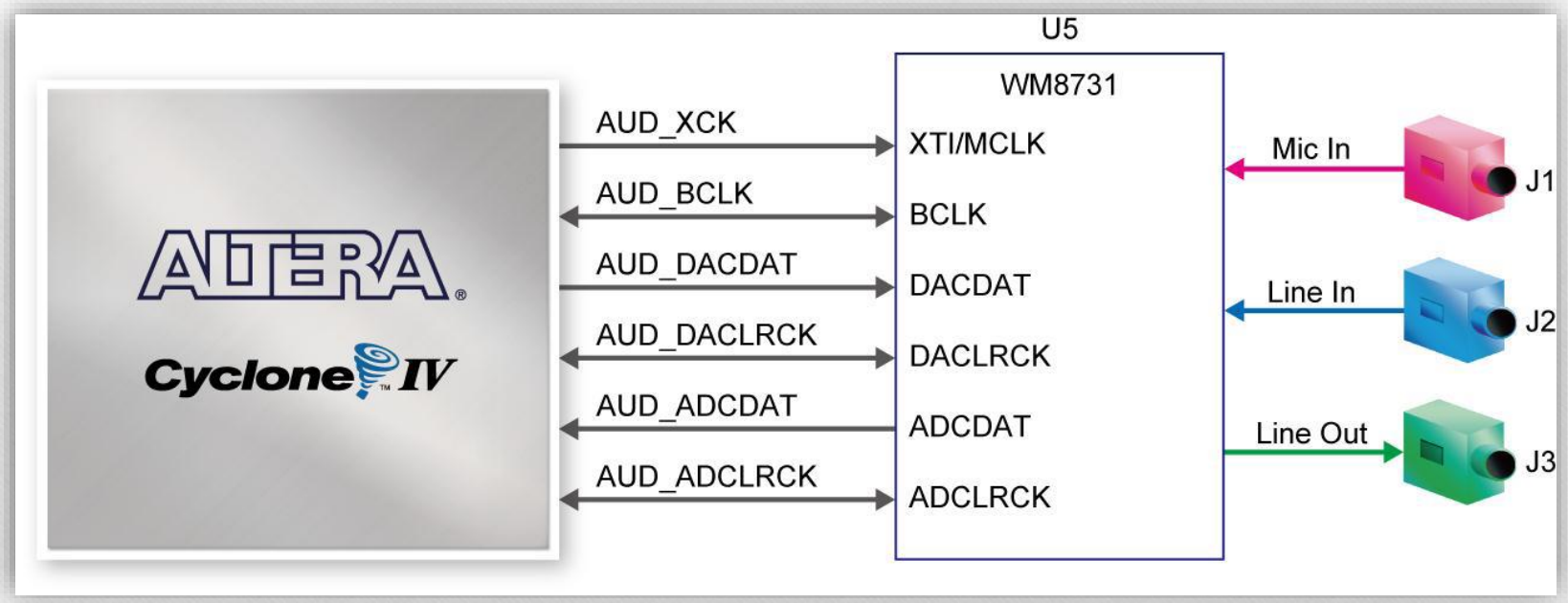
http://appleinsider.com/articles/09/02/12/macbook_owners_frustrated_by_new_audio_jacks

Architecture Overview

DE2_115_User_manual\DE2_115_User_manual.pd



Schematic Diagram



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Audio CODEC Pin Assignments

Signal Name	FPGA Pin No.	Description
I2C_SCLK	PIN_B7	I2C Clock
I2C_SDAT	PIN_A8	I2C Data
AUD_XCK	PIN_E1	Audio CODEC Chip Clock
AUD_BCLK	PIN_F2	Audio CODEC Bit-Steam Clock
AUD_ADCLRCK	PIN_C2	Audio CODEC ADC LR Clock
AUD_ADCDAT	PIN_D2	Audio CODEC ADC Data
AUD_DACLRCK	PIN_E3	Audio CODEC DAC LR Clock
AUD_DACDAT	PIN_D1	Audio CODEC DAC Data

Audio chip and TV decoder chip share one I2C bus

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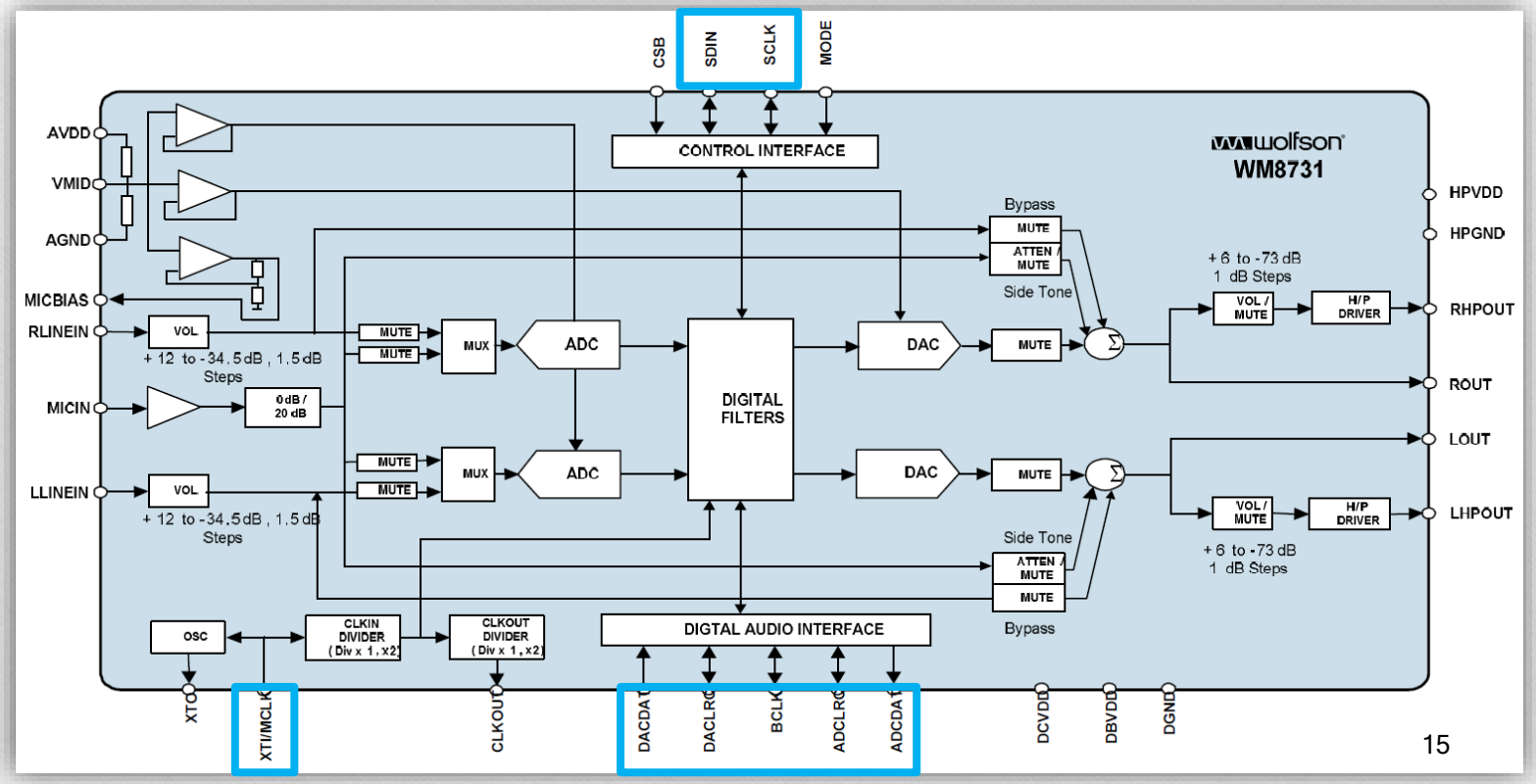
WM8731 Block Diagram



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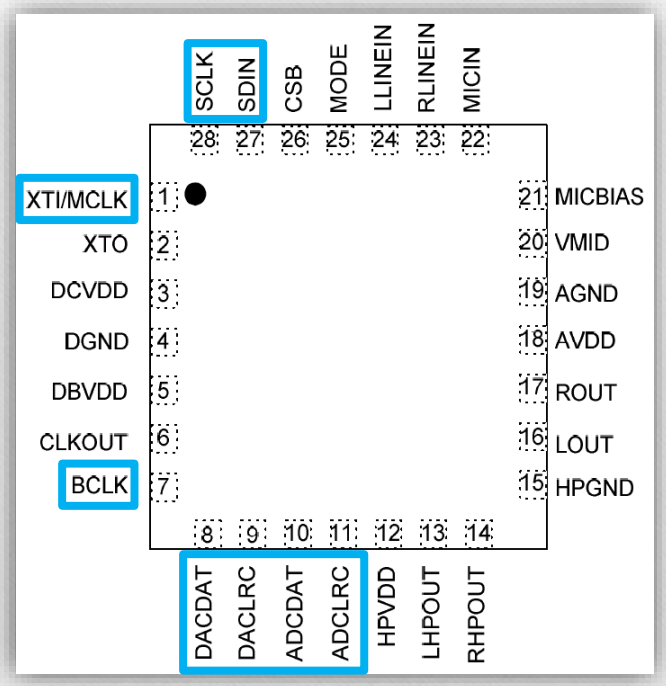
WM8731 Pin Configuration

- Top view of 28 pin QFN



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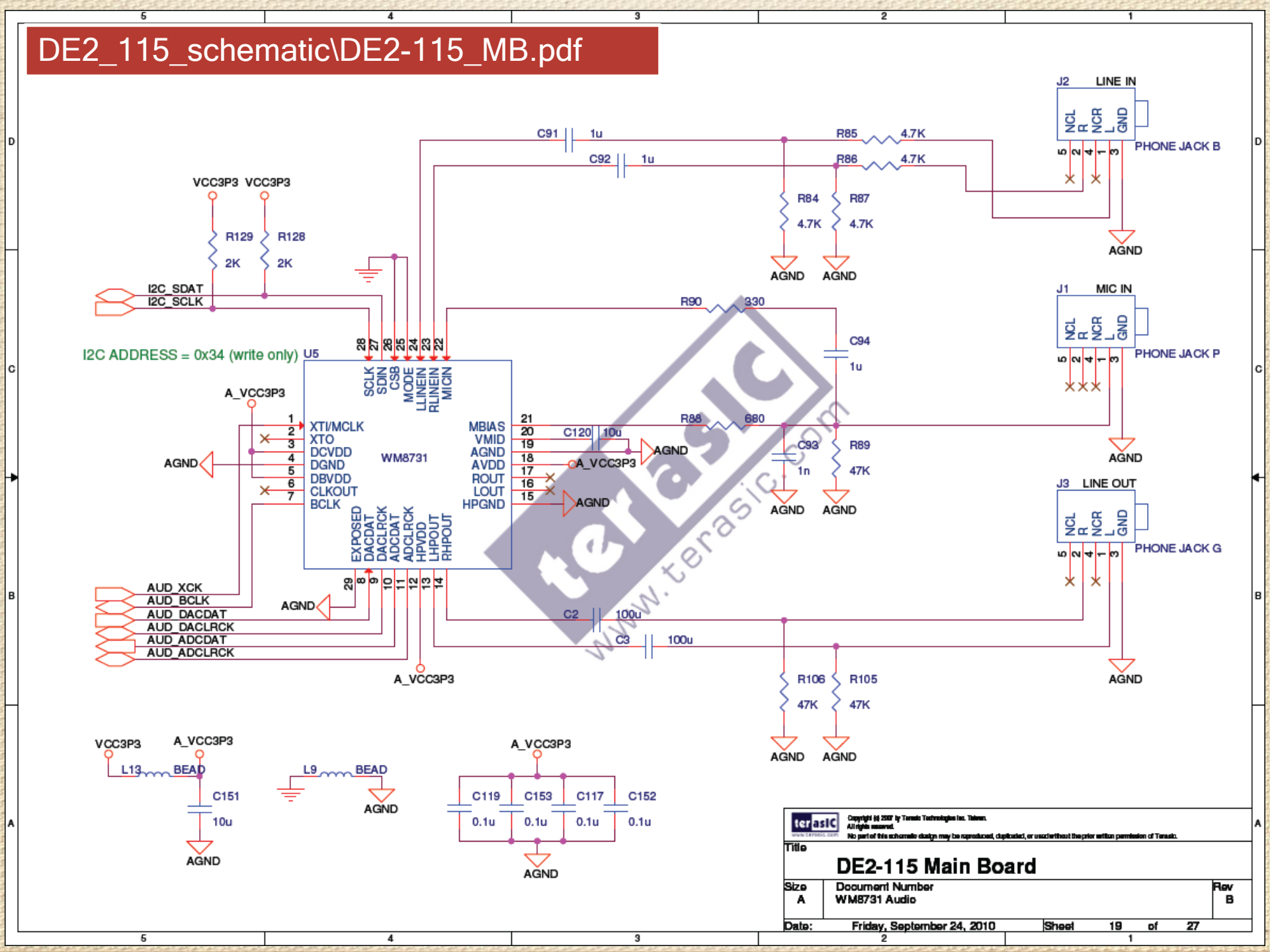


Title	DE2-115 Main Board	
Size A	Document Number WM8731 Audio	Rev B
Date: Friday, September 24, 2010	Sheet 19 of 27	

How to Use WM8731?

1. Initialize the device by setting the registers via I2C bus interface.
2. After correct initialization, we can receive or transmit audio data via digital audio interface.

Device Initialization

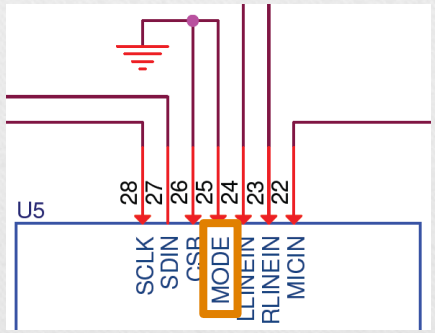
Software Control Interface (1/2)

- Different modes can be configured under software control.
  - Input to ADC: Microphone
  - Sampling rate: 32kHz
  - Input audio data bit length: 16 bits
  - etc.

Software Control Interface (2/2)

- Selection of serial control mode
  - The serial control interface may be selected to operate in either 2 or 3-wire modes. This is achieved by setting the state of the MODE pin.

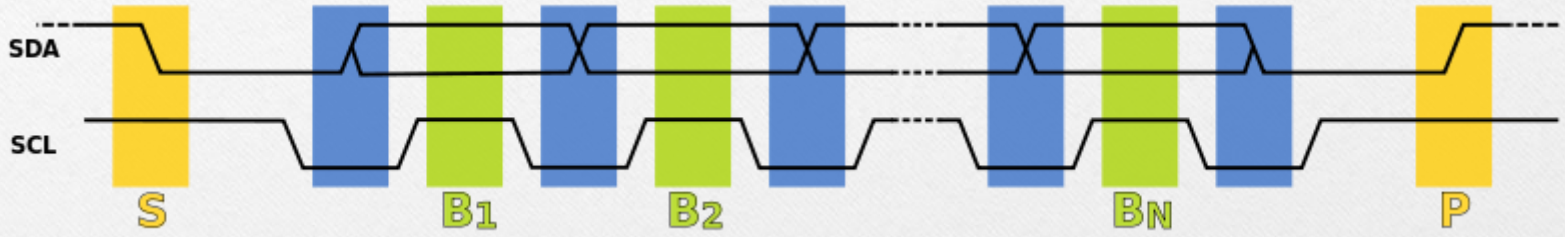
MODE	INTERFACE FORMAT
0	2 wire
1	3 wire



2-Wire Serial Control Mode

- The WM8731/L supports a 2-wire MPU (Microprocessor unit) interface, which is compatible with I²C protocol.
  - I²C (Inter-Integrated Circuit, referred to as I-squared-C) uses only two bidirectional open-drain lines, Serial Data Line (SDA) and Serial Clock (SCL).

I²C protocol (1/4)

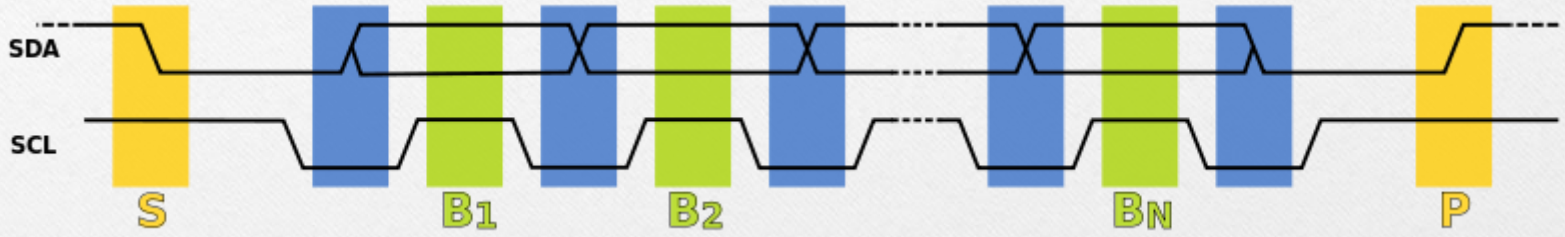


- Data transfer in initiated with the START bit (S) when SDA is **pulled low** while SCL stays high.

SDA=1'b0

- Then, SDA sets the transferred bit while SCL is low (blue) and the data is sampled (received) when SCL rises (green).

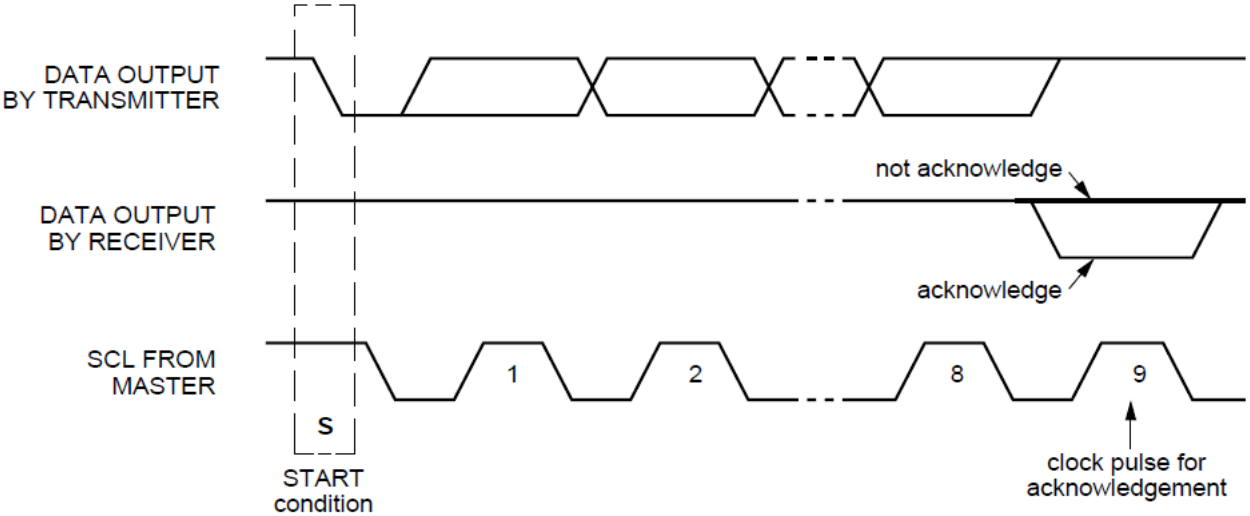
I²C protocol (2/4)



- When the transfer is complete, a STOP bit (P) is sent by **releasing** the data line to allow it to be pulled up while SCL is constantly high. SDA=1'b1 or SDA=1'bz
- In order to avoid false marker detection, the level on SDA is changed on the falling edge and is captured on the rising edge of SCL.

I²C protocol (3/4)

- After every 8 data bits in one direction, an "acknowledge" bit (0) is transmitted in the other direction.



I²C protocol (4/4)

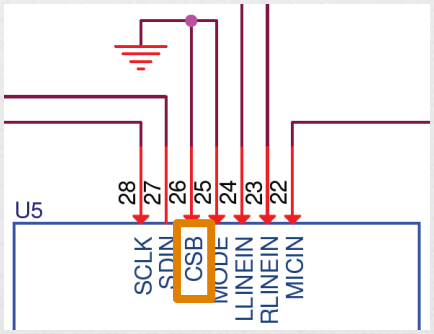
- About inout port:

```
module inout_port(oe, clk, SDA)

input oe; // output enable
input clk;
inout SDA;

wire a; // output data
reg b; // input data

assign SDA = oe? a: 1'bz;

always @(posedge clk) begin
    b <= SDA;
end
```

2-Wire Interface (1/2)

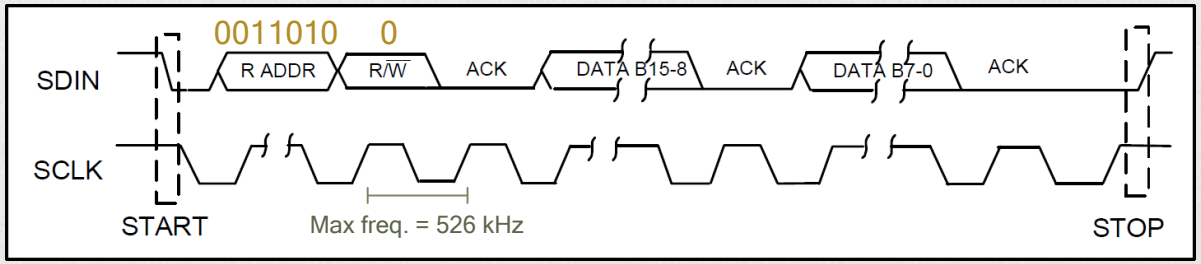
- The device operates as a slave device only.
- The WM8731/L has one of two slave address that are selected by setting the state of the CSB pin.

CSB STATE	ADDRESS
0	0011010
1	0011011



2-Wire Interface (2/2)

- 2-wire serial interface
  - ADDR[6:0] (7 bits) are Slave Address Bits
  - R/W is '0', indicating a write
  - B[15:9] (7 bits) are Register Address Bits
  - B[8:0] (9 bits) are Register Data Bits



Register Map

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R0 (00h) Left Line In	LRINBOTH	LINMUTE	0	0	LINVOL[4:0]					0_1001_0111
R1 (01h) Right Line In	RLINBOTH	RINMUTE	0	0	RINVOL[4:0]					0_1001_0111
R2 (02h) Left Headphone Out	LRHPBOTH	LZCEN	LHPVOL[6:0]							0_0111_1001
R1 (01h) Right Headphone Out	RLHPBOTH	RZCEN	RHPVOL[6:0]							0_0111_1001
R4 (04h) Analogue Audio Path Control	0	SIDEATT[1:0]		SIDETONE	DACSEL	BYPASS	INSEL	MUTEMIC	MICBOOST	0_0000_1010
R5 (05h) Digital Audio Path Control	0	0	0	0	HPOR	DACMU	DEEMPH[1:0]		ADCHPD	0_0000_1000
R6 (06h) Power Down Control	0	POWEROFF	CLKOUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD	0_1001_1111
R7 (07h) Digital Audio Interface Format	0	BCLKINV	MS	LRSWAP	LRP	IWL[1:0]		FORMAT[1:0]		0_1001_1111
R8 (08h) Sampling Control	0	CLKODIV2	CLKIDIV2	SR[3:0]				BOSR	USB/ NORMAL	0_0000_0000
R9 (09h) Active Control	0	0	0	0	0	0	0	0	Active	0_0000_0000
R15 (0Fh) Reset	RESET[8:0]									not reset

Check the WM8731/L document to see the details.

Left Line In

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R0 (00h) Left Line In	LRINBOTH	LINMUTE	0	0	LINVOL[4:0]					0_1001_0111

- Just use the default setting if we do not use the line input.
  - 000_0000_0_1001_0111

Right Line In

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R1 (01h) Right Line In	RLINBOTH	RINMUTE	0	0	RINVOL[4:0]					0_1001_0111

- Just use the default setting if we do not use the line input.
  - 000_0001_0_1001_0111

Left Headphone Out

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R2 (02h) Left Headphone Out	LRHPBOTH	LZCEN	LHPVOL[6:0]							0_0111_1001

- Here we can just use the default setting.
  - 000_0010_0_0111_1001

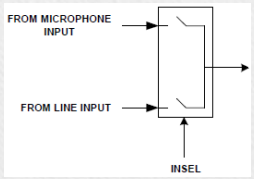
Right Headphone Out

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R3 (03h) Right Headphone Out	RLHPBOTH	RZCEN	RHPVOL[6:0]							0_0111_1001

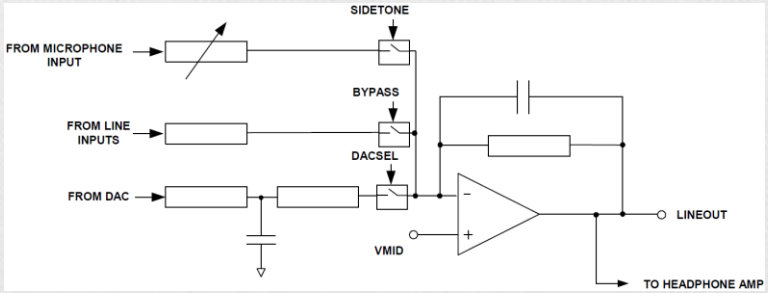
- Here we can just use the default setting.
  - 000_0011_0_0111_1001

Analogue Audio Path Control

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R4 (04h) Analogue Audio Path Control	0	SIDEATT[1:0]		SIDETONE	DACSEL	BYPASS	INSEL	MUTEMIC	MICBOOST	0_0000_1010



- Enable boost, disable mute, choose microphone input, disable bypass, and select DAC.
  - 000_0100_0_0001_0101



Digital Audio Path Control

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R5 (05h) Digital Audio Path Control	0	0	0	0	HPOR	DACMU	DEEMPH[1:0]		ADCHPD	0_0000_1000

- Disable soft mute
  - 000_0101_0_0000_0000

Power Down Control

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R6 (06h) Power Down Control	0	POWER OFF	CLKOUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD	0_1001_1111

- Choose power on and disable all the power down options.
  - 000_0110_0_0000_0000

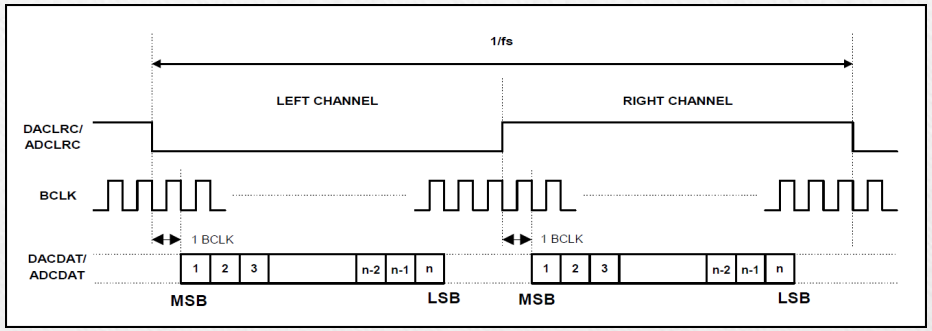
Digital Audio Interface Format (1/2)

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R7 (07h) Digital Audio Interface Format	0	BCLKIVE	MS	LRSWAP	LRP	IWL[[1:0]		FORMAT[1:0]		0_0000_1010

- Choose I^2S format, 16-bit length, and master mode.
  - 000_0111_0_0100_**0010**

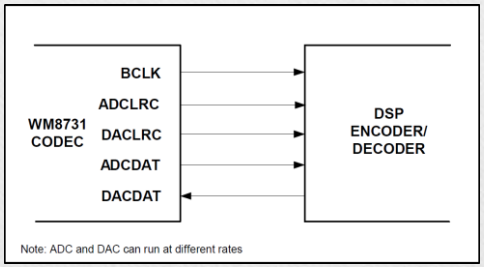
Digital Audio Interface Format (2/2)

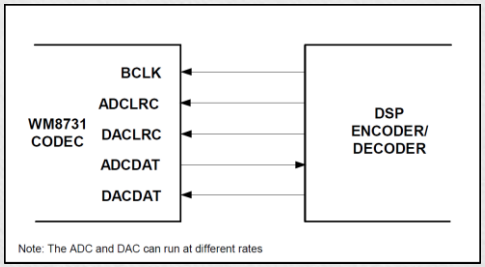
- I²S format



➢ 16-bit length

- Master mode v.s. Slave mode





Sampling Control (1/2)

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R8 (08h) Sampling Control	0	CLKODIV2	CLKIDIV2	SR[3:0]				BOSR	USB/ Normal	0_0000_0000

- Choose USB mode (fixed MCLK 12MHz) and sampling rate = 32 kHz.
  - 000_1000_0_0001_1001

Sampling Control (2/2)

SAMPLING RATE		MCLK FREQUENCY	SAMPLE RATE REGISTER SETTINGS					DIGITAL FILTER TYPE
ADC	DAC							
kHz	kHz	MHz	BOSR	SR3	SR2	SR1	SR0	
48	48	12.000	0	0	0	0	0	0
44.1 (Note 2)	44.1 (Note 2)	12.000	1	1	0	0	0	1
48	8	12.000	0	0	0	0	1	0
44.1 (Note 2)	8 (Note 1)	12.000	1	1	0	0	1	1
8	48	12.000	0	0	0	1	0	0
8 (Note 1)	44.1 (Note 2)	12.000	1	1	0	1	0	1
8	8	12.000	0	0	0	1	1	0
8 (Note 1)	8 (Note 1)	12.000	1	1	0	1	1	1
32	32	12.000	0	0	1	1	0	0
96	96	12.000	0	0	1	1	1	3
88.2 (Note 3)	88.2 (Note 3)	12.000	1	1	1	1	1	2

Active Control

REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R9 (09h) Active Control	0	0	0	0	0	0	0	0	Active	0_0000_0000

- Activate interface
  - 000_1001_0_0000_0001

Reset Register

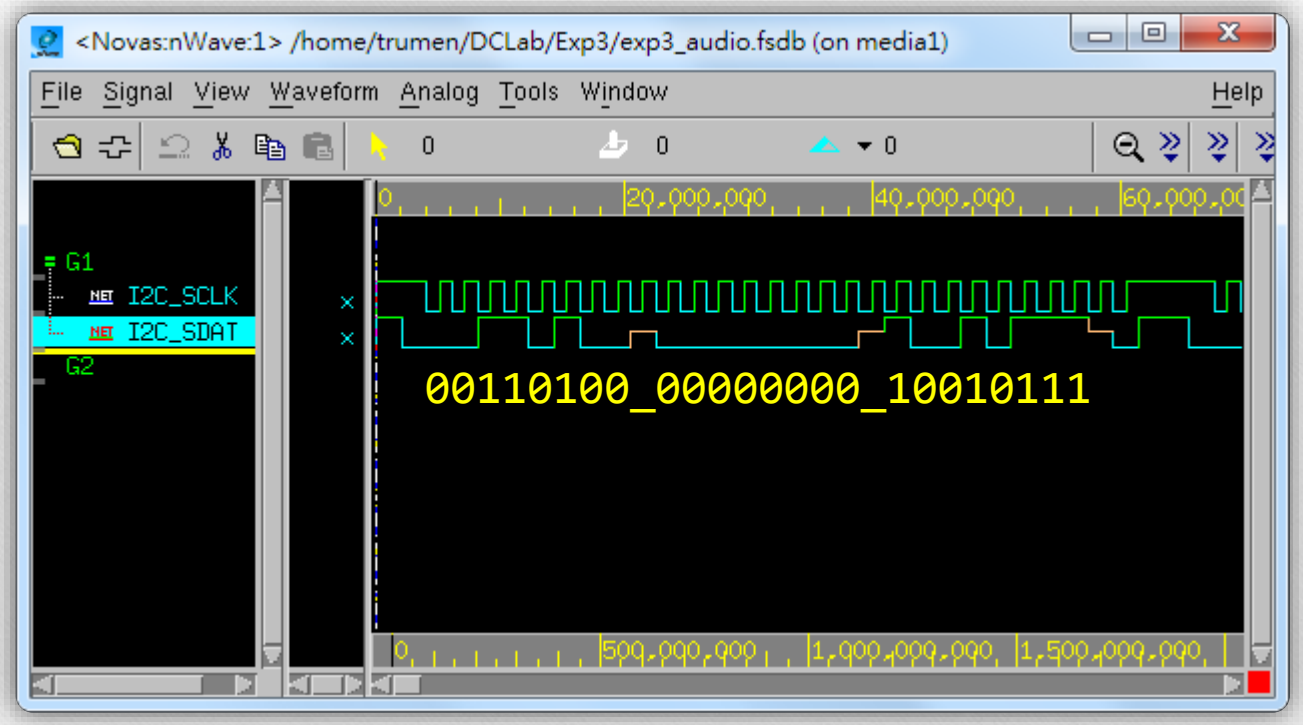
REGISTER	BIT[8]	BIT[7]	BIT[6]	BIT[5]	BIT[4]	BIT[3]	BIT[2]	BIT[1]	BIT[0]	DEFAULT
R15 (15h) Active Control	RESET[8:0]									not reset

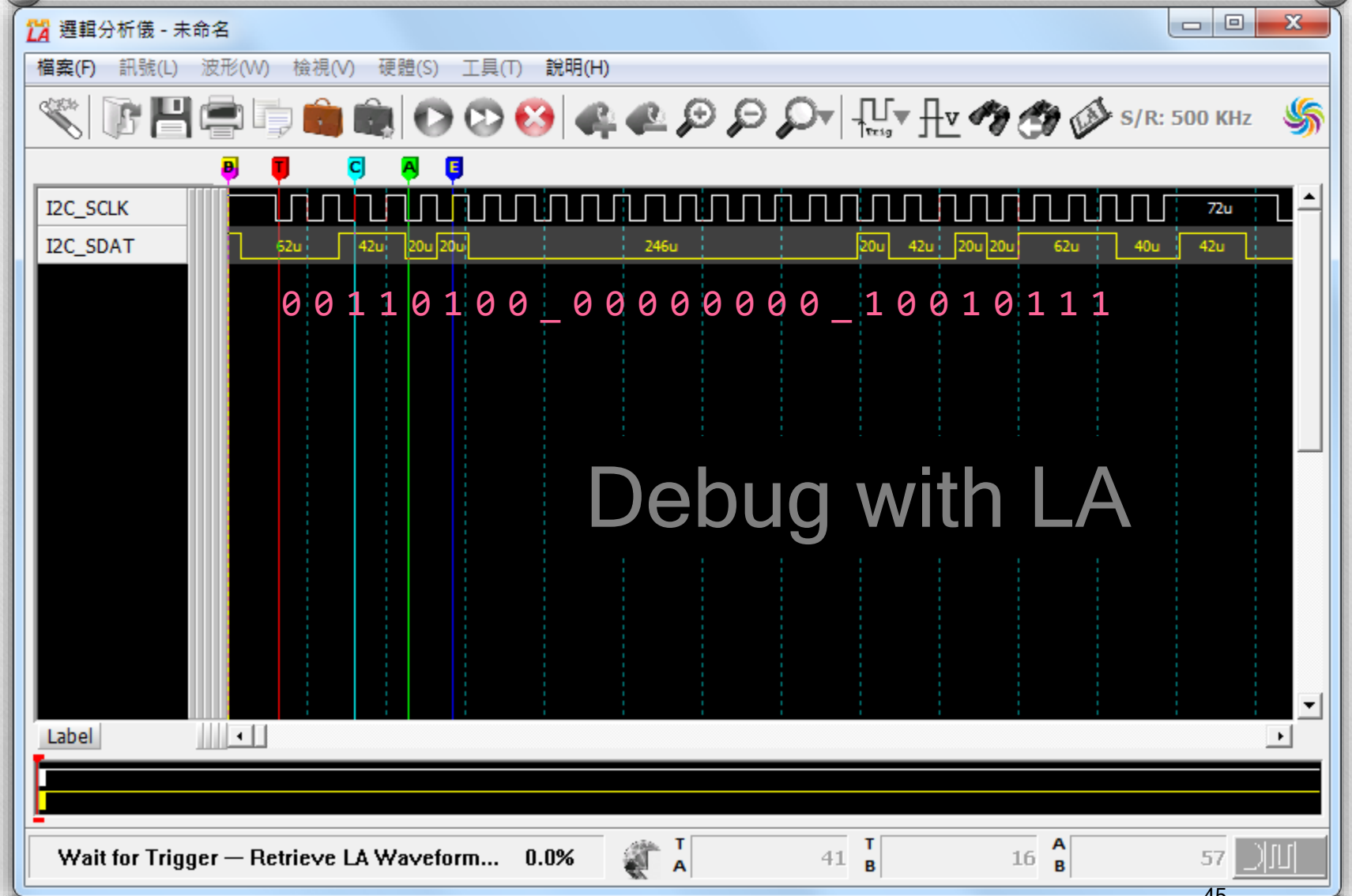
- You can try to reset the device to a known (?) state.
  - 000_1111_0_0000_0000 (?)

Recommended settings

Left Line In	000_0000_0_1001_0111
Right Line In	000_0001_0_1001_0111
Left Headphone Out	000_0010_0_0111_1001
Right Headphone Out	000_0011_0_0111_1001
Analogue Audio Path Control	000_0100_0_0001_0101
Digital Audio Path Control	000_0101_0_0000_0000
Power Down Control	000_0110_0_0000_0000
Digital Audio Interface Format	000_0111_0_0100_0010
Sampling Control	000_1000_0_0001_1001
Active Control	000_1001_0_0000_0001

Check the Waveform

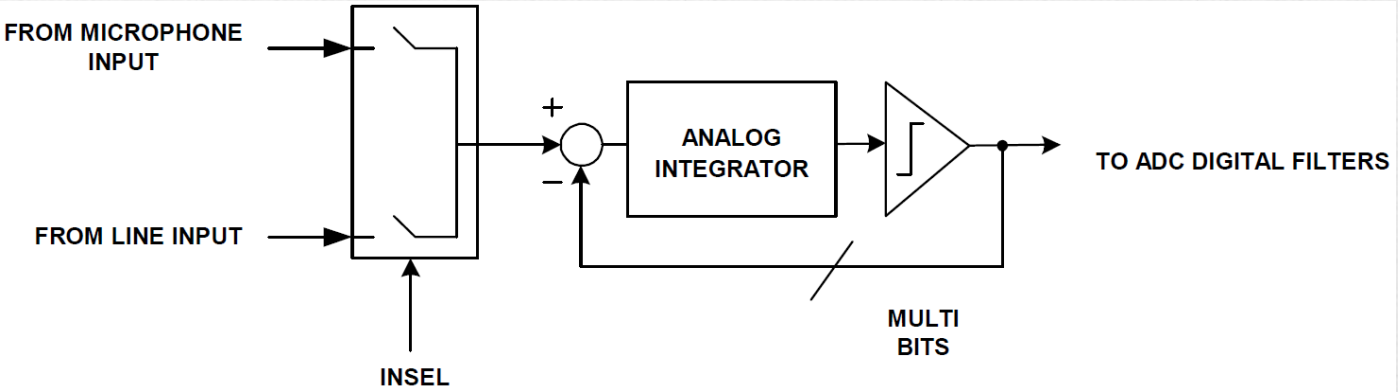



邏輯分析儀 - 未命名
檔案(F) 訊號(L) 波形(W) 檢視(V) 硬體(S) 工具(T) 說明(H)
S/R: 500 KHz
B T C A E
I2C_SCLK
I2C_SDAT
72u
62u 42u 20u 20u 246u 20u 42u 20u 20u 62u 40u 42u
0 0 1 1 0 1 0 0 _ 0 0 0 0 0 0 0 0 _ 1 0 0 1 0 1 1 1
Debug with LA
Label
Wait for Trigger — Retrieve LA Waveform... 0.0%
T A 41
T B 16
A B 57

Device Operation

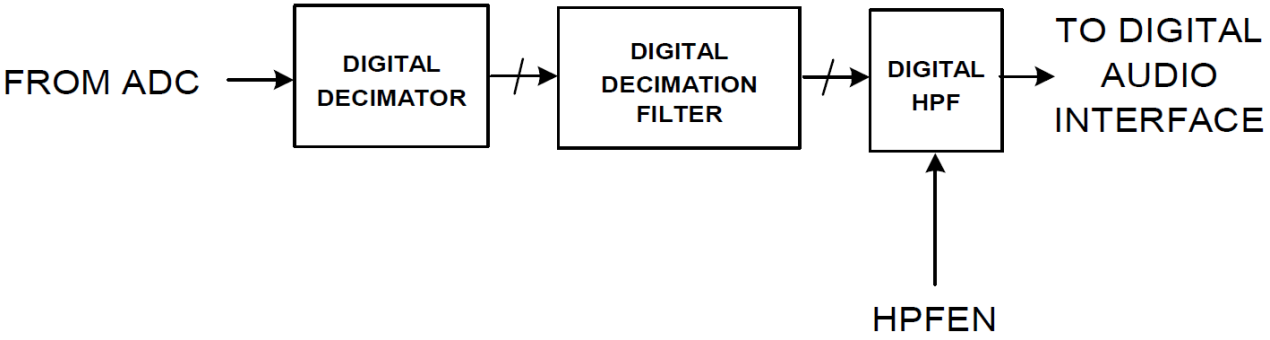
ADC

- The WM8731/L uses a multi-bit oversampled sigma-delta ADC. A single channel of the ADC is illustrated below.



ADC Filters

- The ADC filters perform true 24 bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface.

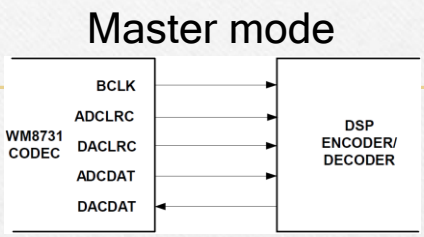


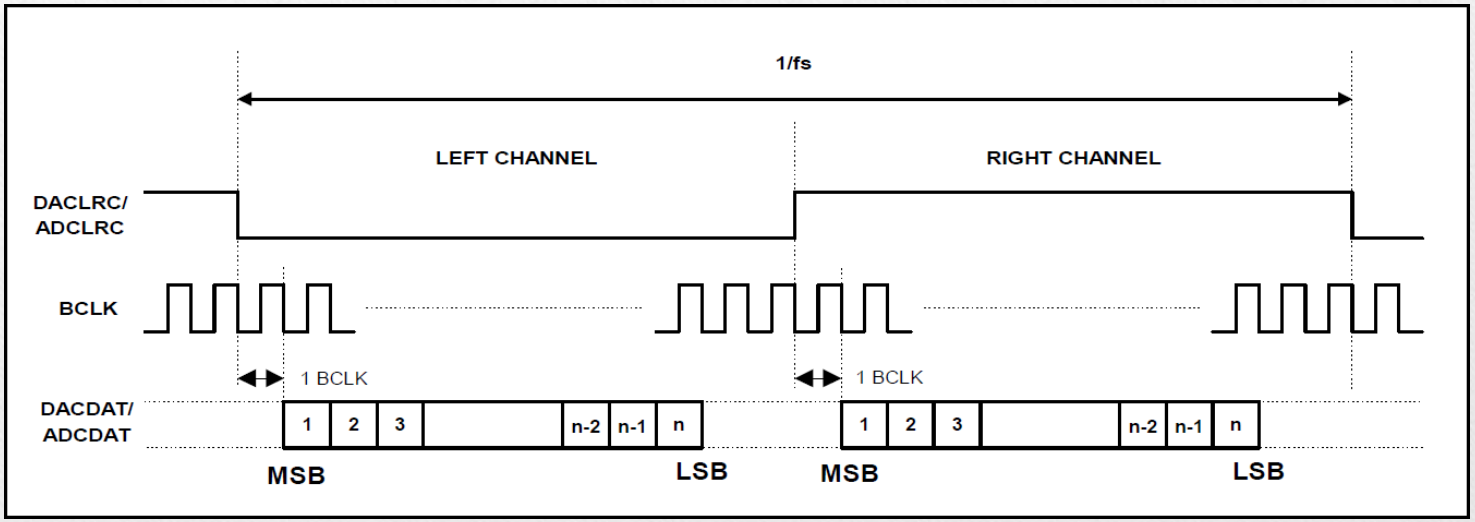
Digital Audio Interfaces (1/5)

- WM8731/L may be operated in either one of the 4 offered audio interface modes. These are:
  - Right justified
  - Left justified
  - I^2S
  - DSP mode
- All four of these modes are MSB first and operate with data 16 to 32 bits.

Digital Audio Interfaces (2/5)

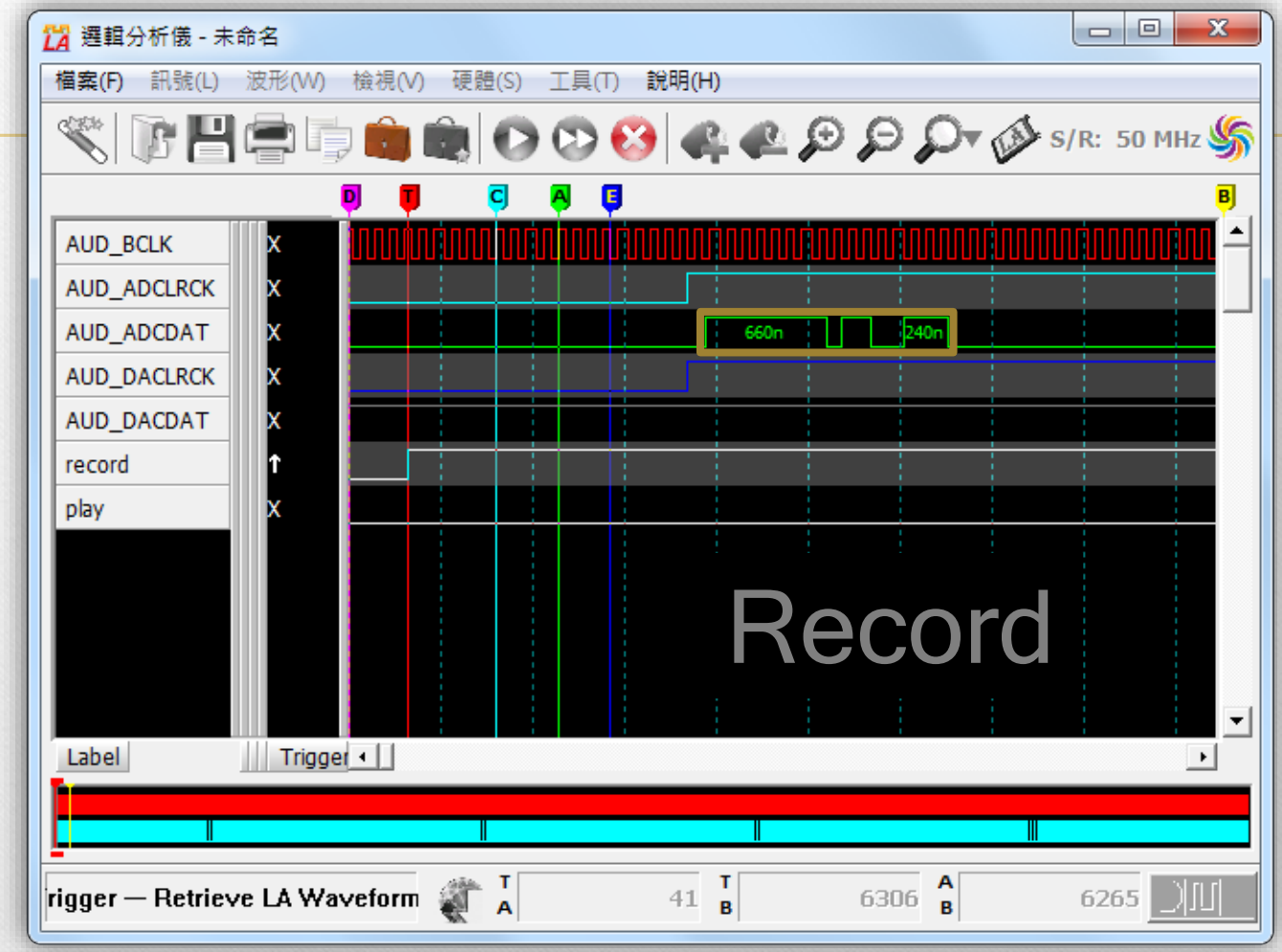
- I²S mode



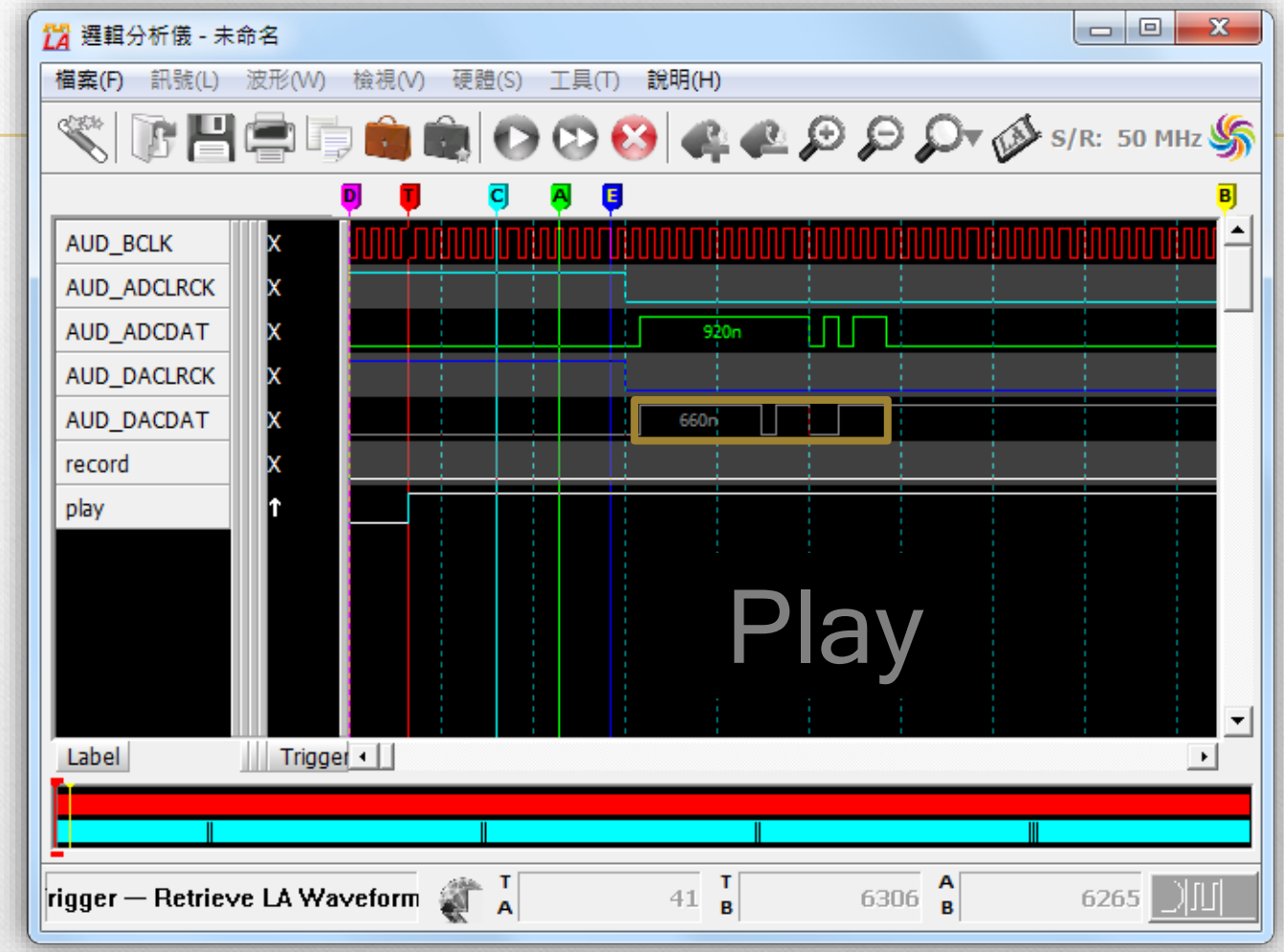


n = 16, 20, 24, or 32

Digital Audio Interfaces (3/5)



Digital Audio Interfaces (4/5)

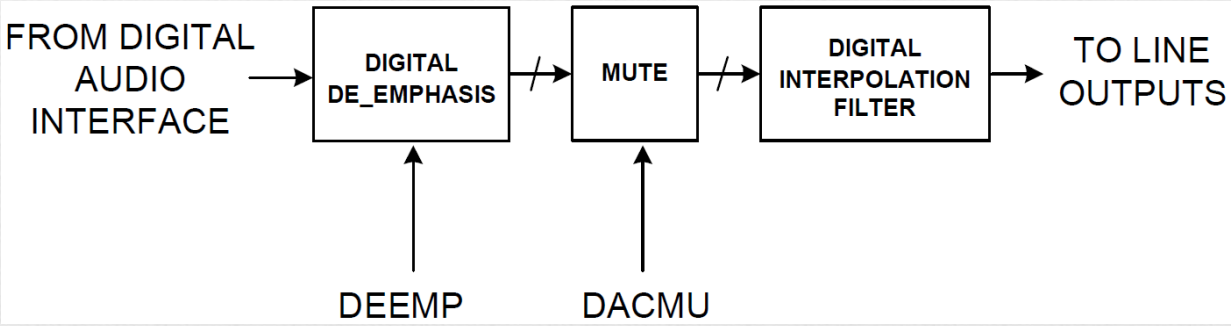


Digital Audio Interfaces (5/5)

- The length of the digital audio data is programmable at 16/20/24 or 32 bits.
- The data is signed 2's complement.
  - If the ADC is programmed to output 16 or 20 bit data then it strips the LSBs from the 24 bit data.
  - If the ADC is programmed to output 32 bits then it packs the LSBs with zeros.
  - Similar adjustments in DAC.

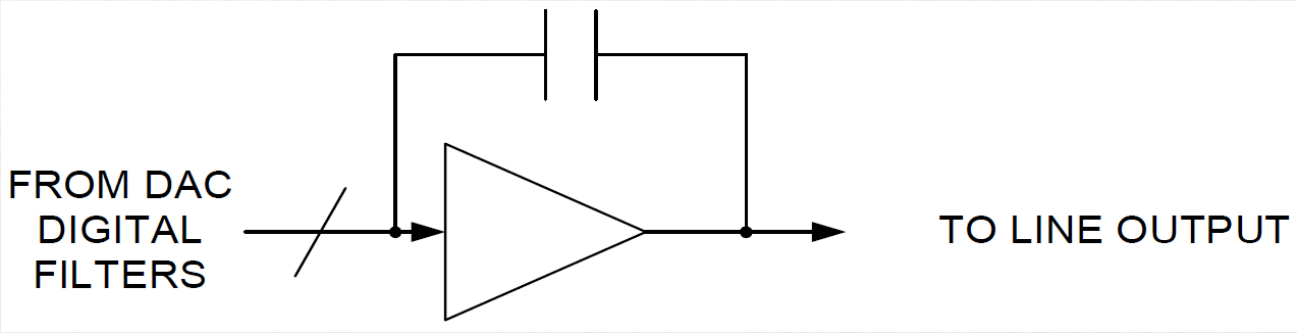
DAC Filters

- The DAC filters perform true 24 bit signal processing to convert the incoming digital audio data from the digital audio interface at the specified sample rate to multi-bit oversampled data for processing by the analogue DAC.



DAC

- The WM8731/L employs a multi-bit sigma delta oversampling digital to analogue converter.



The End.

Any question?

Reference

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2. http://en.wikipedia.org/wiki/I%C2%B2C
3. "THE I 2C-BUS SPECIFICATION VERSION 2.1" by Philips.
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