Memory Devices on DE2-115

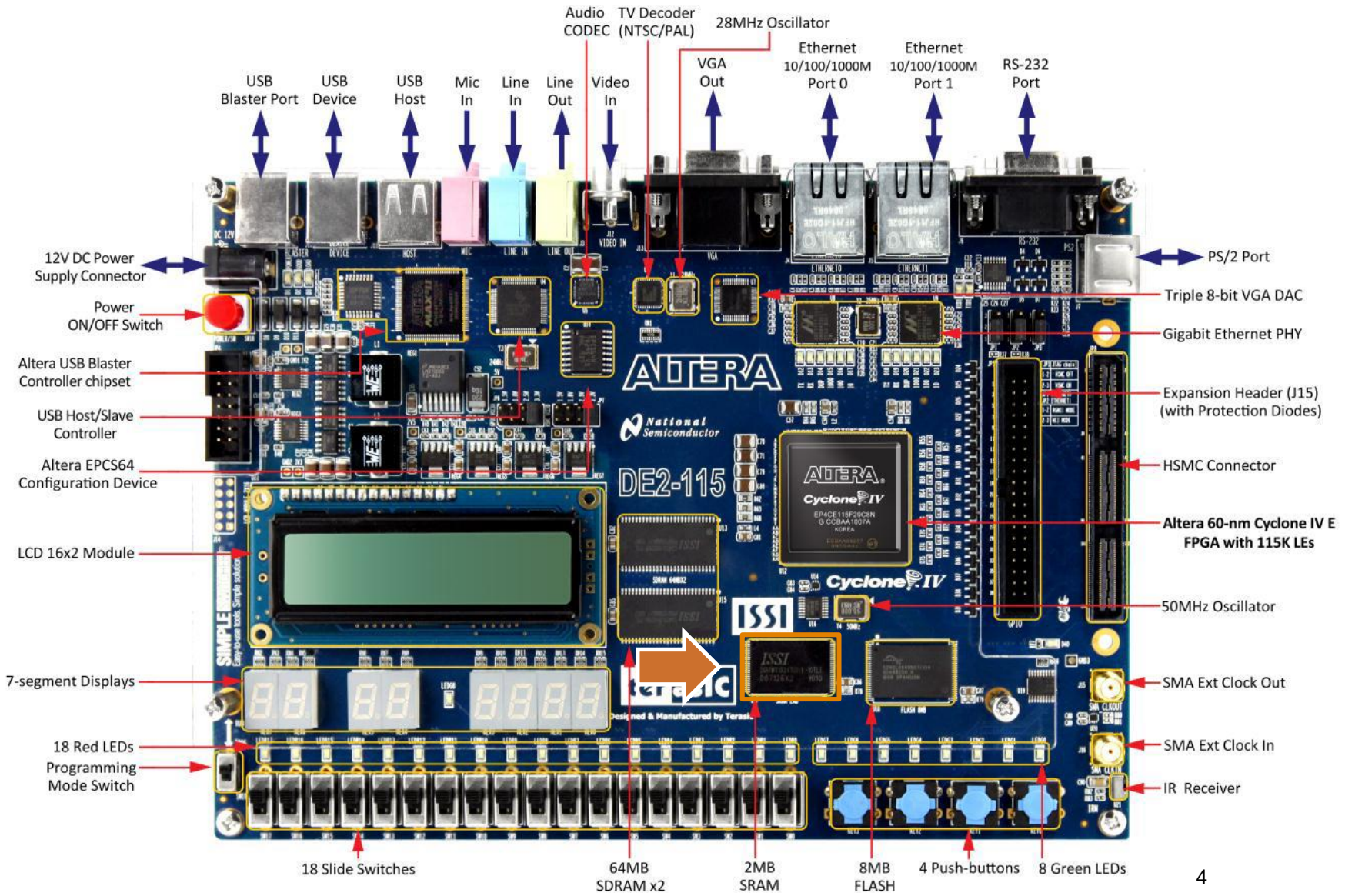
Digital Circuit Lab

TA: Po-Chen Wu

Outline

- SRAM
- SDRAM
- FLASH
- EEPROM
- SD Card

SRAM


Audio CODEC
TV Decoder (NTSC/PAL)
28MHz Oscillator
VGA Out
Ethernet 10/100/1000M Port 0
Ethernet 10/100/1000M Port 1
RS-232 Port
USB Blaster Port
USB Device
USB Host
Mic In
Line In
Line Out
Video In
12V DC Power Supply Connector
Power ON/OFF Switch
Altera USB Blaster Controller chipset
USB Host/Slave Controller
Altera EPCS64 Configuration Device
LCD 16x2 Module
7-segment Displays
18 Red LEDs
Programming Mode Switch
18 Slide Switches
64MB SDRAM x2
2MB SRAM
8MB FLASH
4 Push-buttons
8 Green LEDs
PS/2 Port
Triple 8-bit VGA DAC
Gigabit Ethernet PHY
Expansion Header (J15) (with Protection Diodes)
HSMC Connector
Altera 60-nm Cyclone IV E FPGA with 115K LEs
50MHz Oscillator
SMA Ext Clock Out
SMA Ext Clock In
IR Receiver
ALTERA
DE2-115
Cyclone IV
ISSI

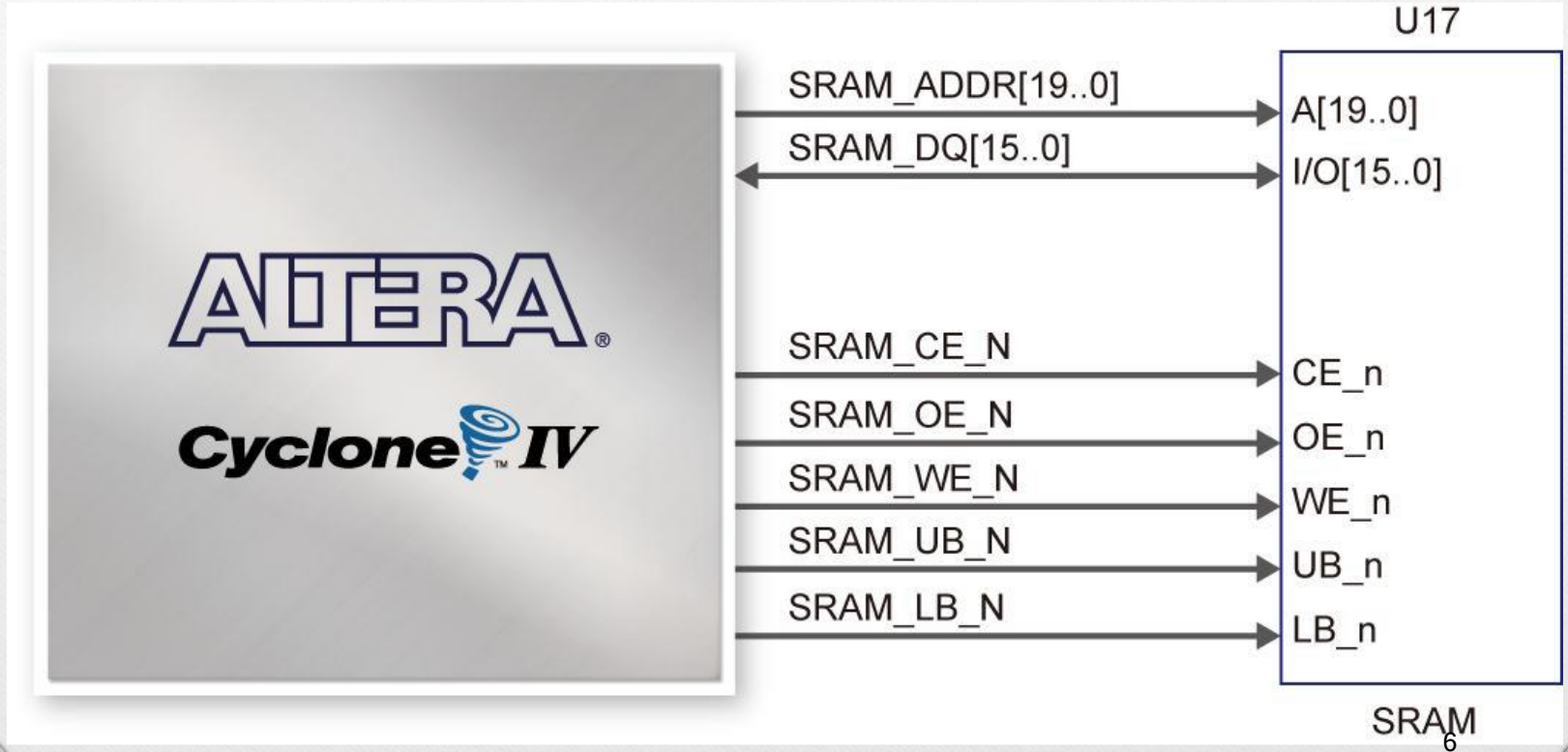
Features

of addresses

- 16M-bit (2MB) static RAMs organized as 1024K words by 16 bits.
- High-speed access times:
  - speed = 20ns for VDD 1.65V to 2.2V
  - speed = 10ns for VDD 2.4V to 3.6V
  - speed = 8ns for VDD 3.3V + 5%

Maximum performance frequency: 125MHz

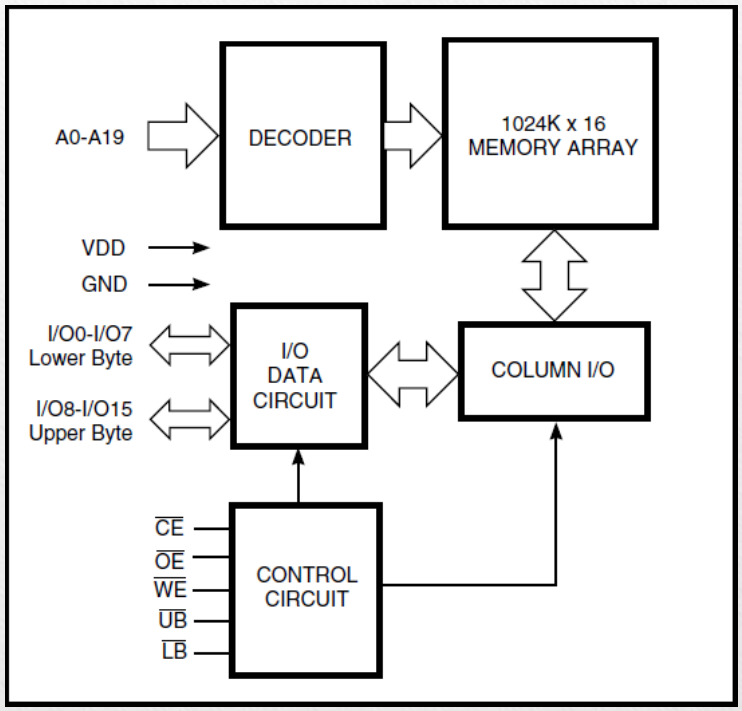
Schematic Diagram



SRAM Pin Assignments

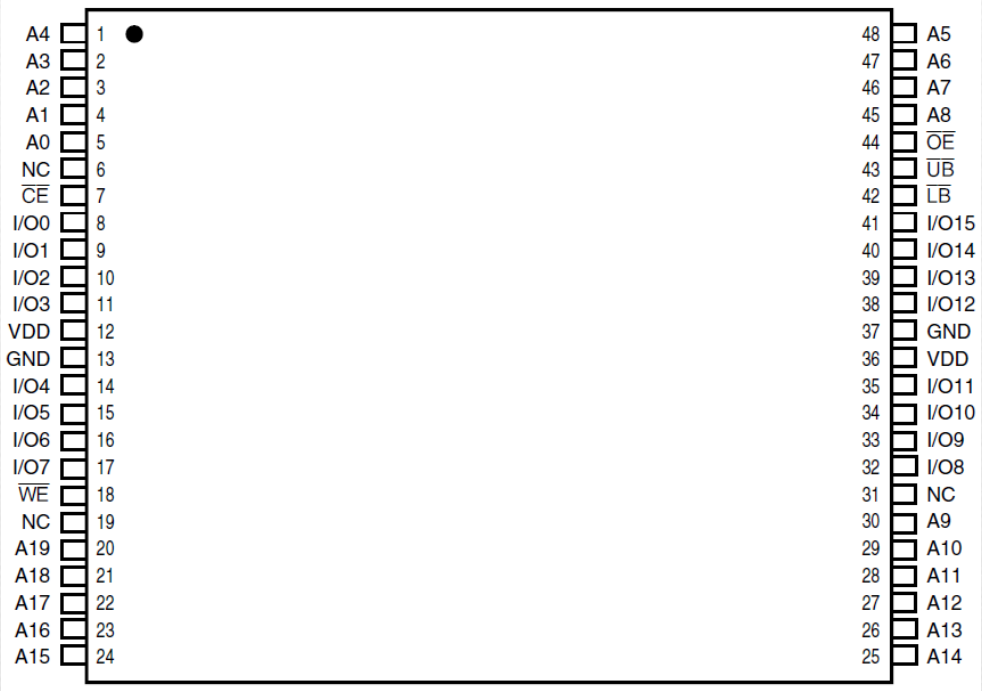
Signal Name	FPGA Pin No.	Description
SRAM_ADDR[0]~	PIN_AB7~	SRAM Address[0]~
SRAM_DQ[0]~	PIN_AH3~	SRAM Data[0]~
SRAM_OE	PIN_AD5	SRAM Output Enable
SRAM_WE	PIN_AE8	SRAM Write Enable
SRAM_CE	PIN_AF8	SRAM Chip Enable
SRAM_LB	PIN_AD4	SRAM Lower Byte Control
SRAM_UB	PIN_AC4	SRAM Upper Byte Control

SRAM Block Diagram



SRAM Pin Configuration

- 48-pin TSOP-1 (12mm x 20mm)

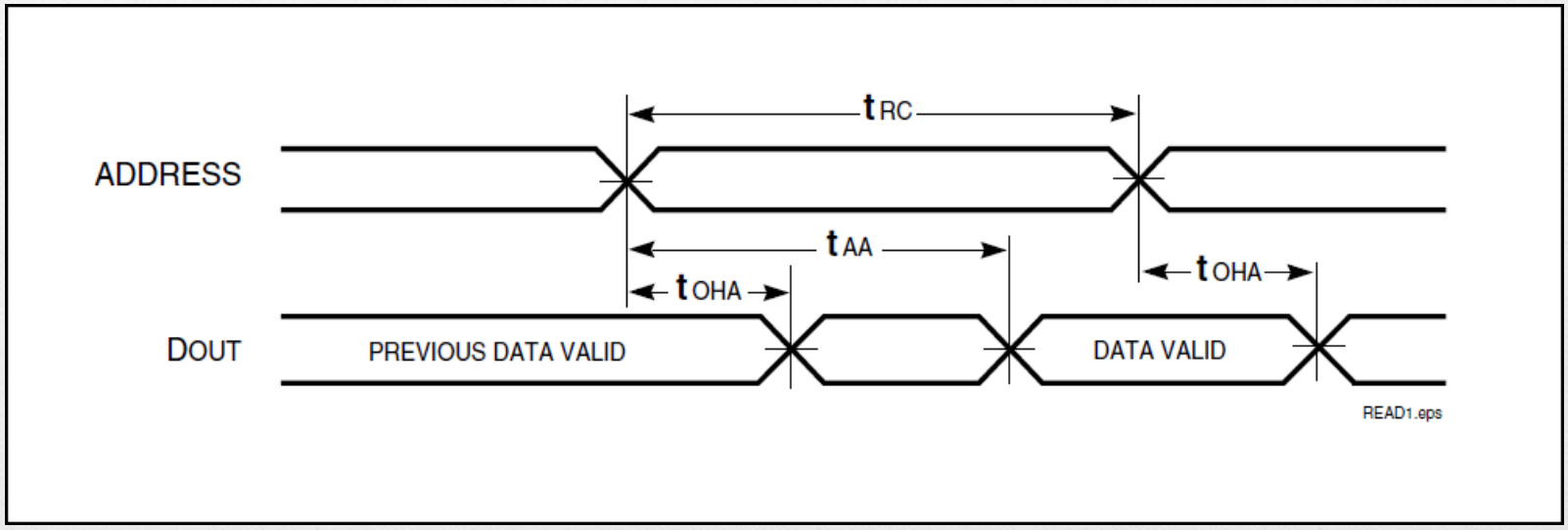


Truth Table

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN I/O0-I/O7	I/O PIN I/O8-I/O15	V_{DD} Current
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I_{CC}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	L	H	L	High-Z	D_{OUT}	
	H	L	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	X	H	L	High-Z	D_{IN}	
	L	L	X	L	L	D_{IN}	D_{IN}	

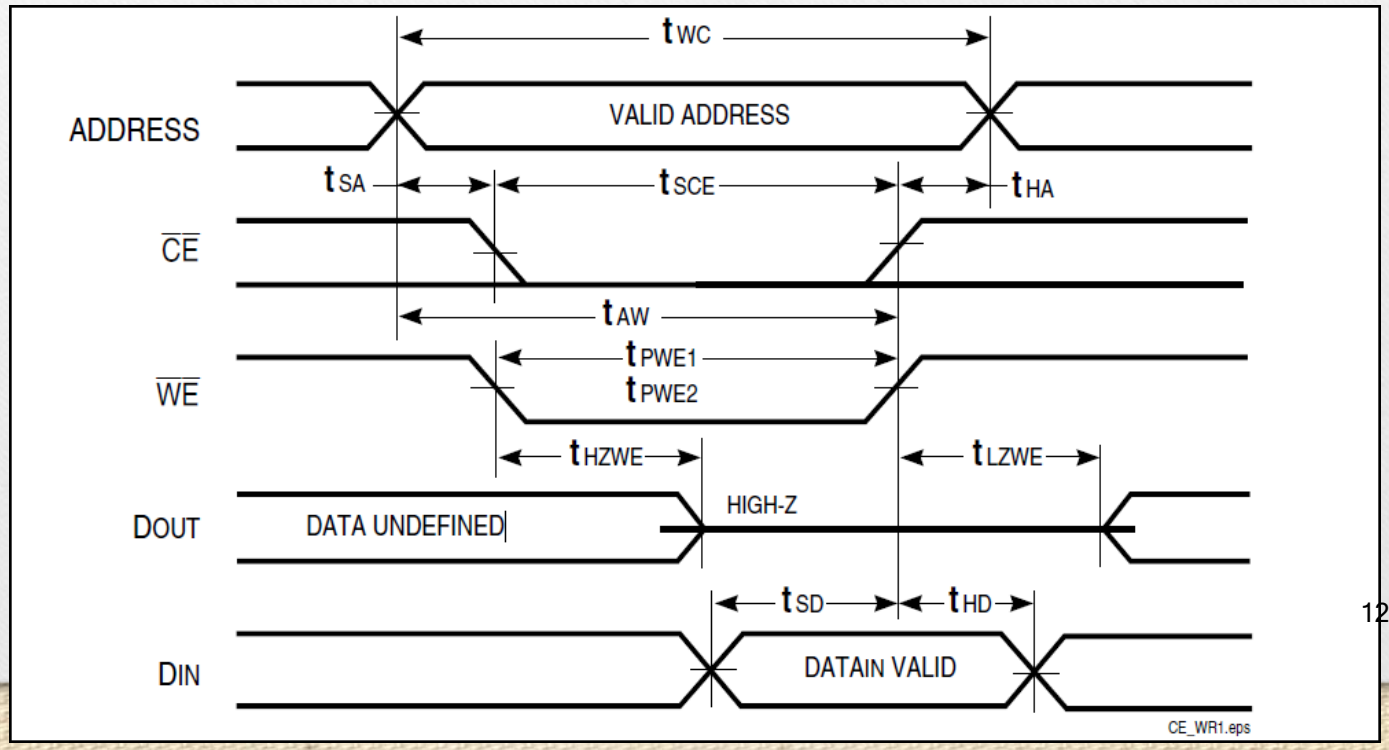
Read Cycle

- Min. read cycle time t_{RC} = 8ns



Write Cycle

- Min. write cycle time t_{WC} = 8ns



The End.

Any question?

Reference

1. "DE2-115 User Manual" by Terasic.
2. "DE2-115_MB.pdf" by Terasic.
3. "61WV102416ALL(ISSI_1M x 16_SRAM).pdf" by ISSI.