My Second FPGA for Altera DE2-115 Board

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Digital Circuit Lab

TA: Po-Chen Wu



Outline

- DE2-115 System Builder
- ModelSim-Altera

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DE2-115 System Builder



Introduction to DE2-115 System Builder (1/2)

- This section describes how users can create a custom design project on the DE2-115 board by using DE2-115 Software Tool DE2-115 System Builder.
- The DE2-115 System Builder is a Windows based software utility, designed to assist users to create a Quartus II project for the DE2-115 board withim minutes.



Introduction to DE2-115 System Builder (2/2)

- The generated Quartus II projects files include:
 - Quartus II Project File (.qpf)
 - Quartus II Setting File (.qsf)
 - Top-Level Design File (.v)
 - Synopsis Design Constraints file (.sdc)
 - Pin Assignment Document (.htm)



General Design Flow





DE2_115_tools\DE2_115_system_builder.exe

Terasic DE2-115 System Builder V 1.0.1			×
		System Configuration Project Name: DE2_115	
DE2-115 FPGA Bo	pard	 ✓ CLOCK ✓ LED x 27 ✓ Button x 4 ✓ PS2 ✓ VGA ✓ SDRAM, 128MB ✓ SRAM, 2MB ✓ Audio ✓ Ethernet 1 ✓ TV Decoder ✓ IR Receiver 	
		GPIO Header IO Voltage: 3.3 V (1 Prefix Name: None HSMC	Default) <u> </u>
Load Setting	Generate	IO Voltage: 2.5 V (I Prefix Name:	Default) 🔽
Save Setting	Exit	None	_

Input Project Name

		System Configuration-	
UNIVERSITY terasic		Project Name:	
PROGRAM WWW.terasic.com		exp2 rsa 1	
DE2-115 FPGA Bo	bard	CLOCK	🖻 RS-232
		LED x 27	🔽 7-Segment x 8
		🖬 🛛 🖻 Button x 4	Switch x 18
		PS2	SD CARD
		VGA	
		SDRAM, 128MB	M FLASH, 8MB
		I SRAM, 2MB	M SMA I≣ NOD
DE2-			M OSB
		Ethernet I	Ethernet 2
			F EA_IU
			EEPROM, JZNU
	151C	GPIO Header	
		IO Voltage: 3.3 V (I	Default) 💽
		Prefix Name	
	11.5V 11.5V 11.5V 11.5V 11.5V 11.5V 11.5V 11.5V 11.5V 11.5V 11.5V		
		None	_
8		HSMC	
1		1 IO Voltage: 2.5 V (I	Default) 🔻
Load Setting	Generate	Dueff Manual	
Save Setting	Exit	None	•



System Configuration

		System Configuration	
NIVERSITY LETASIC		Project Name:	
N U U N M		exp2_rsa	
DE2-115 FPGA Bo	ard	CLOCK	□ RS-232 □ 7-Seament x 8
	W UU UU UU	Button x 4	Switch x 18
		PS2	SD CARD
		U VGA	
		E SBAM 2MB	E FLASH, OMD
DE2.44			
		E Ethernet 1	Ethernet 2
	ial Cyclone IV	TV Decoder	EX_IO
		IR Receiver	EEPROM, 32Kb
988 88 1 8818 teras		GPIO Header	
		IO Voltage: 3.3 V (Default) 💌
<u> </u>		Prefix Name:	
JP6	1.8 1.8 1.8 1.8 1.8 1.8 1.8 1.8	None	•
OV OV O			
			Defently 1
Load Setting	Generate	10 Voltage: 2.5 V (Derault)
		Prefix Name:	
Save Setting	Exit	None	*

GPIO Expansion

		System Configuration-	
UNIVERSITY terasic		Project Name:	
ROGRAM		exp2_rsa	
DE2-115 FPGA Bo	ard	CLOCK	□ RS-232
sala ann a Chailean		LED x 27	□ 7-Segment x 8
		Button x 4	Switch x 18
ان 🏹 زين الكر 🗇			
		E SBAM 2MB	
			□ USB
		Ethernet 1	Ethernet 2
	EB' Cyclone PIV	TV Decoder	EX_IO
		IR Receiver	🗖 EEPROM, 32Kb
988 88 1 8818 tera		GPIO Header	1
		IO Voltage: 3.3 V (Default) 🔹 💼
<u> </u>		Prefix Name:	
	¹⁴¹ 32 52 52 52 52 52 54 52 52 52 52 52 52 52 52 52 52 52 52 52 5	GPIO Default	
C BRO VO		HSMC	
1			Default) 🔻
Load Setting	Generate	10 Voltage. [2.0 V (
		Prefix Name:	
Save Setting	Exit	None	•

HSMC Expansion

		System Configuration-	
INIVERSITY terasic		Project Name:	
ROGRAM		exp2_rsa	
DE2-115 FPGA Bo	bard		□ RS-232
	ann ann a Cho	E LED x 27	7-Segment x 8
×,,,,,,,	W W W	📓 🛛 🗆 Button x 4	🗆 Switch x 18
		PS2	SD CARD
		🗧 🗆 🗆 🗆 🗖	E LCD
	ERA	SDRAM, 128MB	🗖 FLASH, 8MB
		SRAM, 2MB	🗆 SMA
DE2-	115 🛃 🧰 💐 🗐 👘	📕 🗆 Audio	🗆 USB
		Ethernet 1	Ethernet 2
		TV Decoder	E EX_IO
		IR Receiver	EEPROM, 32Kb
288 88 1 8818 tera		GPIO Header	
		IO ∨oltage: 3.3 V (Default) 🔽 📷 📊
<u> </u>	<u>hhhh an an an an a</u>	Drefix Name:	
	1.5V 1.5V 1.5V 1.5V 1.5V 1.5V 1.5V 1.3V 2.5V 2.5V 2.5V 2.5V		
		GPIO Delault	
		HSMC	1
Logid Catting	Oursets	1 IO Voltage: 2.5 V (Default) 🚽
Load Setting	Generale	Prefix Name	
1			

Project Setting Management

Terasic DE2-115 System Builder V 1.0.1			×
	ſ	System Configuration Project Name: exp2_rsa	
DE2-115 FPGA Bo	e the current b	CLOCK LED x 27 Button x 4 PS2 VGA SDRAM, 128MB SRAM, 2MB	 RS-232 7-Segment x 8 Switch x 18 SD CARD LCD FLASH, 8MB SMA USB hernet 2 LO PROM, 32Kb
	DEZ-115 Syste		
		Prefix Name: GPIO Default	
Load Setting	2 Generate	IO Voltage: 2.5 V (I Prefix Name:	Default) 🔹
Save Setting	Exit	HTG - HSMC to PIO	Adaptor -

Project Generation

 When users press the Generation buttion, the DE2-115 System Builder will generate the corresponding Quartus II files and documents.

No.	Filename	Description
1	exp2_rsa.v	Top level verilog HDL file for Quartus II
2	exp2_rsa.qpf	Quartus II Project File
3	exp2_rsa.qsf	Quartus II Setting File
4	exp2_rsa.sdc	Synopsis Design Constraints file for Quartus II
5	exp2_rsa.ht m	Pin Assignment Document

THDB-HTG Board

 This figure illustrates how the THDB-HTG board is connected to the DE2-115 board.



Be sure to turn off the power whenever you connect or disconnect the THDB-HTG board!!

exp2_rsa.htm (1/2)

	🕒 exp2_rsa.ht	tm	×			□
ſ	← ⇒ C ²	n 🗋 file:	///C:/Users	/Trumen/Deskt	op/exp2_rsa/exp2_	<u>∽</u> =
ľ		GPI	O connect	to GPIO Defau	lt	
	Name	Location	Direction	Standard	GPIO Pin Index	
	GPIO[0]	AB22	inout	3.3-V LVTTL	1	
	GPIO[1]	AC15	inout	3.3-V LVTTL	2	
	GPIO[2]	AB21	inout	3.3-V LVTTL	3	
	GPIO[3]	Y17	inout	3.3-V LVTTL	4	
	GPIO[4]	AC21	inout	3.3-V LVTTL	5	
	GPIO[5]	Y16	inout	3.3-V LVTTL	6	
	GPIO[6]	AD21	inout	3.3-V LVTTL	7	
	GPIO[7]	AE16	inout	3.3-V LVTTL	8	
	GPIO[8]	AD15	inout	3.3-V LVTTL	9	
	GPIO[9]	AE15	inout	3.3-V LVTTL	10	
	GPIO[10]	AC19	inout	3.3-V LVTTL	13	
	GPIO[11]	AF16	inout	3.3-V LVTTL	14	
	GPIO[12]	AD19	inout	3.3-V LVTTL	15	
	GPIO[13]	AF15	inout	3.3-V LVTTL	16	
	GPIO[14]	AF24	inout	3.3-V LVTTL	17	
	GPIO[15]	AE21	inout	3.3-V LVTTL	18	
	GPIO[16]	AF25	inout	3.3-V LVTTL	19	
	GPIO[17]	AC22	inout	3.3-V LVTTL	20	
	IICDIO[10]	LATOO	17 4	10 0 17 T 17 T T 1	10.1	

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DE2_115_User_manual.pdf 4.8 Usiing the Expansiion Header



exp2_rsa.htm (2/2)

HSMC CLKINn2 HSMC_CLKINp2

HSMC_CLKOUTn2

HSMC_CLKOUTp2



I2C Serial EEPROM(U1)

16

THDB-HTG_V1.0.3.pdf 1-6 Expansion Prototype Connectors

	J2			J3			J4	
HSMC_CLKINn2	0 1 2 0	HSMC_RX_n16	HSMC_CLKINn1		HSMC_RX_n7	ND		ND
HSMC_CLKINp2	0340	HSMC_RX_p16	HSMC_CLKINp1	0340	HSMC_RX_p7	HSMC_TXVR_TXn0	○ 3 4 ○	HSMC_TXVR_RXn0
HSMC_TX_n16	0 5 6 0	HSMC_RX_n15	HSMC_TX_n7	0560	HSMC_RX_n6	HSMC_TXVR_TXp0	0560	HSMC_TXVR_RXP0
HSMC_TX_p16	0780	HSMC_RX_p15	HSMC_TX_p7	0780	HSMC_RX_p6	ND	0780	ND
HSMC_TX_n15	0 9 10	HSMC_RX_n14	HSMC_TX_n6	0 9 10 0	HSMC_RX_n5	HSMC_TXVR_TXn1	○ 9 10 ○	HSMC_TXVR_RXn1
5V	● 11 12 €	GND	5V	11 12	- GND	5∨	11 12	GND
HSMC_TX_15	0 13 14 0	HSMC_RX_p14	HSMC_TX_p6	0 13 14 0	— HSMC_RX_p5	HSMC_TXVR_TXp1	0 13 14 0	HSMC_TXVR_RXp1
HSMC_TX_n14	0 15 16 0	HSMC_RX_n13	HSMC_TX_n5	0 15 16 0	HSMC_RX_n4	ND	0 15 16 0	ND
HSMC_TX_014	0 17 18	HSMC_RX_p13	HSMC_TX_p5	0 17 180	HSMC_RX_p4	HSMC_TXVR_TXn2	0 17 180	HSMC_TXVR_RXn2
MC_CLKOUTn2	°⊖1920⊂	HSMC_RX_n12	HSMC_CLKOUTn1	° 🔿 19 20 🔿	HSMC_RX_n3	HSMC_TXVR_TXp2	0 19 20 0	HSMC_TXVR_RXp2
MC_CLKOUTp2	0 21 22 0	HSMC_RX_p12	HSMC_CLKOUTp1	0 21 22 0	HSMC_RX_p3	ND	21 22	ND
HSMC_TX_n13	0 23 24 🤇	HSMC_RX_n11	HSMC_TX_n4	23 24	HSMC_RX_n2	HSMC_TXVR_TXn3	23 24	HSMC_TXVR_RXn3
HSMC_TX_p13	25 26	HSMC_RX_011	HSMC_TX_p4	0 25 260	HSMC_RX_p2	HSMC_TXVR_TXp3	25 26	HSMC_TXVR_RXp3
HSMC_TX_n12	0 27 280	HSMC_RX_n10	HSMC_TX_n3	0 27 280	HSMC_RX_n1	ND	27 28	ND
3.3V	29 30	GND	3.3V	29 30	GND	3,3V	29 30	GND
HSMC_TX_p12	○ 31 32 ○	HSMC_RX_p10	HSMC_TX_p3	31 32	HSMC_RX_p1	HSMC_TXVR_TXn4	31 32	HSMC_TXVR_RXn4
HSMC_TX_n11	◯ 33 34◯	HSMC_RX_n9	HSMC_TX_n2	○ 33 34○	HSMC_RX_n0	HSMC_TXVR_TXp4	○ 33 34○	HSMC_TXVR_RXn5
HSMC_TX_p11	◯ 35 36◯	HSMC_RX_p9	HSMC_TX_p2	○ 35 36○	HSMC_RX_p0	ND	○ 35 36○	HSMC_TXVR_RXp5
HSMC_TX_n10	○ 37 38 ○	HSMC_TX_n9	HSMC_TX_n1	37 38	HSMC_TX_n0	HSMC_TXVR_TXn5	37 38	HSMC_TXVR_RXp4
HSMC_TX_p10	○ 39 40 ◯	HSMC_TX_p9	HSMC_TX_p1	39 40	HSMC_TX_p0	HSMC_TXVR_TXp5	○ 39 40 ○	ND
							ND : Not Defined	

HSMC connec	t to HTG -	· HSMC to	PIO Adap	tor	^
Name	Location	Direction	Standard	HSMC Pin Index	
HSMC_CLKOUT_0	AD28	output	2.5 V	39	
HSMC_CLKIN_0	AH15	input	2.5 V	40	
HSMC_D[0]	AE26	inout	2.5 V	41	
HSMC_D[1]	AE28	inout	2.5 V	42	
HSMC_D[2]	AE27	inout	2.5 V	43	
HSMC_D[3]	AF27	inout	2.5 V	44	
HSMC_TX_p[0]	D27	inout	2.5 V	47	
HSMC_RX_p[0]	F24	inout	2.5 V	48	
HSMC_TX_n[0]	D28	inout	2.5 V	49	Ε
HSMC_RX_n[0]	F25	inout	2.5 V	50	
HSMC_TX_p[1]	E27	inout	2.5 V	53	
HSMC_RX_p[1]	D26	inout	2.5 V	54	
HSMC_TX_n[1]	E28	inout	2.5 V	55	
HSMC_RX_n[1]	C27	inout	2.5 V	56	
HSMC_TX_p[2]	F27	inout	2.5 V	59	
HSMC_RX_p[2]	F26	inout	2.5 V	60	
HSMC_TX_n[2]	F28	inout	2.5 V	61	
HSMC RX n[2]	E26	inout	2.5 V	62	

- 0 **X**

← → C ☆ file:///C:/Users/Trumen/Desktop/exp2_rsa/exp2_☆ Ξ

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🗋 exp2_rsa.htm

exp2_rsa.sdc

- Remember to modify the .sdc file.
 - clock, i/o delay, etc.

exp2	_rsa.sdc	
1	#*******	******
2	# This .sdc file is created by Te	erasic Tool.
3	# Users are recommended to modify	y this file to match users]
4	#****	******
5		
6	#*****	******
7	# Create Clock	
8	#*******	create clock -period 1000 [get ports clk]
9		derive clock uncertainty
10	#*****	act input delay Quele els els fell inputel
11	# Create Generated Clock	set_input_delay 0 -clock cik [all_inputs]
12	#*****	set_output_delay 0 -clock clk [all_outputs]
13	derive_pll_clocks	
14		
15		
16		
17	#*******	******
18	# Set Clock Latency	17

Can't place multiple pins...?

 If you try to assign pins by yourself, this error message may occur.

😵 176310 Can't place multiple pins assigned to pin location Pin_P28 (IOPAD_X115_Y43_N7)

• How to fix it?



	Abagamenta Processing Tools		Search altera.com	,
🗋 💕 🖬 🗿 🐰 🖻	Pevice	2	🛛 🖓 🕜 🏈 🦃 🖉 👂	»
🚥 🕨 🏹 🍢 🤣	🥜 Settings	Ctrl+Shift+E		
roject Navigator	TimeQuest Timing Analyzer Wi	zard	🛛 🔶 exp2_rsa.v 🗵	
	Intersection Assignment Editor	Ctrl+Shift+A	Flow Summary	
Cyclone IV E: EP4CE115F2	💝 Pin Planner	Ctrl+Shift+N	Quartus II 64-Bit Versi	or
P and a set of the	Remove Assignments		Revision Name	
101 101 101	Back-Annotate Assignments		Top-level Entity Name	
	Import Assignments		Device	
	Export Assignments		Timing Models	
	Assignment Groups		Total combinationa	al t
Merarchy E Files	LogicLock Regions Window	Alt+L	Dedicated logic reg	gis
asks	Design Partitions Window	Alt+D	Total pins	
ow: Compilation	Customize		Total virtual pins	
	Task 🔺		Total memory bits Embedded Multiplier 9-	bi
🕻 🔹 🕨 Compile Design	E		Total PLLs	
Analysis &	Synthesis			
	< <search>></search>	~		
		•		
▶ 🕄 176310 Can't	age t place multiple pins a	assigned to pin	location Pin P28 (IOPAD	
g 🕺 171000 Can't	t fit design in device			
			4	10

🔮 Device

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Select the family and device you want to target for compilation. You can install additional device support with the Install Devices command on the Tools menu.

Device family	Show in 'Availa	ble devices' list
Family: Cyclone IV E	Package:	Any 🔻
Devices: All 🔹	Pin count:	Any 🔻
Target device	Speed grade:	Any
Auto device selected by the Fitter	Name filter:	
 Specific device selected in 'Available devices' list 	Show adva	anced devices HardCopy compatible only
Other: n/a	Device and Pin (Options

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements	*
EP4CE75F29I7	1.2V	75408	427	2810880	400	
EP4CE75F29I8L	1.0V	75408	427	2810880	400	
EP4CE75U19I7	1.2V	75408	293	2810880	400	
EP4CE115F23C7	1.2V	114480	281	3981312	532	
EP4CE115F23C8	1.2V	114480	281	3981312	532	
EP4CE115F23C8L	1.0V	114480	281	3981312	532	
EP4CE115F23C9L	1.0V	114480	281	3981312	532	
EP4CE115F23I7	1.2V	114480	281	3981312	532	
EP4CE115F23I8L	1.0V	114480	281	3981312	532	
EP4CE115F29C7	1.2V	114480	529	3981312	532	
ED40E11EE0000	1.01/	11///00	500	2001212	E27	
•			111		•	

Migration compatibility

Migration Devices...

Companion device HardCopy:

✓ Limit DSP & RAM to HardCopy device resources

0 migration devices selected

OK

Cancel



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Oevice and Pin Options - exp2_rsa

Category:

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General
Configuration
Programming Files
Unused Pins
Dual-Purpose Pins
Capacitive Loading
Board Trace Model
I/O Timing
Voltage
Pin Placement
Error Detection CRC
CvP Settings
Partial Reconfiguration

Dual-Purpose Pins

Specify how dual-purpose pins should be used after device configuration is complete. The default settings for each pin depend on the current configuration scheme selected in the Configuration tab, which is: Active Serial

Note: For HardCopy, these settings apply to the FPGA prototype device.

Dual-purpose pins:

Name	Value
DCLK	Use as programming pin
Data[0]	As input tri-stated
Data[1]/ASDO	As input tri-stated
Data[72]	Use as regular I/O
FLASH_nCE/nCSO	As input tri-stated
Other Active Parallel pins	Use as regular I/O
nCEO	Use as regular I/O

Description:

Specifies how the nCEO pin should be used when the device is operating in user mode after configuration is complete. The nCEO pin can be reserved as dedicated nCEO programming pin or a regular I/O pin.

3

OK

Reset

Cancel

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Help

X

🔮 Device

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Select the family and device you want to target for compilation. You can install additional device support with the Install Devices command on the Tools menu.

Device family	She	Show in 'Available devices' list				
Family: Cyclone IV E	Pa	ckage: count:	Any			
Target device	Sp	eed grade:	Any 🔻			
Auto device selected by the Fitter	Na	me filter:				
 Specific device selected in 'Available devices' list 	V	Show adva	nced devices HardCopy compatible only			
◯ Other: n/a	Dev	ice and Pin C	Options			

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements	*
EP4CE75F29I7	1.2V	75408	427	2810880	400	
EP4CE75F29I8L	1.0V	75408	427	2810880	400	
EP4CE75U19I7	1.2V	75408	293	2810880	400	
EP4CE115F23C7	1.2V	114480	281	3981312	532	
EP4CE115F23C8	1.2V	114480	281	3981312	532	
EP4CE115F23C8L	1.0V	114480	281	3981312	532	
EP4CE115F23C9L	1.0V	114480	281	3981312	532	
EP4CE115F23I7	1.2V	114480	281	3981312	532	
EP4CE115F23I8L	1.0V	114480	281	3981312	532	
EP4CE115F29C7	1.2V	114480	529	3981312	532	-
ED40E11EE0000	1.51/	11///00	500	0001010	600	Ψ.
•					•	

Migration compatibility

Migration Devices...

0 migration devices selected

Companion device HardCopy:

✓ Limit DSP & RAM to HardCopy device resources

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Help



Introduction to ModelSim (1/5)

- ModelSim is a simulation and verification tool for VHDL, Verilog, SystemVerilog, and mixed language designs.
- The following diagram shows the basic steps for simulating a design in ModelSim.





Introduction to ModelSim (2/5)

- Creating the Working Library
 - In ModelSim, all designs are compiled into a library.
 - You typically start a new simulation in ModelSim by creating a working library called "work," which is the default library name used by the compiler as the default destination for compiled design units.



Introduction to ModelSim (3/5)

- Compiling Your Design
 - After creating the working library, you compile your design units into it.
 - The ModelSim library format is compatible across all supported platforms.
 - You can simulate your design on any platform without having to recompile your design.



Introduction to ModelSim (4/5)

- Loading the Simulator with Your Design and Running the Simulation
 - With the design compiled, you load the simulator with your design by invoking the simulator on a top-level module (Verilog) or a configuration or entity/architecture pair (VHDL).



Introduction to ModelSim (5/5)

Debugging Your Results

 If you don't get the results you expect, you can use ModelSim's robust debugging environment to track down the cause of the problem.



ModelSim-Altera

- Altera Quartus II software allows the user to launch Modelsim-Altera simulator from within the software using the Quartus II feature called NativeLink.
- It facilitates the process of simulation by providing an easy to use mechanism and precompiled libraries for simulation.



Setting up EDA Tool Options



🔮 Options

Category:

1

▲ General

▲ Messages Colors Fonts

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General	EDA Tool Options	
EDA Tool Options Fonts	Specify the location of	of the tool executable for each third-party EDA tool:
Headers & Footers Settings	EDA Tool	Location of Executable
Notifications	Precision Synthesis	
Libraries	Synplify	
Preferred Text Editor	Synplify Pro	
Processing	Active-HDL	
Tooltip Settings Messages	Riviera-PRO	
Colors	ModelSim	
Fonts	QuestaSim	Z
	ModelSim-Altera	C:\altera\13.1\modelsim_ase\win32aloem\
	Use NativeLink w	ith a Synplify/Synplify Pro node-locked license
		3 OK Cancel Help

X

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Setting Up the Simulation



✓ Settings - exp2 rsa

Settings - exp2_rsa		x
Category:	Device	
General	Simulation	
Files Libraries Operating Settings and Conditions Voltage Temperature Compilation Process Settings Early Timing Estimate Incremental Compilation	Specify options for generating output files for use with other EDA tools. Tool name: ModelSim-Altera 2 Run gate-level simulation automatically after compilation EDA Netlist Writer settings	_
Physical Synthesis Optimizations	Format for output netlist: Verilog HDL 3 Time scale: 1 ps Output directory: simulation/modelsim Map illegal HDL characters Enable glitch filtering Options for Power Estimation	
VHDL Input Verilog HDL Input Default Parameters Fitter Settings TimeQuest Timing Analyzer Assembler Design Assistant SignalTap II Logic Analyzer Logic Analyzer Interface PowerPlay Power Analyzer Settings SSN Analyzer	Generate Value Change Dump (VCD) file script Script Settings Design instance name:	
	 Script to compile test bench: More NativeLink Settings Reset 	
	33	
	OK Cancel Apply Help	



Settings - exp2_rsa

Category:	Device
General Files Libraries	Simulation Specify options for generating output files for use with other EDA tools.
 Operating Settings and Conditions Voltage Tomporative 	Tool name: ModelSim-Altera
Compilation Process Settings Early Timing Estimate	Run gate-level simulation automatically after compilation
Incremental Compilation Physical Synthesis Optimizations DA Tool Settings	Format for output netlist: Verilog HDL Time scale: 1 ps
Design Entry/Synthesis Simulation	Output directory: simulation/modelsim
Formal Verification Board-Level Analysis & Synthesis Settings VHDL Input Verilog HDL Input Default Parameters Fitter Settings	Options for Power Estimation Generate Value Change Dump (VCD) file script Script Settings Design instance name:
TimeQuest Timing Analyzer Assembler Design Assistant	More EDA Netlist Writer Settings
Logic Analyzer Interface PowerPlay Power Analyzer Settings	
SSN Analyzer	Use script to set up simulation:
	⊘ Script to compile test bench:
	More NativeLink Settings Reset
	35
	OK Cancel Apply Help

Before Simulation...

- We should compile our design before simulation to generate a simulation snapshot.
- "Start Analysis & Elaboration" is enough, and it takes much less time than "Start Compilation".
- And then we can run the simulation.



Issues of Working Directory

 The working directory of ModelSim-Altera is under "(project directory)/simulation/modelsim", so be careful of setting the directory of input data in the testbench.

```
initial $readmemh("../../dat/dn.dat", dn_mem);
initial $readmemh("../../dat/c.dat", c_mem);
initial $readmemh("../../dat/m.dat", m_mem);
```



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If There are Something Wrong...

 Your simulation takes a long time and seems it will not stop.

#
#
Error!!! Somethings' wrong with your code ...!!
#
#
-----FAIL-----FAIL-----#
#
** Note: \$finish : C:/Users/Trumen/Desktop/exp2_rsa/testbench.v(184)
Time: 1 sec Iteration: 0 Instance: /testbench

The calculated result is incorrect.

# # : #	ERR	OR at		Oth m[7:	0]:	output	00000051	!=expect	50
# # #	**	Note: Time:	\$finish 49635 ms	: C:/Users/ Iteration: 0	Trumen/Desk Instance:	top/exp /test	p2_rsa/t bench	testbench	.v(162)	



If the Input Date are not Found...

```
# run -all
# ** Warning: (vsim-7) Failed to open readmem file "./dat/dn.dat" in read mode.
# No such file or directory. (errno = ENOENT) : E:/DCLab/102 2/MyExp/Exp2/exp2 rsa/testbench.v(38)
    Time: 0 ps Iteration: 0 Instance: /testbench
# ** Warning: (vsim-7) Failed to open readmem file "./dat/c.dat" in read mode.
# No such file or directory. (errno = ENOENT) : E:/DCLab/102 2/MyExp/Exp2/exp2 rsa/testbench.v(39)
    Time: 0 ps Iteration: 0 Instance: /testbench
# ** Warning: (vsim-7) Failed to open readmem file "./dat/m.dat" in read mode.
                                            : E:/DCLab/102 2/MyExp/Exp2/exp2 rsa/testbench.v(40)
# No such file or directory. (errno = ENOENT)
    Time: 0 ps Iteration: 0 Instance: /testbench
# Congratulations! All data have been generated successfully!
                                                      It is a fake "PASS"...
    -----PASS------
# ** Note: $finish : E:/DCLab/102 2/MyExp/Exp2/exp2 rsa/testbench.v(175)
  Time: 200927 us Iteration: 1 Instance: /testbench
```



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Reference

- 1. "DE2-115 User manual" by Terasic.
- 2. "THDB-HTG User Manual" by Terasic.
- 3. ModelSim® Tutorial by Mentor Graphics Corporation.
- 4. "Getting Started with Quartus II Simulation Using the ModelSim-Altera Software User Guide" by Altera.

