My Second FPGA for Altera DE2-115 Board

Digital Circuit Lab

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Outline

- DE2-115 System Builder
- ModelSim-Altera

DE2-115 System Builder

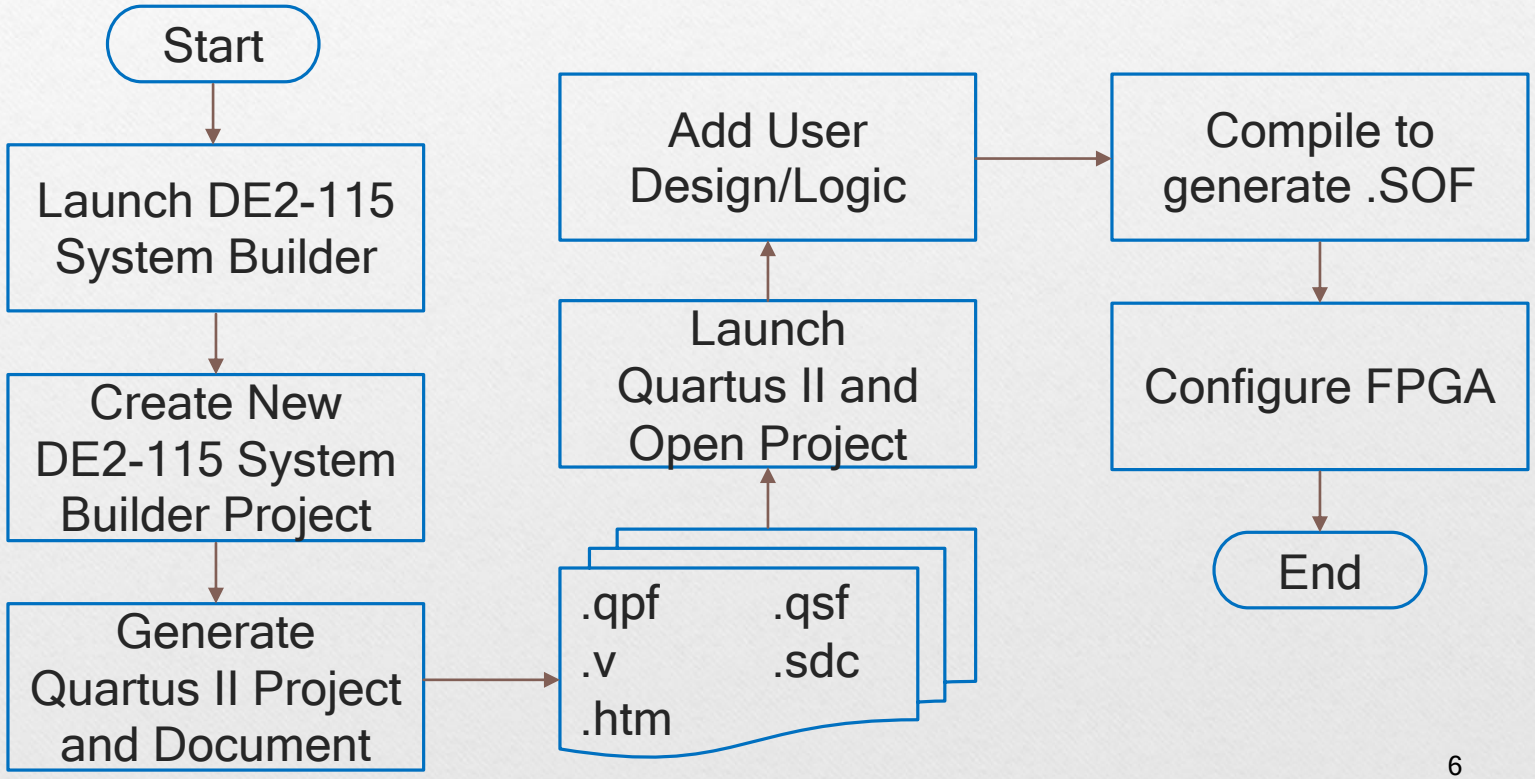
Introduction to DE2-115 System Builder (1/2)

- This section describes how users can create a custom design project on the DE2-115 board by using DE2-115 Software Tool DE2-115 System Builder.
- The DE2-115 System Builder is a Windows based software utility, designed to assist users to create a Quartus II project for the DE2-115 board withim minutes.

Introduction to DE2-115 System Builder (2/2)

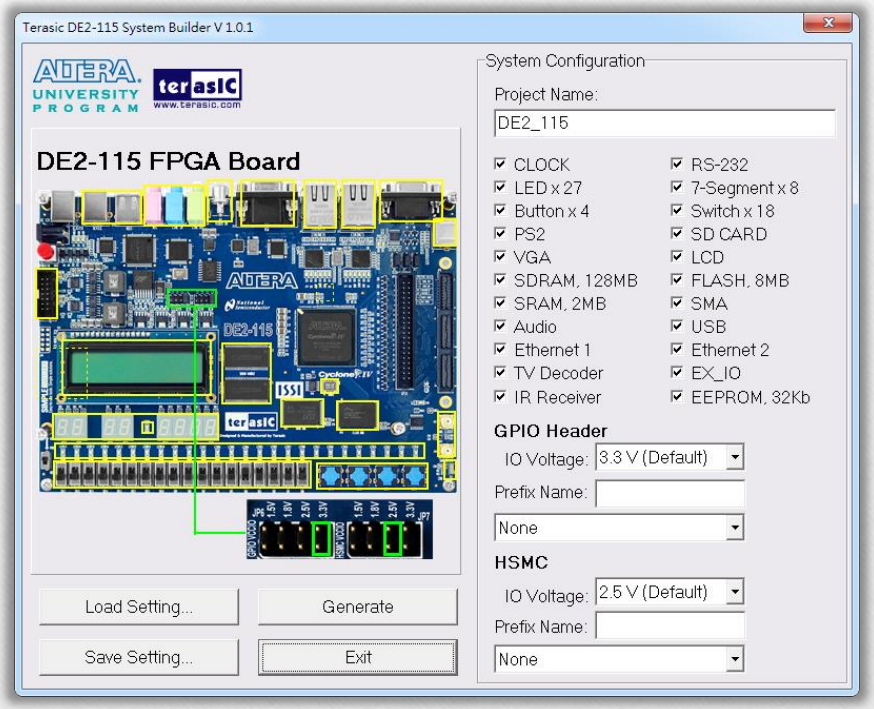
- The generated Quartus II projects files include:
  - Quartus II Project File (.qpf)
  - Quartus II Setting File (.qsf)
  - Top-Level Design File (.v)
  - Synopsis Design Constraints file (.sdc)
  - Pin Assignment Document (.htm)

General Design Flow

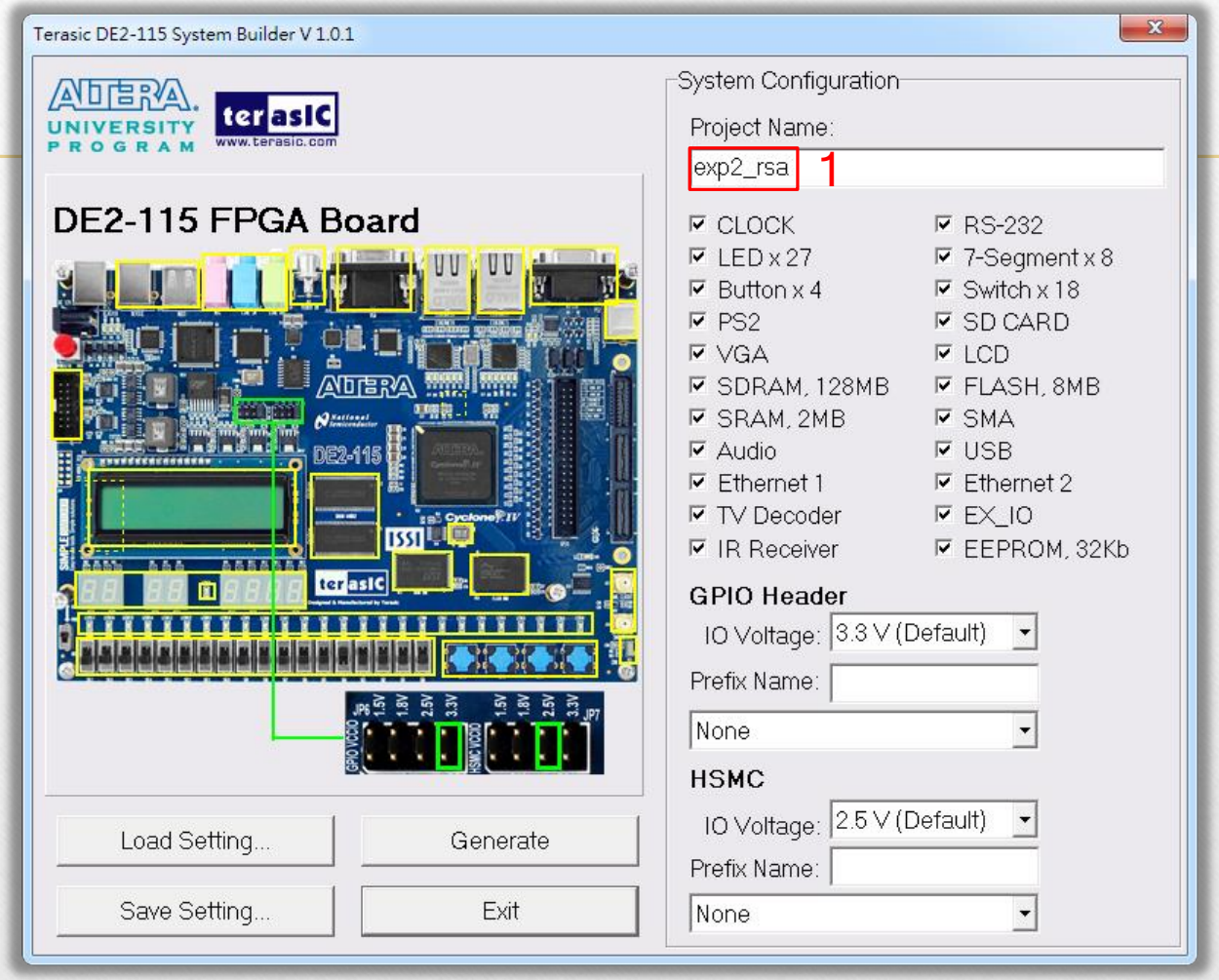


Launch DE2-115 System Builder

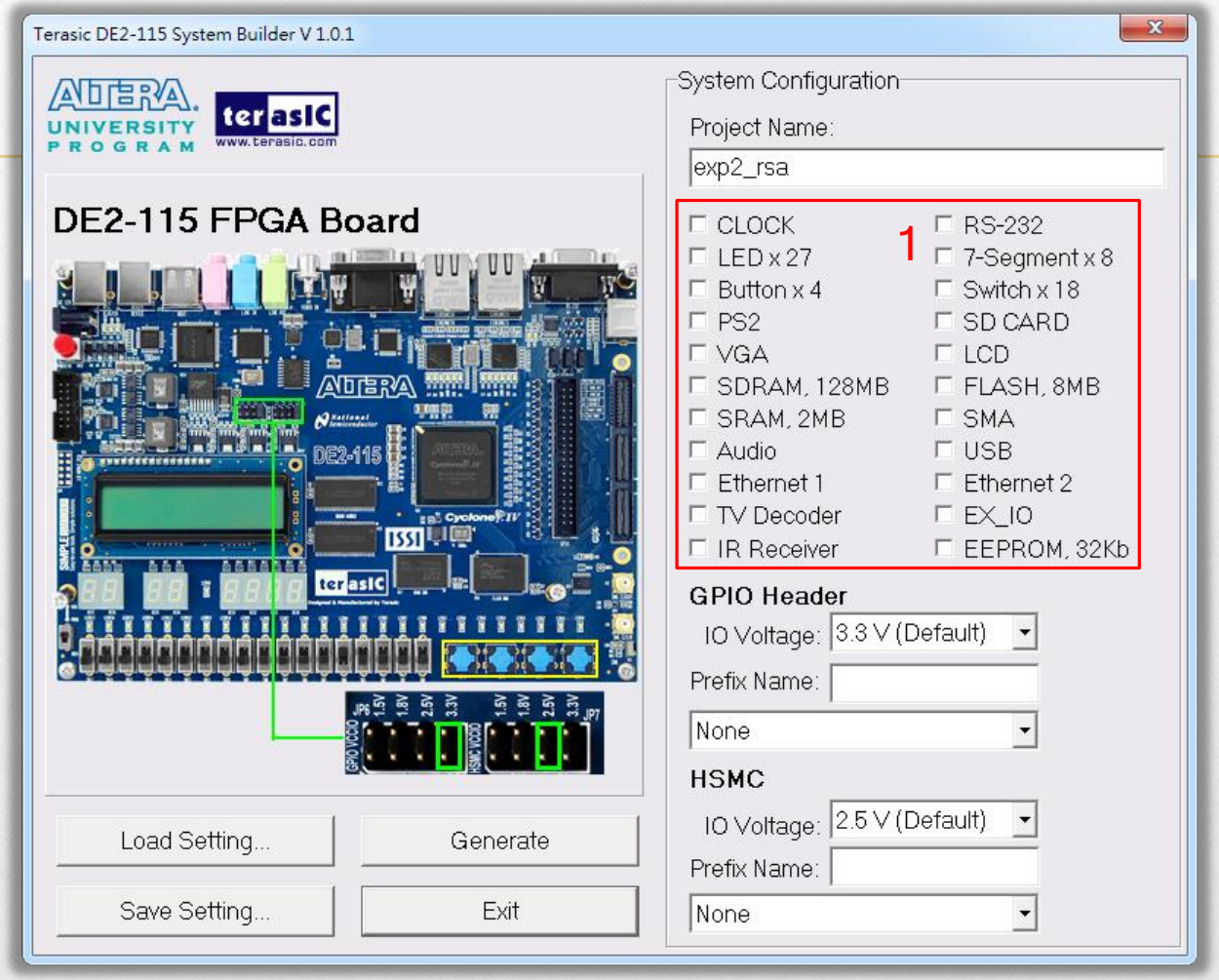
- DE2_115_tools\DE2_115_system_builder.exe



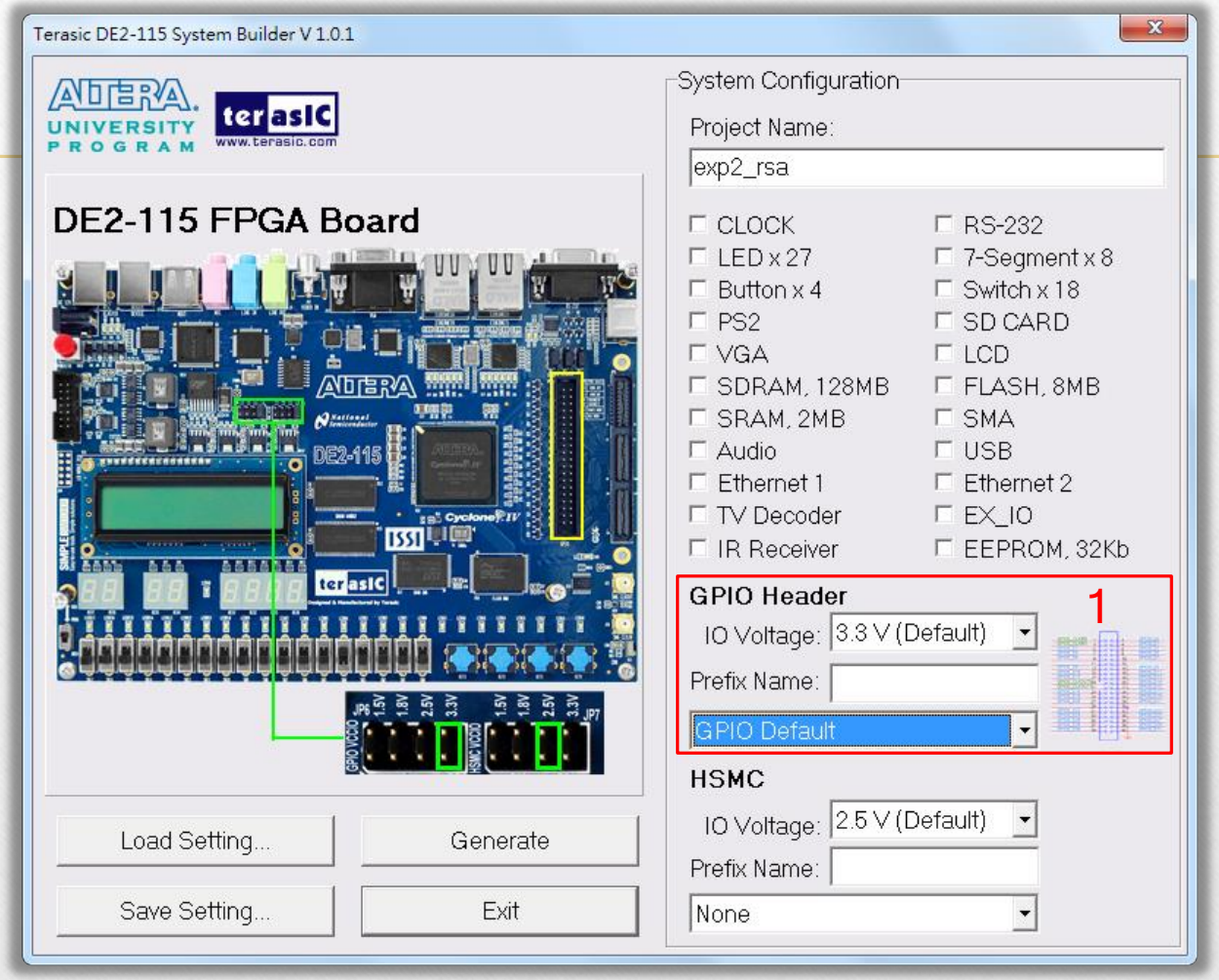
Input Project Name



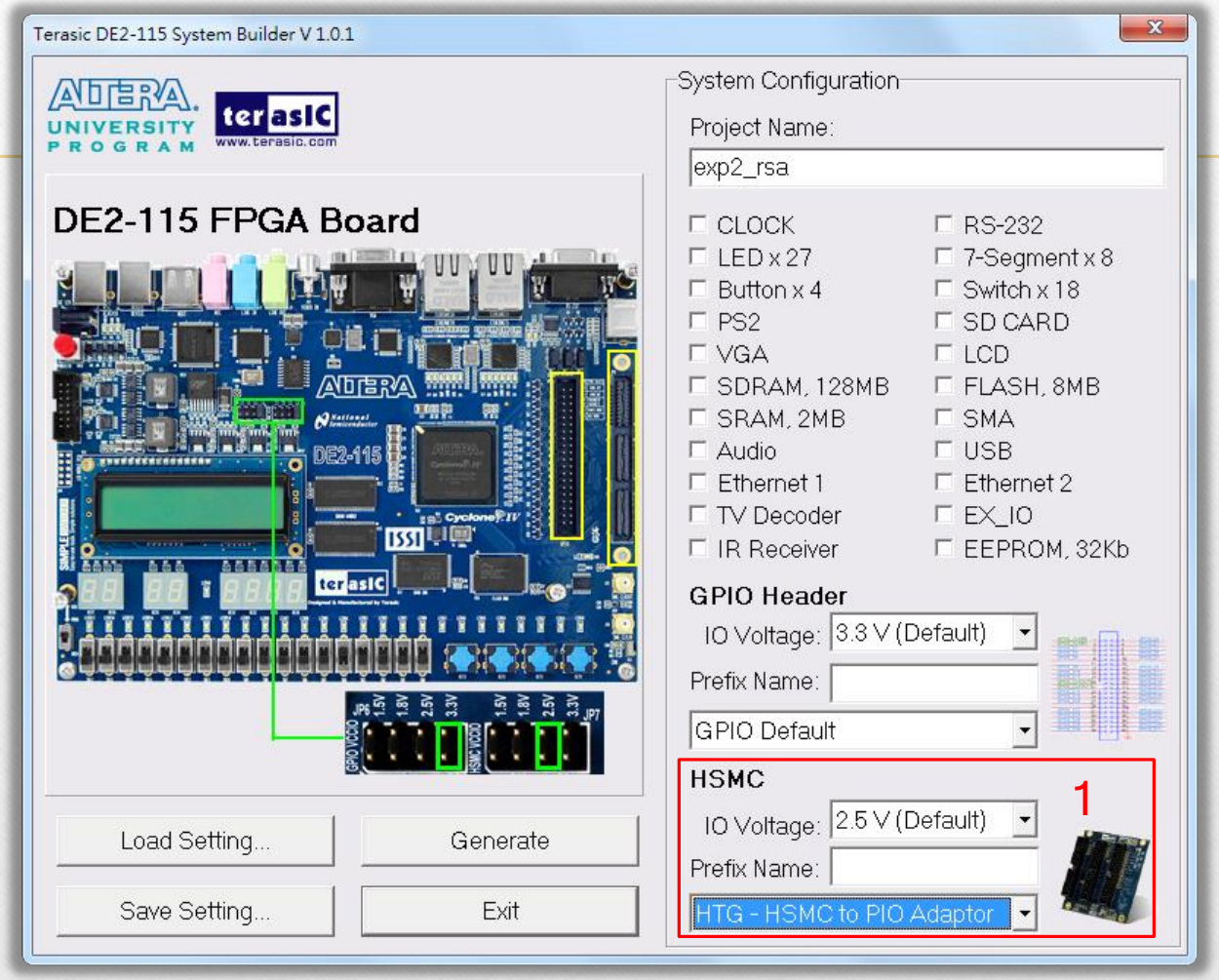
System Configuration



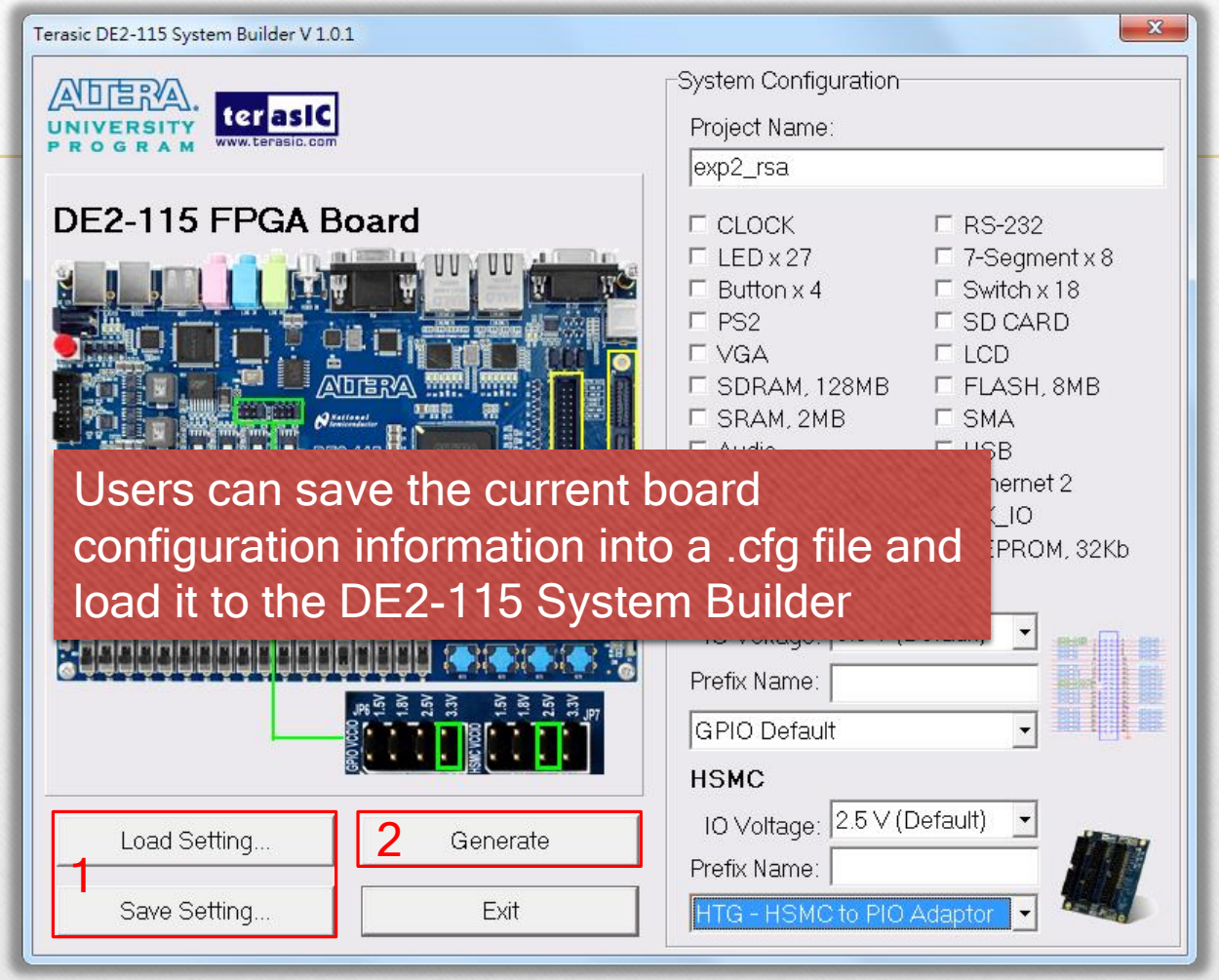
GPIO Expansion



HSMC Expansion



Project Setting Management



Project Generation

- When users press the Generation buttion, the DE2-115 System Builder will generate the corresponding Quartus II files and documents.

No.	*Filename*	*Description*
1	exp2_rsa.v	Top level verilog HDL file for Quartus II
2	exp2_rsa.qpf	Quartus II Project File
3	exp2_rsa.qsf	Quartus II Setting File
4	exp2_rsa.sdc	Synopsis Design Constraints file for Quartus II
5	exp2_rsa.htm	Pin Assignment Document

THDB-HTG Board

- This figure illustrates how the THDB-HTG board is connected to the DE2-115 board.

Be sure to **turn off** the power whenever you connect or disconnect the THDB-HTG board!!

exp2_rsa.htm (1/2)

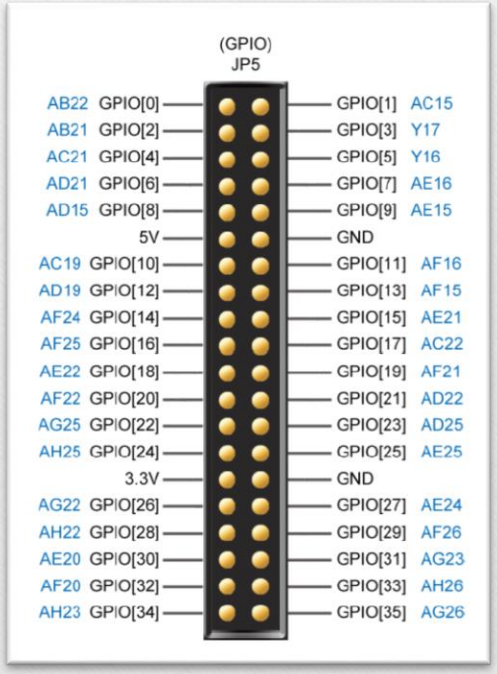
exp2_rsa.htm

file:///C:/Users/Trumen/Desktop/exp2_rsa/exp2_

GPIO connect to GPIO Default

Name	Location	Direction	Standard	GPIO Pin Index
GPIO[0]	AB22	inout	3.3-V LVTTL	1
GPIO[1]	AC15	inout	3.3-V LVTTL	2
GPIO[2]	AB21	inout	3.3-V LVTTL	3
GPIO[3]	Y17	inout	3.3-V LVTTL	4
GPIO[4]	AC21	inout	3.3-V LVTTL	5
GPIO[5]	Y16	inout	3.3-V LVTTL	6
GPIO[6]	AD21	inout	3.3-V LVTTL	7
GPIO[7]	AE16	inout	3.3-V LVTTL	8
GPIO[8]	AD15	inout	3.3-V LVTTL	9
GPIO[9]	AE15	inout	3.3-V LVTTL	10
GPIO[10]	AC19	inout	3.3-V LVTTL	13
GPIO[11]	AF16	inout	3.3-V LVTTL	14
GPIO[12]	AD19	inout	3.3-V LVTTL	15
GPIO[13]	AF15	inout	3.3-V LVTTL	16
GPIO[14]	AF24	inout	3.3-V LVTTL	17
GPIO[15]	AE21	inout	3.3-V LVTTL	18
GPIO[16]	AF25	inout	3.3-V LVTTL	19
GPIO[17]	AC22	inout	3.3-V LVTTL	20

DE2_115_User_manual.pdf
4.8 Usiing the Expansiion Header



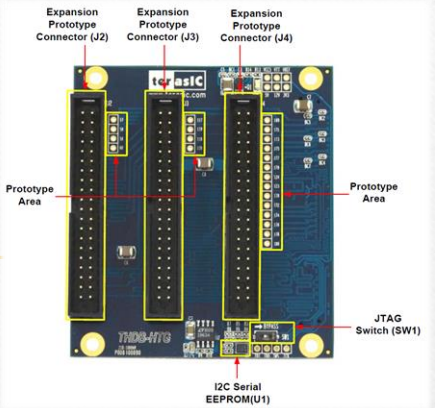
exp2_rsa.htm (2/2)

exp2_rsa.htm

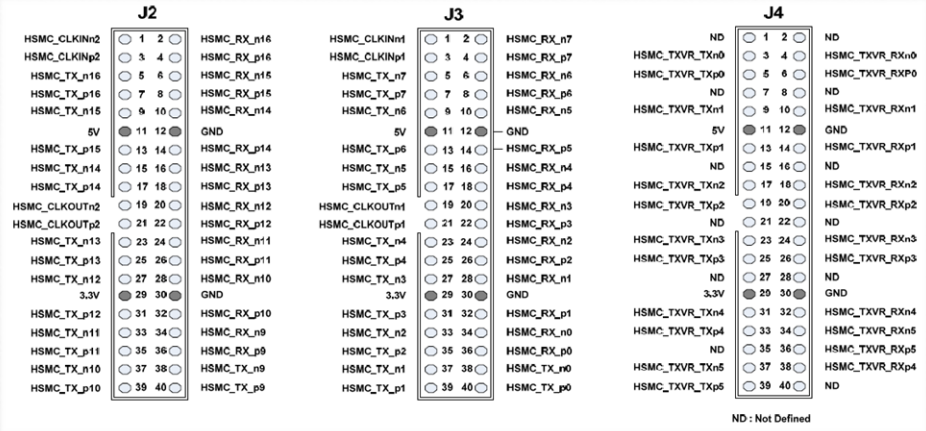
file:///C:/Users/Trumen/Desktop/exp2_rsa/exp2_

HSMC connect to HTG - HSMC to PIO Adaptor

Name	Location	Direction	Standard	HSMC Pin Index
HSMC_CLKOUT_0	AD28	output	2.5 V	39
HSMC_CLKIN_0	AH15	input	2.5 V	40
HSMC_D[0]	AE26	inout	2.5 V	41
HSMC_D[1]	AE28	inout	2.5 V	42
HSMC_D[2]	AE27	inout	2.5 V	43
HSMC_D[3]	AF27	inout	2.5 V	44
HSMC_TX_p[0]	D27	inout	2.5 V	47
HSMC_RX_p[0]	F24	inout	2.5 V	48
HSMC_TX_n[0]	D28	inout	2.5 V	49
HSMC_RX_n[0]	F25	inout	2.5 V	50
HSMC_TX_p[1]	E27	inout	2.5 V	53
HSMC_RX_p[1]	D26	inout	2.5 V	54
HSMC_TX_n[1]	E28	inout	2.5 V	55
HSMC_RX_n[1]	C27	inout	2.5 V	56
HSMC_TX_p[2]	F27	inout	2.5 V	59
HSMC_RX_p[2]	F26	inout	2.5 V	60
HSMC_TX_n[2]	F28	inout	2.5 V	61
HSMC_RX_n[2]	E26	inout	2.5 V	62



THDB-HTG_V1.0.3.pdf
1-6 Expansion Prototype Connectors



exp2_rsa.sdc

- Remember to modify the .sdc file.
  - clock, i/o delay, etc.

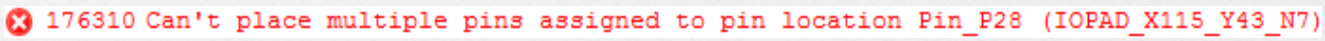
exp2_rsa.sdc

```
1  #**************************************************************
2  # This .sdc file is created by Terasic Tool.
3  # Users are recommended to modify this file to match users l
4  #**************************************************************
5
6  #**************************************************************
7  # Create Clock
8  #**************************************
9
10 #**************************************
11 # Create Generated Clock
12 #**************************************
13 derive_pll_clocks
14
15
16
17 #**************************************************************
18 # Set Clock Latency
```

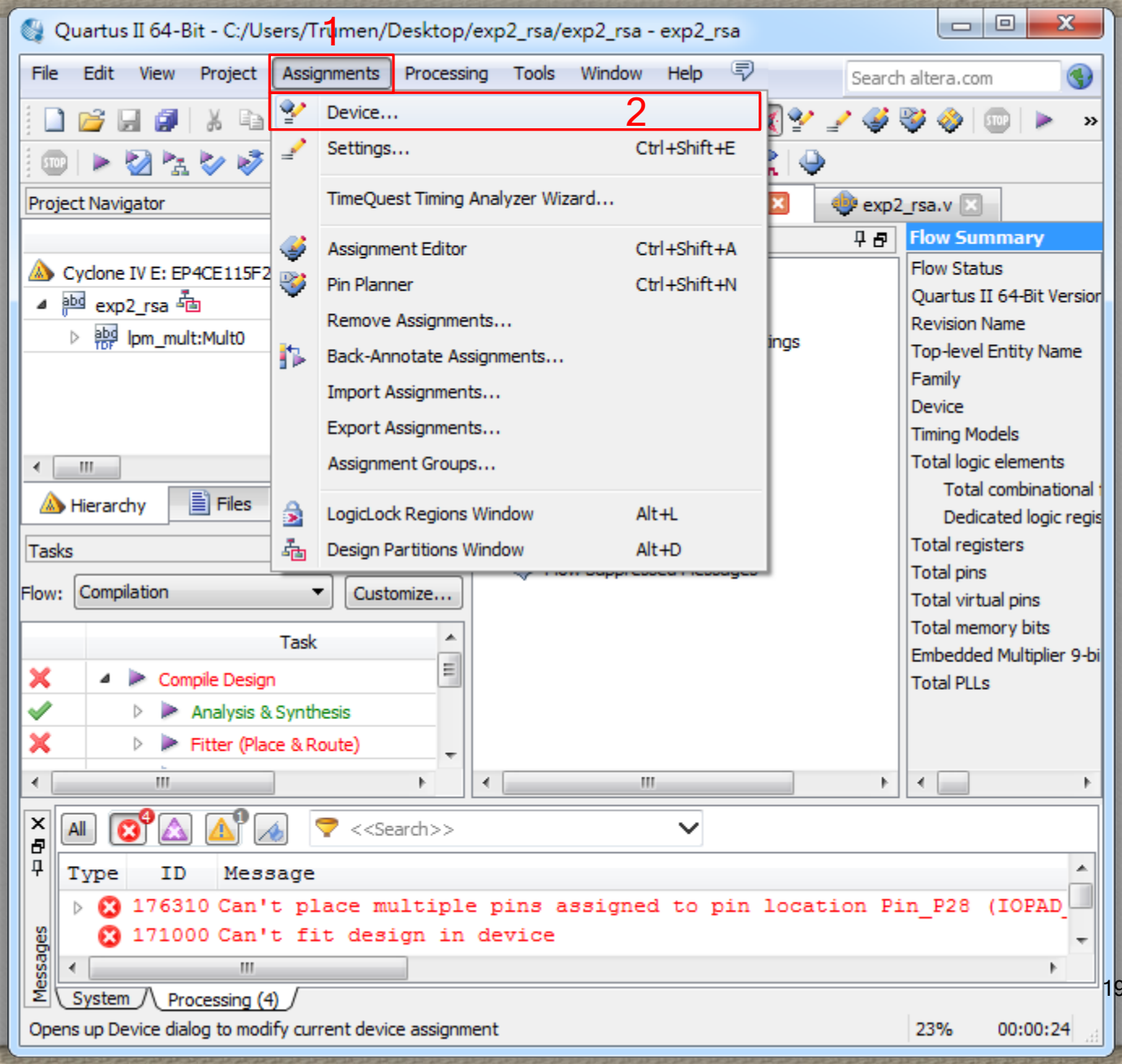
```
create_clock -period 1000 [get_ports clk]
derive_clock_uncertainty
set_input_delay 0 -clock clk [all_inputs]
set_output_delay 0 -clock clk [all_outputs]
```

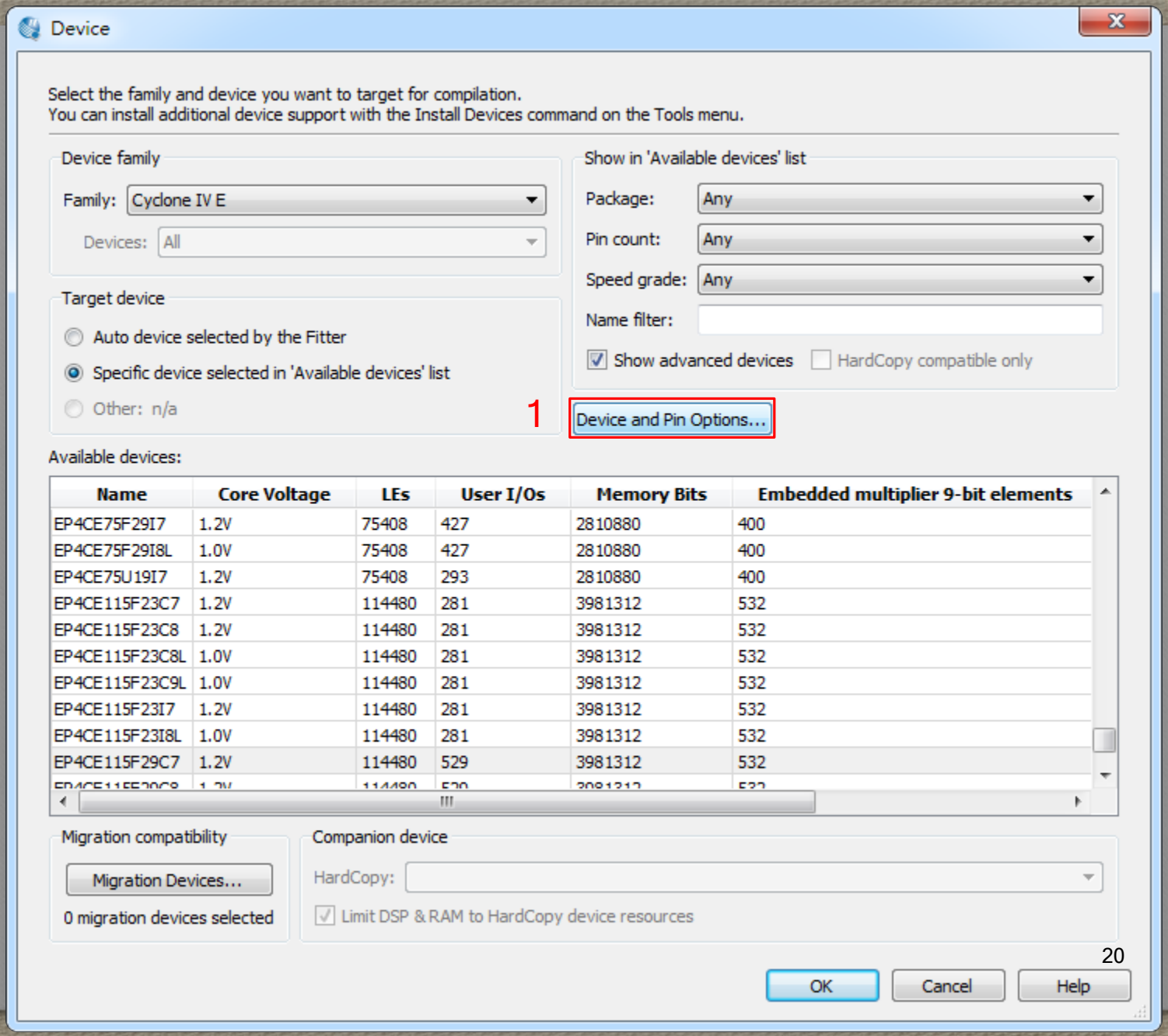
Can't place multiple pins…?

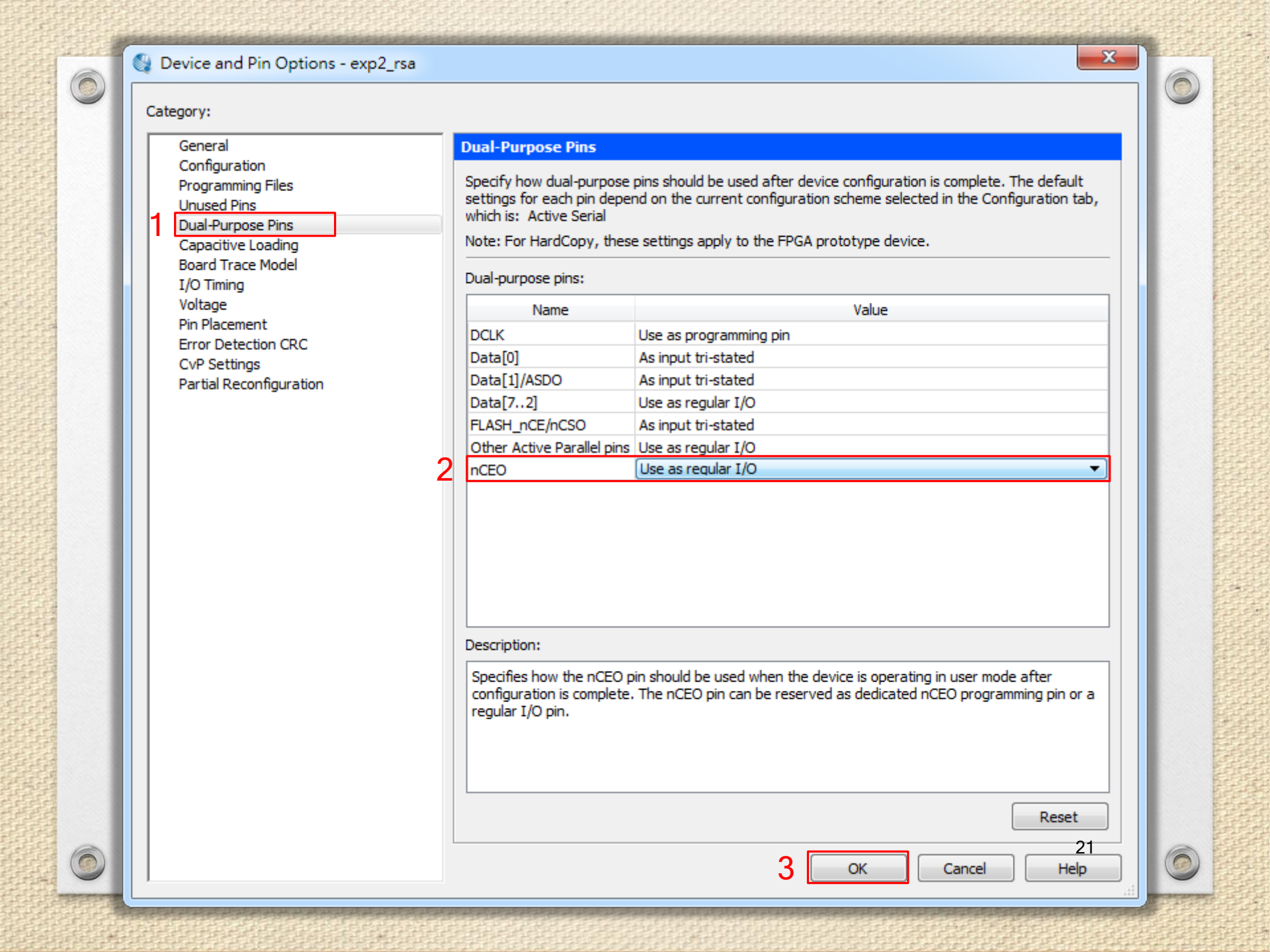
- If you try to assign pins by yourself, this error message may occur.

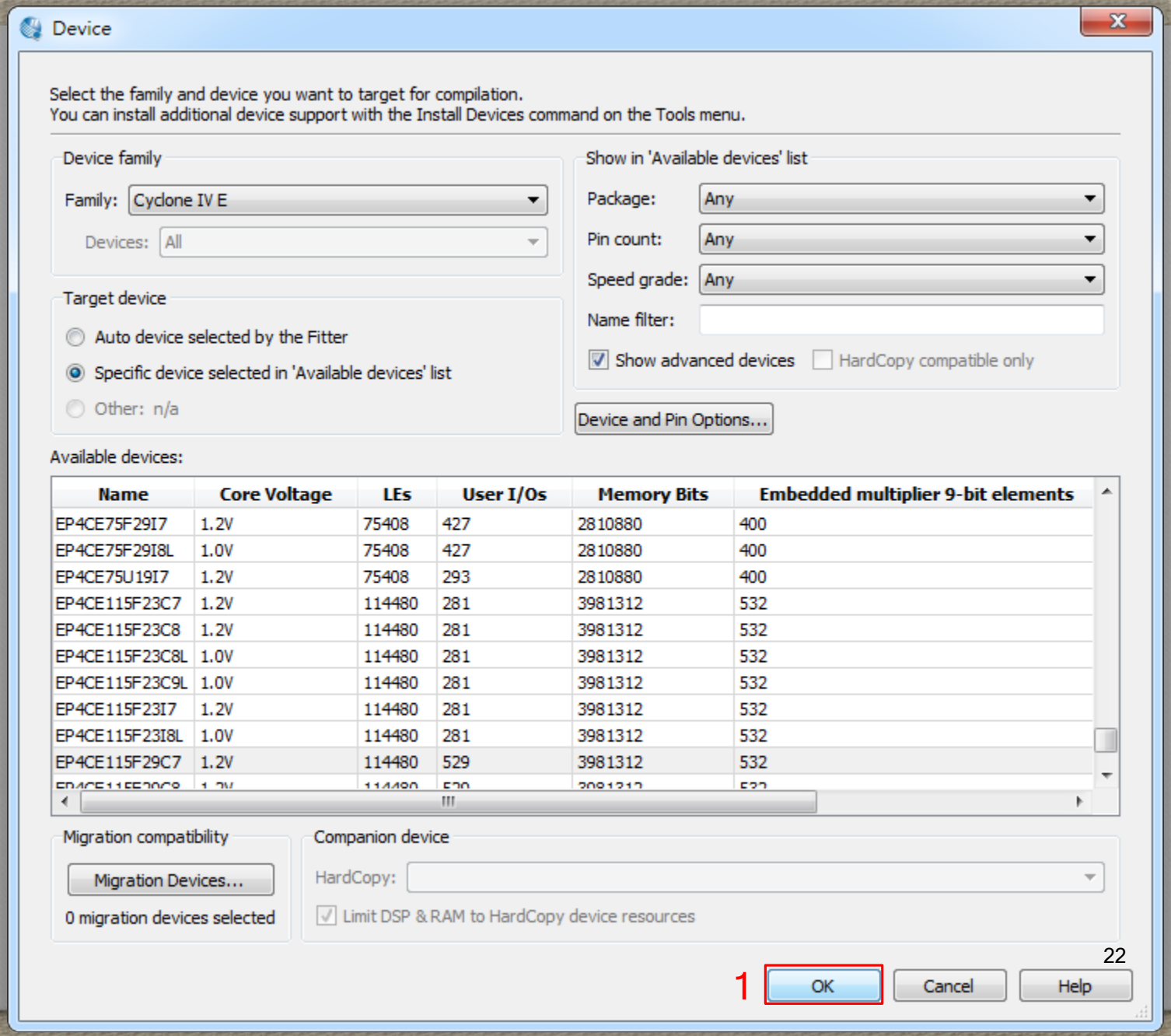


- How to fix it?


Quartus II 64-Bit - C:/Users/Truimen/Desktop/exp2_rsa/exp2_rsa - exp2_rsa
1
File
Edit
View
Project
Assignments
Processing
Tools
Window
Help
Search altera.com
2
Device...
Settings... Ctrl+Shift+E
TimeQuest Timing Analyzer Wizard...
Assignment Editor Ctrl+Shift+A
Pin Planner Ctrl+Shift+N
Remove Assignments...
Back-Annotate Assignments...
Import Assignments...
Export Assignments...
Assignment Groups...
LogicLock Regions Window Alt+L
Design Partitions Window Alt+D
Project Navigator
Cyclone IV E: EP4CE115F2
exp2_rsa
lpm_mult:Mult0
exp2_rsa.v
Flow Summary
Flow Status
Quartus II 64-Bit Version
Revision Name
Top-level Entity Name
Family
Device
Timing Models
Total logic elements
Total combinational
Dedicated logic regis
Total registers
Total pins
Total virtual pins
Total memory bits
Embedded Multiplier 9-bi
Total PLLs
Hierarchy
Files
Tasks
Flow: Compilation
Customize...
Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
All
<<Search>>
Type ID Message
176310 Can't place multiple pins assigned to pin location Pin_P28 (IOPAD_
171000 Can't fit design in device
Messages
System
Processing (4)
Opens up Device dialog to modify current device assignment
23%
00:00:24


Device
Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.
Device family
Family: Cyclone IV E
Devices: All
Target device
Auto device selected by the Fitter
Specific device selected in 'Available devices' list
Other: n/a
1
Show in 'Available devices' list
Package: Any
Pin count: Any
Speed grade: Any
Name filter:
Show advanced devices
HardCopy compatible only
Device and Pin Options...
Available devices:
Name | Core Voltage | LEs | User I/Os | Memory Bits | Embedded multiplier 9-bit elements
EP4CE75F29I7 | 1.2V | 75408 | 427 | 2810880 | 400
EP4CE75F29I8L | 1.0V | 75408 | 427 | 2810880 | 400
EP4CE75U19I7 | 1.2V | 75408 | 293 | 2810880 | 400
EP4CE115F23C7 | 1.2V | 114480 | 281 | 3981312 | 532
EP4CE115F23C8 | 1.2V | 114480 | 281 | 3981312 | 532
EP4CE115F23C8L | 1.0V | 114480 | 281 | 3981312 | 532
EP4CE115F23C9L | 1.0V | 114480 | 281 | 3981312 | 532
EP4CE115F23I7 | 1.2V | 114480 | 281 | 3981312 | 532
EP4CE115F23I8L | 1.0V | 114480 | 281 | 3981312 | 532
EP4CE115F29C7 | 1.2V | 114480 | 529 | 3981312 | 532
Migration compatibility
Migration Devices...
0 migration devices selected
Companion device
HardCopy:
Limit DSP & RAM to HardCopy device resources
20
OK
Cancel
Help


Device and Pin Options - exp2_rsa
Category:
General
Configuration
Programming Files
Unused Pins
1
Dual-Purpose Pins
Capacitive Loading
Board Trace Model
I/O Timing
Voltage
Pin Placement
Error Detection CRC
CvP Settings
Partial Reconfiguration
Dual-Purpose Pins
Specify how dual-purpose pins should be used after device configuration is complete. The default settings for each pin depend on the current configuration scheme selected in the Configuration tab, which is: Active Serial
Note: For HardCopy, these settings apply to the FPGA prototype device.
Dual-purpose pins:
Name
Value
DCLK
Use as programming pin
Data[0]
As input tri-stated
Data[1]/ASDO
As input tri-stated
Data[7..2]
Use as regular I/O
FLASH_nCE/nCSO
As input tri-stated
Other Active Parallel pins
Use as regular I/O
2
nCEO
Use as regular I/O
Description:
Specifies how the nCEO pin should be used when the device is operating in user mode after configuration is complete. The nCEO pin can be reserved as dedicated nCEO programming pin or a regular I/O pin.
Reset
21
3
OK
Cancel
Help


Device
Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.
Device family
Family: Cyclone IV E
Devices: All
Target device
Auto device selected by the Fitter
Specific device selected in 'Available devices' list
Other: n/a
Show in 'Available devices' list
Package: Any
Pin count: Any
Speed grade: Any
Name filter:
Show advanced devices
HardCopy compatible only
Device and Pin Options...
Available devices:
Name | Core Voltage | LEs | User I/Os | Memory Bits | Embedded multiplier 9-bit elements
EP4CE75F29I7 | 1.2V | 75408 | 427 | 2810880 | 400
EP4CE75F29I8L | 1.0V | 75408 | 427 | 2810880 | 400
EP4CE75U19I7 | 1.2V | 75408 | 293 | 2810880 | 400
EP4CE115F23C7 | 1.2V | 114480 | 281 | 3981312 | 532
EP4CE115F23C8 | 1.2V | 114480 | 281 | 3981312 | 532
EP4CE115F23C8L | 1.0V | 114480 | 281 | 3981312 | 532
EP4CE115F23C9L | 1.0V | 114480 | 281 | 3981312 | 532
EP4CE115F23I7 | 1.2V | 114480 | 281 | 3981312 | 532
EP4CE115F23I8L | 1.0V | 114480 | 281 | 3981312 | 532
EP4CE115F29C7 | 1.2V | 114480 | 529 | 3981312 | 532
Migration compatibility
Migration Devices...
0 migration devices selected
Companion device
HardCopy:
Limit DSP & RAM to HardCopy device resources
22
1
OK
Cancel
Help

ModelSim-Altera

Introduction to ModelSim (1/5)

- ModelSim is a simulation and verification tool for VHDL, Verilog, SystemVerilog, and mixed language designs.
- The following diagram shows the basic steps for simulating a design in ModelSim.

Introduction to ModelSim (2/5)

- Creating the Working Library
  - In ModelSim, all designs are compiled into a library.
  - You typically start a new simulation in ModelSim by creating a working library called "work," which is the default library name used by the compiler as the default destination for compiled design units.

Introduction to ModelSim (3/5)

- Compiling Your Design
  - After creating the working library, you compile your design units into it.
  - The ModelSim library format is compatible across all supported platforms.
  - You can simulate your design on any platform without having to recompile your design.

Introduction to ModelSim (4/5)

- Loading the Simulator with Your Design and Running the Simulation
  - With the design compiled, you load the simulator with your design by invoking the simulator on a top-level module (Verilog) or a configuration or entity/architecture pair (VHDL).

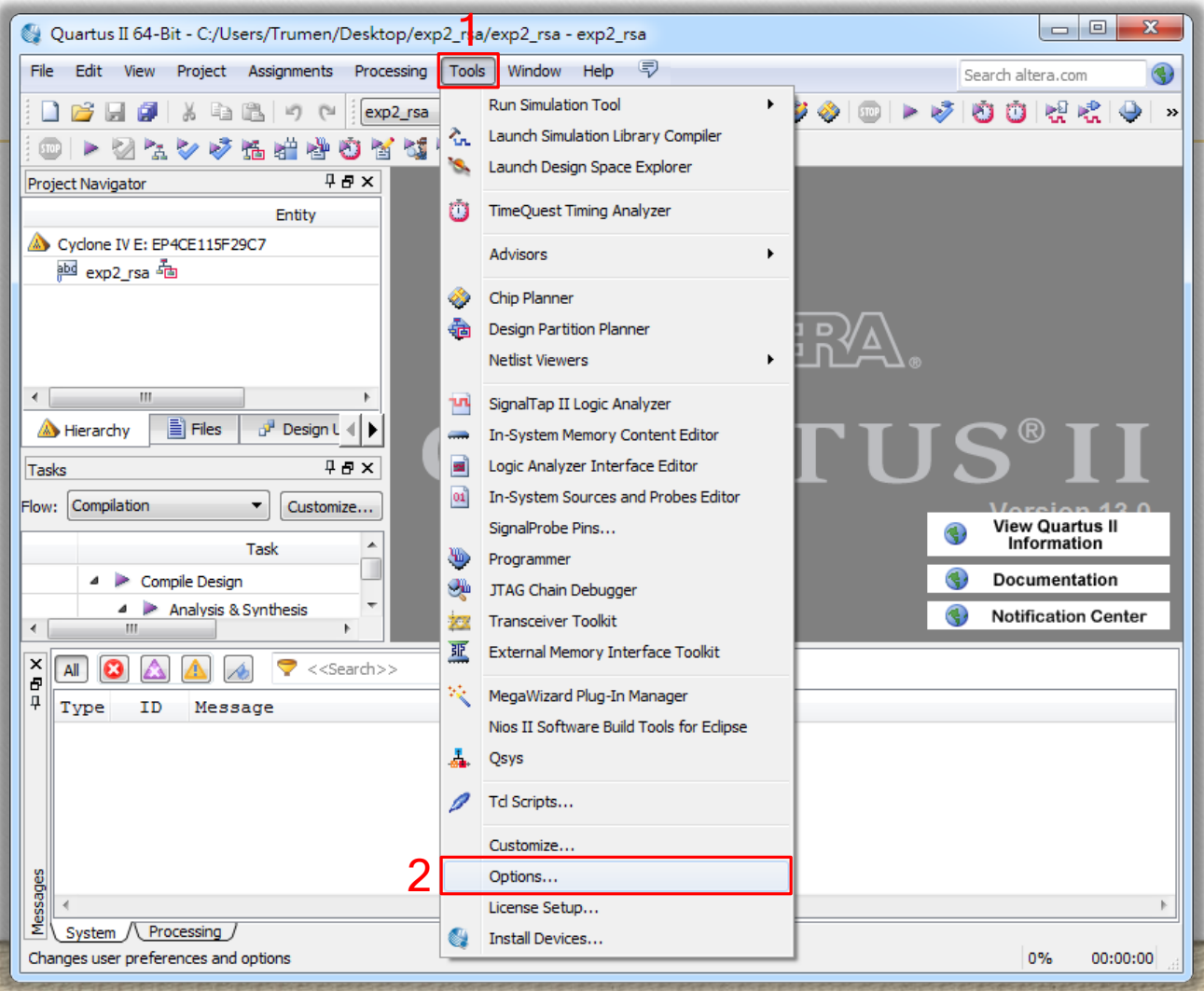
Introduction to ModelSim (5/5)

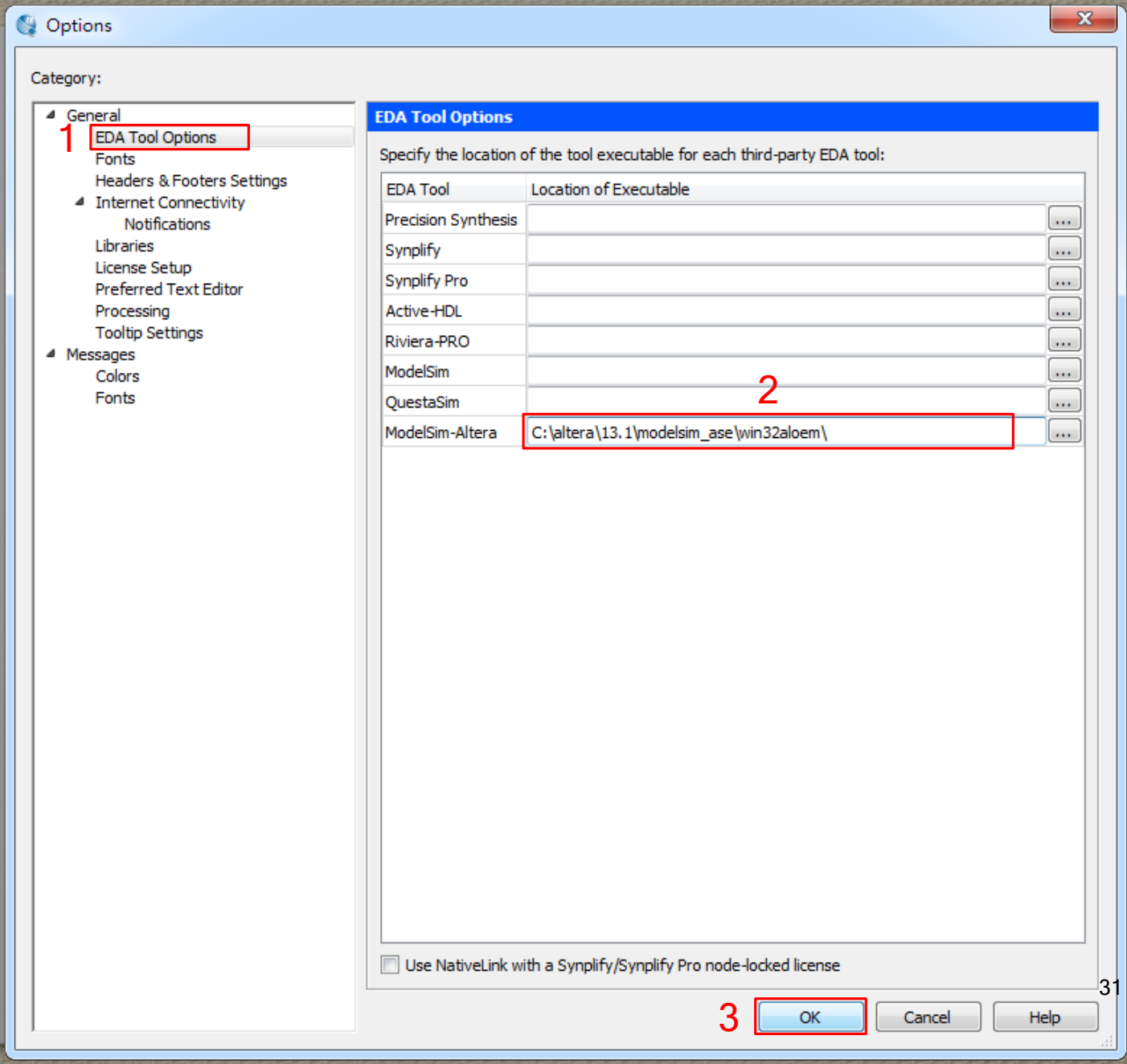
- Debugging Your Results
  - If you don’t get the results you expect, you can use ModelSim’s robust debugging environment to track down the cause of the problem.

ModelSim-Altera

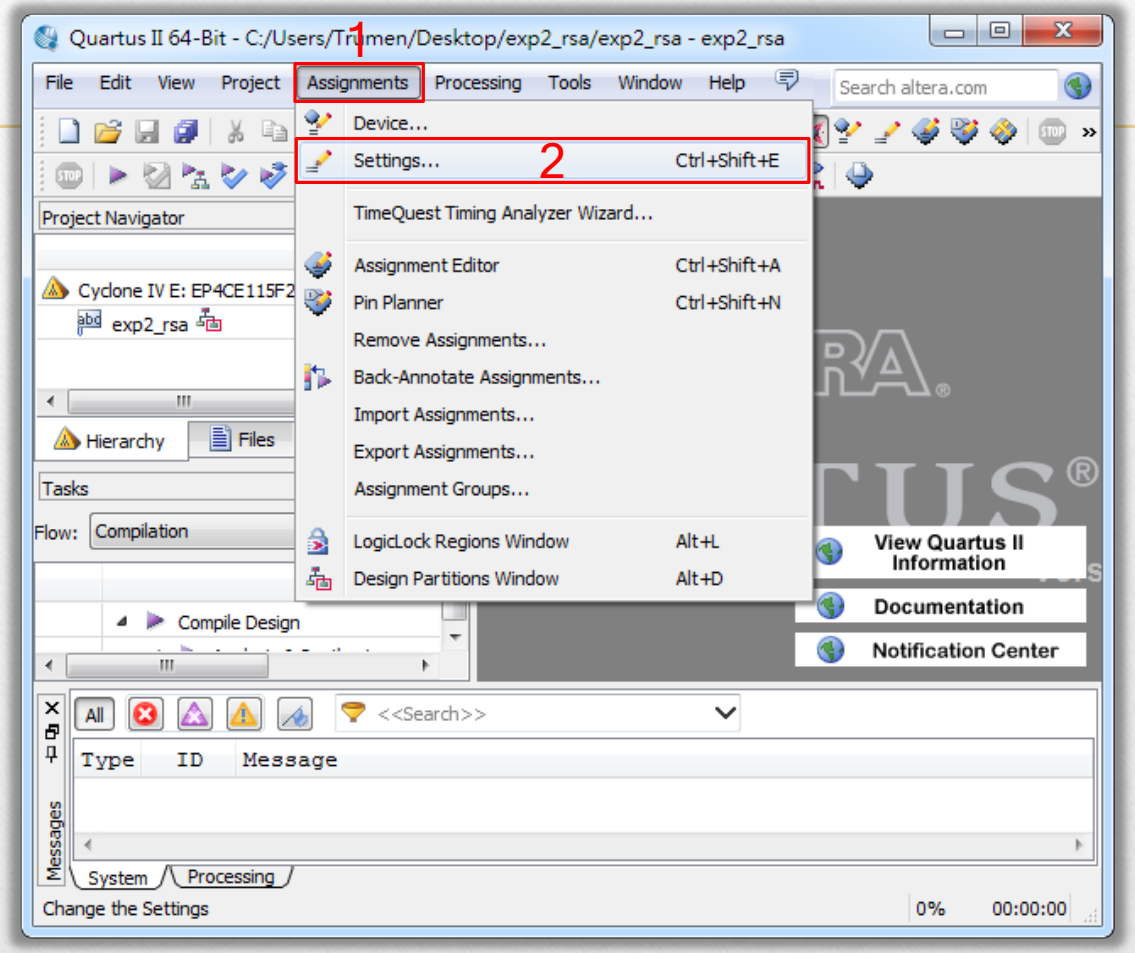
- Altera Quartus II software allows the user to launch Modelsim-Altera simulator from within the software using the Quartus II feature called NativeLink.
- It facilitates the process of simulation by providing an easy to use mechanism and precompiled libraries for simulation.

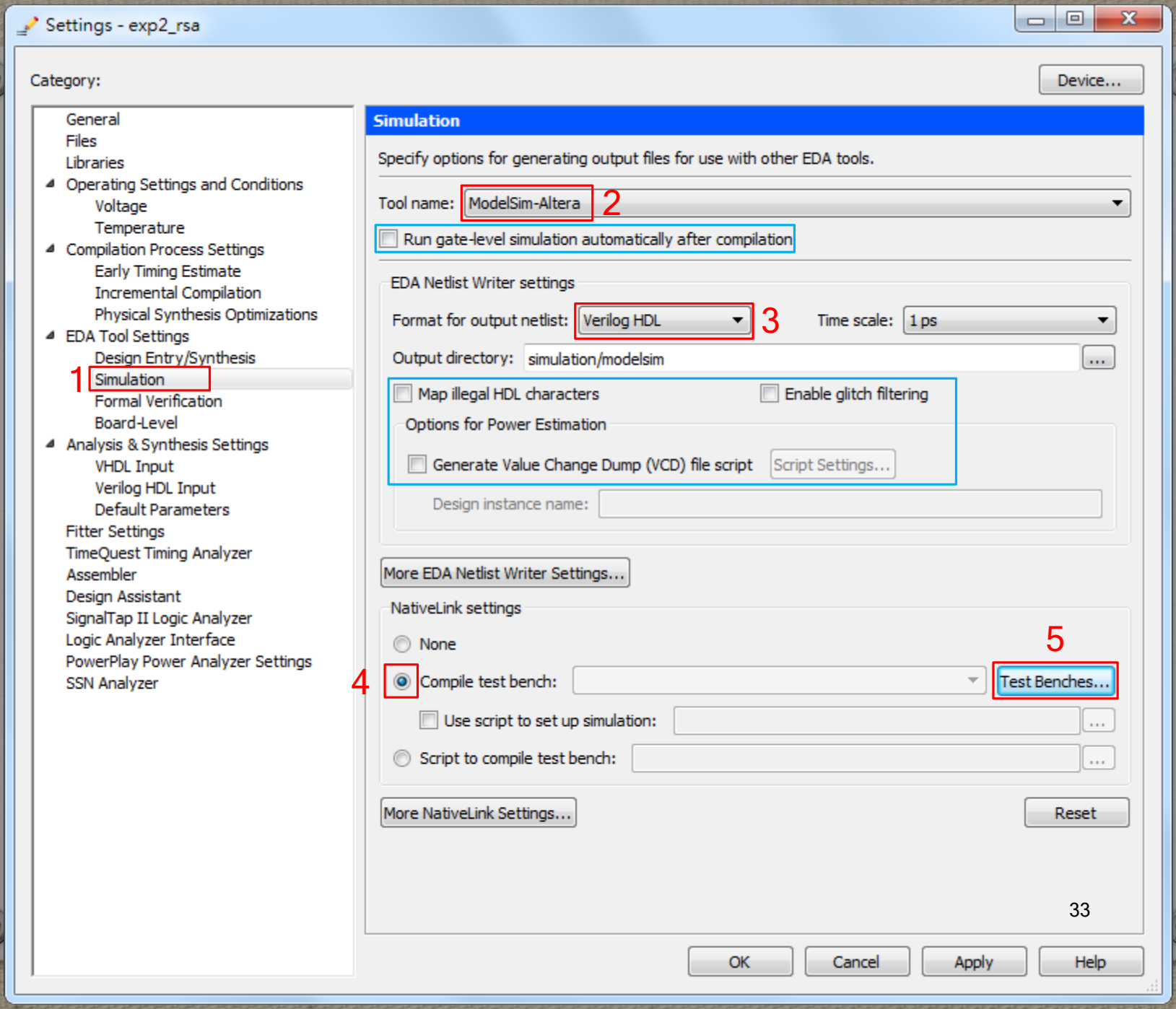
Setting up EDA Tool Options

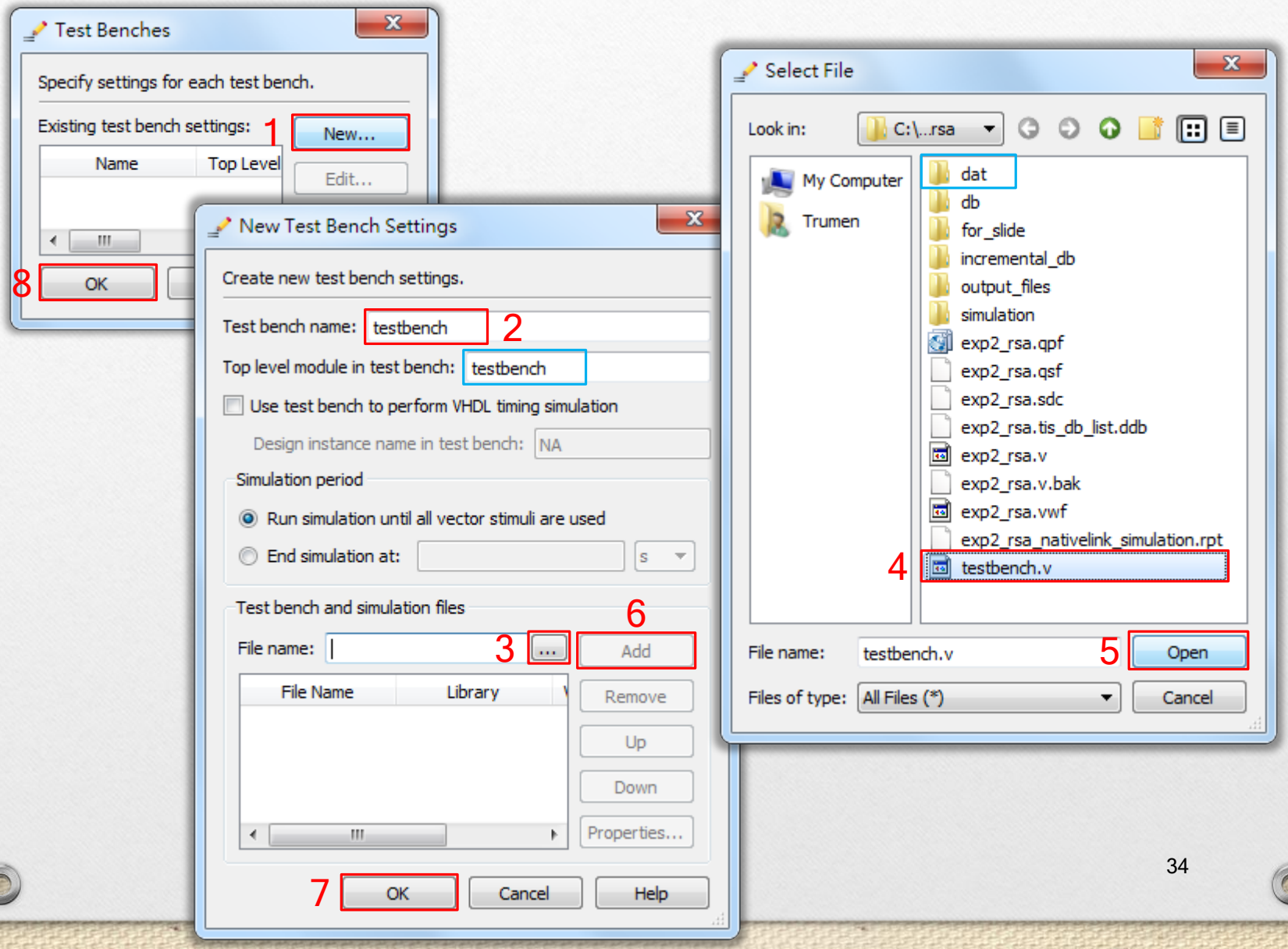


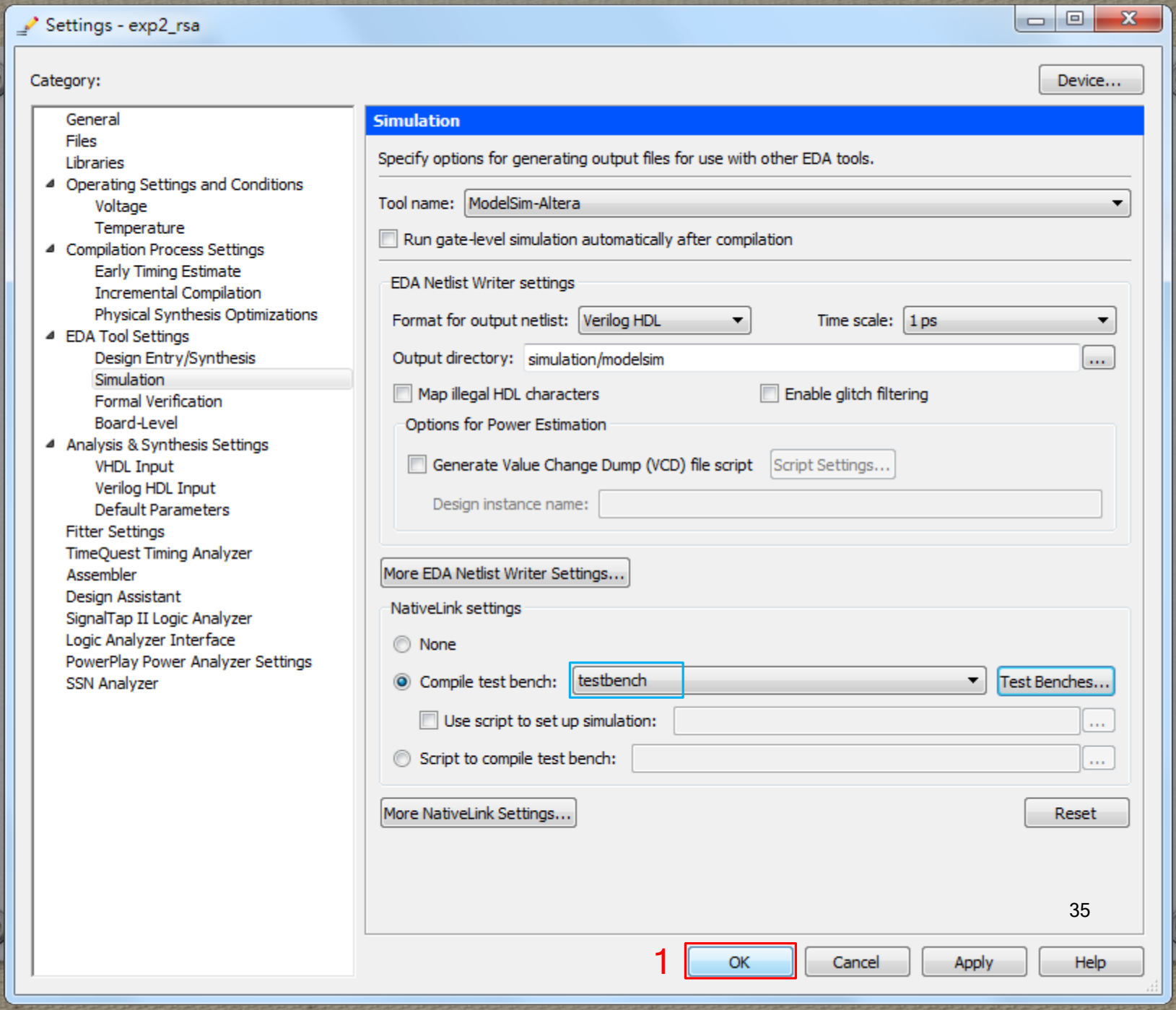

Options
Category:
General
EDA Tool Options
Fonts
Headers & Footers Settings
Internet Connectivity
Notifications
Libraries
License Setup
Preferred Text Editor
Processing
Tooltip Settings
Messages
Colors
Fonts
1
EDA Tool Options
Specify the location of the tool executable for each third-party EDA tool:
EDA Tool
Location of Executable
Precision Synthesis
Synplify
Synplify Pro
Active-HDL
Riviera-PRO
ModelSim
QuestaSim
ModelSim-Altera
C:\altera\13.1\modelsim_ase\win32aloem\
2
Use NativeLink with a Synplify/Synplify Pro node-locked license
3
OK
Cancel
Help

Setting Up the Simulation




Settings - exp2_rsa
Category:
Device...
General
Files
Libraries
Operating Settings and Conditions
Voltage
Temperature
Compilation Process Settings
Early Timing Estimate
Incremental Compilation
Physical Synthesis Optimizations
EDA Tool Settings
Design Entry/Synthesis
1
Simulation
Formal Verification
Board-Level
Analysis & Synthesis Settings
VHDL Input
Verilog HDL Input
Default Parameters
Fitter Settings
TimeQuest Timing Analyzer
Assembler
Design Assistant
SignalTap II Logic Analyzer
Logic Analyzer Interface
PowerPlay Power Analyzer Settings
SSN Analyzer
Simulation
Specify options for generating output files for use with other EDA tools.
Tool name:
ModelSim-Altera
2
Run gate-level simulation automatically after compilation
EDA Netlist Writer settings
Format for output netlist:
Verilog HDL
3
Time scale:
1 ps
Output directory:
simulation/modelsim
Map illegal HDL characters
Enable glitch filtering
Options for Power Estimation
Generate Value Change Dump (VCD) file script
Script Settings...
Design instance name:
More EDA Netlist Writer Settings...
NativeLink settings
None
4
Compile test bench:
5
Test Benches...
Use script to set up simulation:
Script to compile test bench:
More NativeLink Settings...
Reset
OK
Cancel
Apply
Help


Test Benches
Specify settings for each test bench.
Existing test bench settings:
1
New...
Edit...
Name
Top Level
8
OK
New Test Bench Settings
Create new test bench settings.
Test bench name:
testbench
2
Top level module in test bench:
testbench
Use test bench to perform VHDL timing simulation
Design instance name in test bench:
NA
Simulation period
Run simulation until all vector stimuli are used
End simulation at:
s
Test bench and simulation files
File name:
3
...
6
Add
File Name
Library
Remove
Up
Down
Properties...
7
OK
Cancel
Help
Select File
Look in:
C:\...rsa
My Computer
Trumen
dat
db
for_slide
incremental_db
output_files
simulation
exp2_rsa.qpf
exp2_rsa.qsf
exp2_rsa.sdc
exp2_rsa.tis_db_list.ddb
exp2_rsa.v
exp2_rsa.v.bak
exp2_rsa.vwf
exp2_rsa_nativelink_simulation.rpt
4
testbench.v
File name:
testbench.v
5
Open
Files of type:
All Files (*)
Cancel


Settings - exp2_rsa
Category:
Device...
General
Files
Libraries
Operating Settings and Conditions
Voltage
Temperature
Compilation Process Settings
Early Timing Estimate
Incremental Compilation
Physical Synthesis Optimizations
EDA Tool Settings
Design Entry/Synthesis
Simulation
Formal Verification
Board-Level
Analysis & Synthesis Settings
VHDL Input
Verilog HDL Input
Default Parameters
Fitter Settings
TimeQuest Timing Analyzer
Assembler
Design Assistant
SignalTap II Logic Analyzer
Logic Analyzer Interface
PowerPlay Power Analyzer Settings
SSN Analyzer
Simulation
Specify options for generating output files for use with other EDA tools.
Tool name: ModelSim-Altera
Run gate-level simulation automatically after compilation
EDA Netlist Writer settings
Format for output netlist: Verilog HDL
Time scale: 1 ps
Output directory: simulation/modelsim
Map illegal HDL characters
Enable glitch filtering
Options for Power Estimation
Generate Value Change Dump (VCD) file script
Script Settings...
Design instance name:
More EDA Netlist Writer Settings...
NativeLink settings
None
Compile test bench: testbench
Test Benches...
Use script to set up simulation:
Script to compile test bench:
More NativeLink Settings...
Reset
35
1
OK
Cancel
Apply
Help

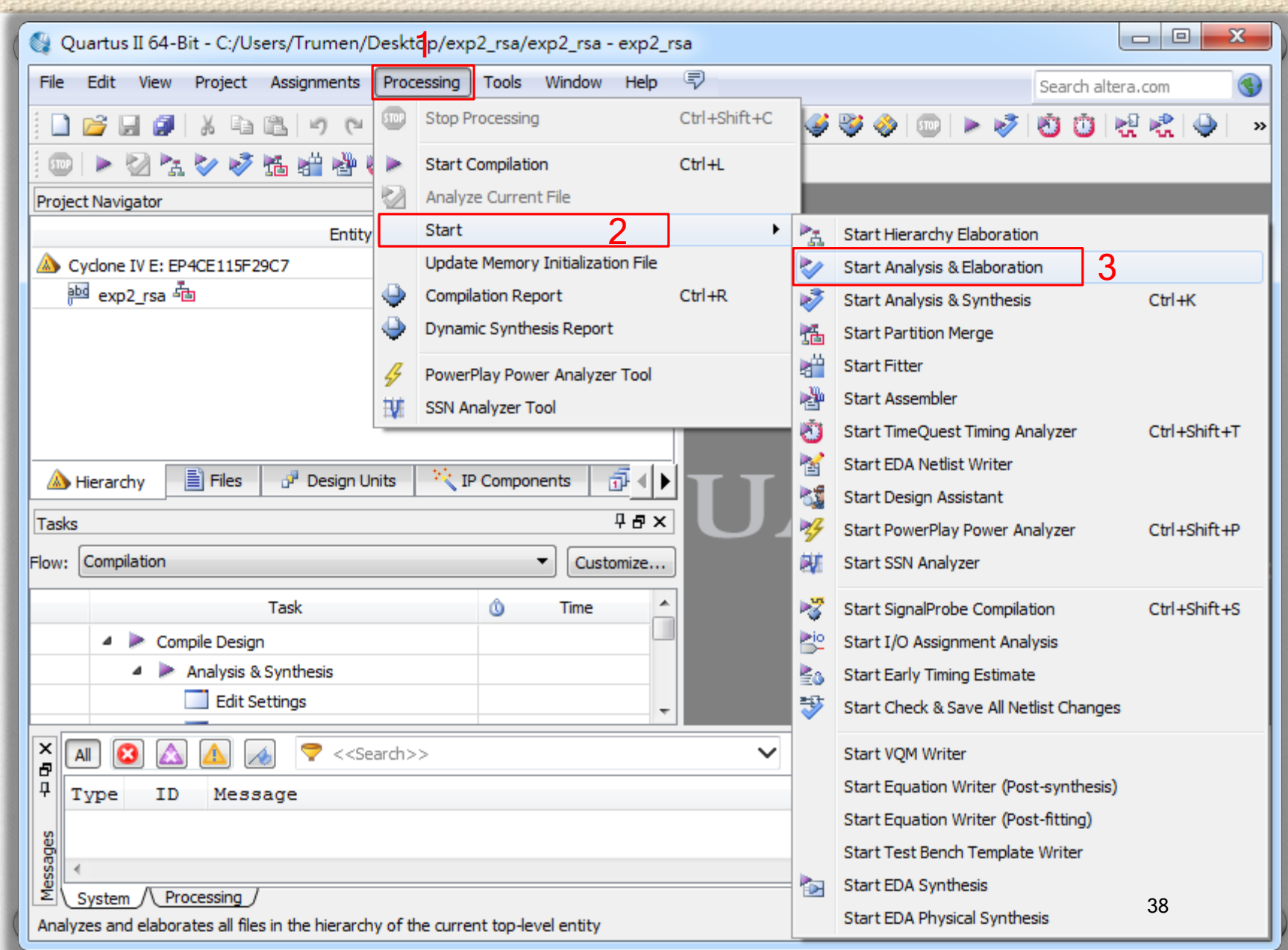
Before Simulation…

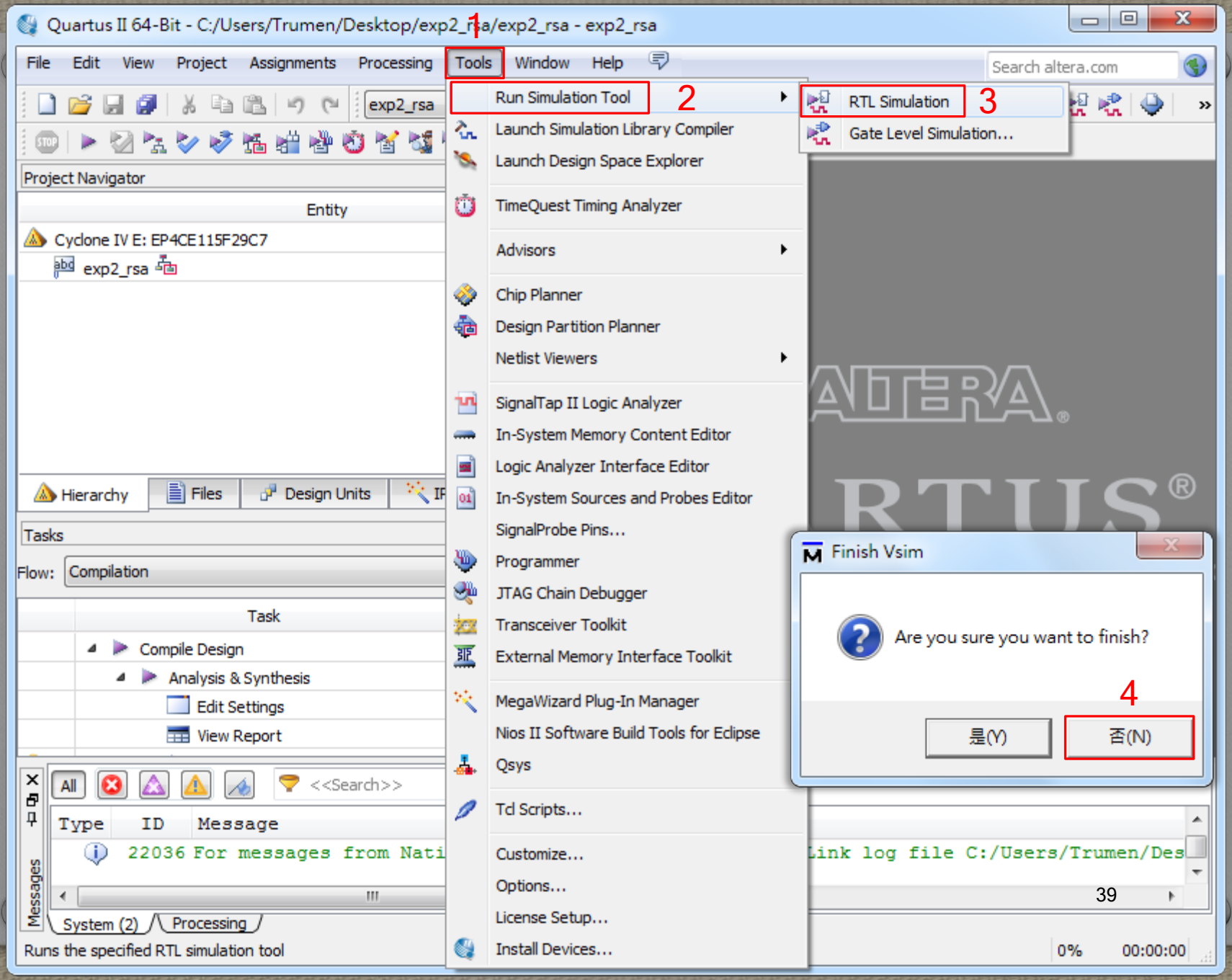
- We should compile our design before simulation to generate a simulation snapshot.
- "Start Analysis & Elaboration" is enough, and it takes much less time than "Start Compilation".
- And then we can run the simulation.

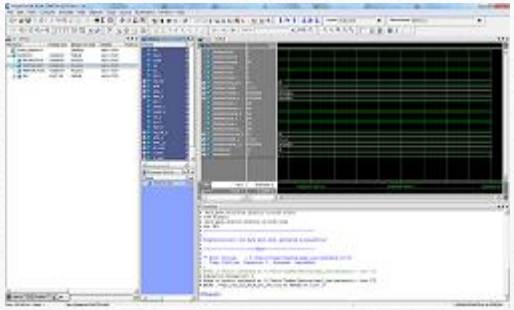
Issues of Working Directory

- The working directory of ModelSim-Altera is under "(project directory)/simulation/modelsim", so be careful of setting the directory of input data in the testbench.

```
initial $readmemh("../../dat/dn.dat", dn_mem);
initial $readmemh("../../dat/c.dat", c_mem);
initial $readmemh("../../dat/m.dat", m_mem);
```


Quartus II 64-Bit - C:/Users/Trumen/Desktop/exp2_rsa/exp2_rsa - exp2_rsa
1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
Stop Processing Ctrl+Shift+C
Start Compilation Ctrl+L
Analyze Current File
Start
2
Update Memory Initialization File
Compilation Report Ctrl+R
Dynamic Synthesis Report
PowerPlay Power Analyzer Tool
SSN Analyzer Tool
Start Hierarchy Elaboration
Start Analysis & Elaboration
3
Start Analysis & Synthesis Ctrl+K
Start Partition Merge
Start Fitter
Start Assembler
Start TimeQuest Timing Analyzer Ctrl+Shift+T
Start EDA Netlist Writer
Start Design Assistant
Start PowerPlay Power Analyzer Ctrl+Shift+P
Start SSN Analyzer
Start SignalProbe Compilation Ctrl+Shift+S
Start I/O Assignment Analysis
Start Early Timing Estimate
Start Check & Save All Netlist Changes
Start VQM Writer
Start Equation Writer (Post-synthesis)
Start Equation Writer (Post-fitting)
Start Test Bench Template Writer
Start EDA Synthesis
Start EDA Physical Synthesis
Project Navigator
Entity
Cyclone IV E: EP4CE115F29C7
exp2_rsa
Hierarchy Files Design Units IP Components
Tasks
Flow: Compilation
Customize...
Task Time
Compile Design
Analysis & Synthesis
Edit Settings
All
<<Search>>
Type ID Message
Messages
System Processing
Analyzes and elaborates all files in the hierarchy of the current top-level entity


Quartus II 64-Bit - C:/Users/Trumen/Desktop/exp2_rsa/exp2_rsa - exp2_rsa
1
File Edit View Project Assignments Processing Tools Window Help
Search altera.com
exp2_rsa
Project Navigator
Entity
Cyclone IV E: EP4CE115F29C7
exp2_rsa
Hierarchy Files Design Units
Tasks
Flow: Compilation
Task
Compile Design
Analysis & Synthesis
Edit Settings
View Report
Run Simulation Tool
2
Launch Simulation Library Compiler
Launch Design Space Explorer
TimeQuest Timing Analyzer
Advisors
Chip Planner
Design Partition Planner
Netlist Viewers
SignalTap II Logic Analyzer
In-System Memory Content Editor
Logic Analyzer Interface Editor
In-System Sources and Probes Editor
SignalProbe Pins...
Programmer
JTAG Chain Debugger
Transceiver Toolkit
External Memory Interface Toolkit
MegaWizard Plug-In Manager
Nios II Software Build Tools for Eclipse
Qsys
Tcl Scripts...
Customize...
Options...
License Setup...
Install Devices...
RTL Simulation
3
Gate Level Simulation...
ALTERA
RTUS
Finish Vsim
Are you sure you want to finish?
4
是(Y)
否(N)
Type ID Message
22036 For messages from Nati
Link log file C:/Users/Trumen/Des
39
Messages
System (2) Processing
Runs the specified RTL simulation tool
0% 00:00:00



Transcript

```
# .main_pane.structure.interior.cs.body.struct
# view signals
# .main_pane.objects.interior.cs.body.tree
# run -all
# ------------------------------------------------------
#
# Congratulations! All data have been generated successfully!
#
# -------------------------PASS-------------------------
#
# ** Note: $finish    : C:/Users/Trumen/Desktop/exp2_rsa/testbench.v(175)
#    Time: 99269 ms  Iteration: 1  Instance: /testbench
# 1
# Break in Module testbench at C:/Users/Trumen/Desktop/exp2_rsa/testbench.v line 175
# Simulation Breakpoint: 1
# Break in Module testbench at C:/Users/Trumen/Desktop/exp2_rsa/testbench.v line 175
# MACRO ./exp2_rsa_run_msim_rtl_verilog.do PAUSED at line 17

VSIM(paused)>
```

Congratulation!

Be sure ModelSim-Altera has found the input data!!

If There are Something Wrong…

- Your simulation takes a long time and seems it will not stop.

```
# ------------------------------------------------------
#
# Error!!! Somethings' wrong with your code ...!!
#
# -------------------------FAIL-------------------------
#
# ** Note: $finish    : C:/Users/Trumen/Desktop/exp2_rsa/testbench.v(184)
#    Time: 1 sec  Iteration: 0  Instance: /testbench
```

- The calculated result is incorrect.

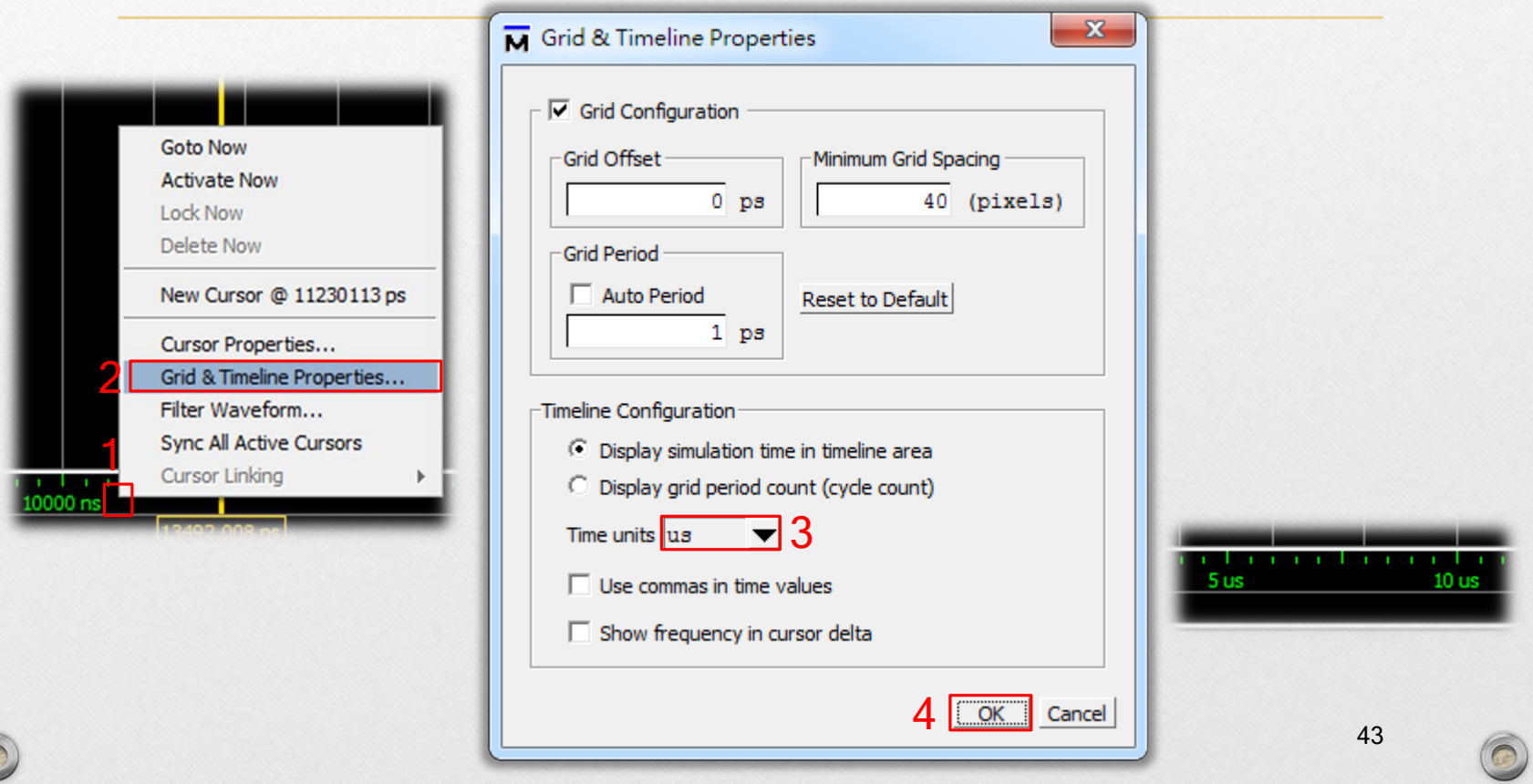
```
# ------------------------------------------------------
#
# ERROR at           0th m[         7:         0]: output 00000051 !=expect 50
#
# -------------------------FAIL-------------------------
#
# ** Note: $finish    : C:/Users/Trumen/Desktop/exp2_rsa/testbench.v(162)
#    Time: 49635 ms  Iteration: 0  Instance: /testbench
```

If the Input Date are not Found…

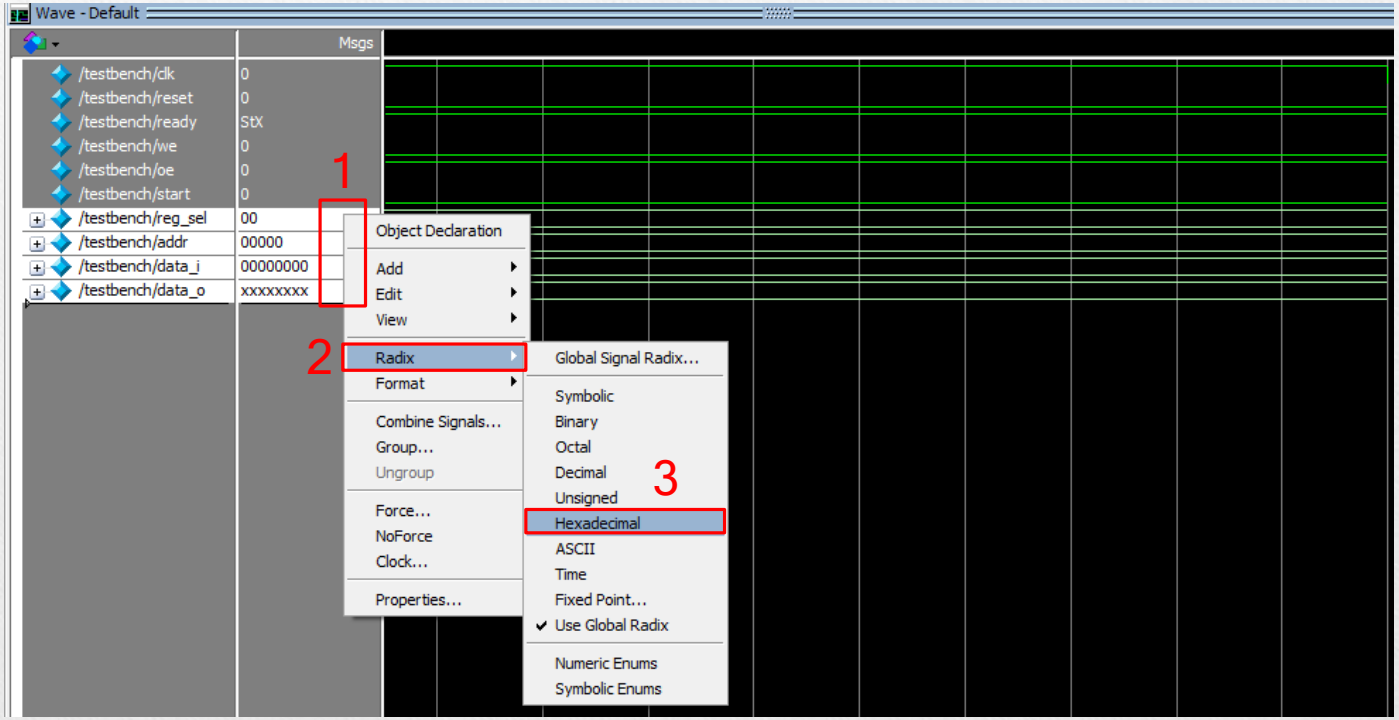
```
# run -all
# ** Warning: (vsim-7) Failed to open readmem file "./dat/dn.dat" in read mode.
#
# No such file or directory. (errno = ENOENT)    : E:/DCLab/102_2/MyExp/Exp2/exp2_rsa/testbench.v(38)
#    Time: 0 ps  Iteration: 0  Instance: /testbench
# ** Warning: (vsim-7) Failed to open readmem file "./dat/c.dat" in read mode.
#
# No such file or directory. (errno = ENOENT)    : E:/DCLab/102_2/MyExp/Exp2/exp2_rsa/testbench.v(39)
#    Time: 0 ps  Iteration: 0  Instance: /testbench
# ** Warning: (vsim-7) Failed to open readmem file "./dat/m.dat" in read mode.
#
# No such file or directory. (errno = ENOENT)    : E:/DCLab/102_2/MyExp/Exp2/exp2_rsa/testbench.v(40)
#    Time: 0 ps  Iteration: 0  Instance: /testbench
# ------------------------------------------------------
#
# Congratulations! All data have been generated successfully!
#
# -------------------------PASS-------------------------
#
# ** Note: $finish    : E:/DCLab/102_2/MyExp/Exp2/exp2_rsa/testbench.v(175)
#    Time: 200927 us  Iteration: 1  Instance: /testbench
```

It is a fake "PASS"…

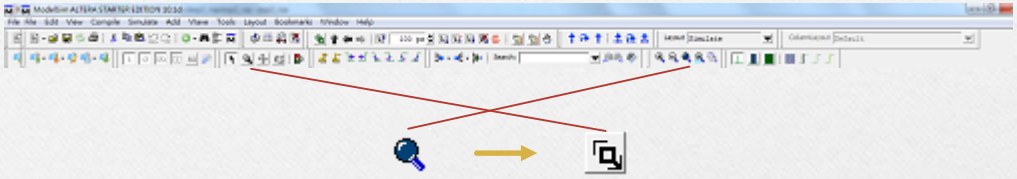
Change the Time Unit of the Timeline



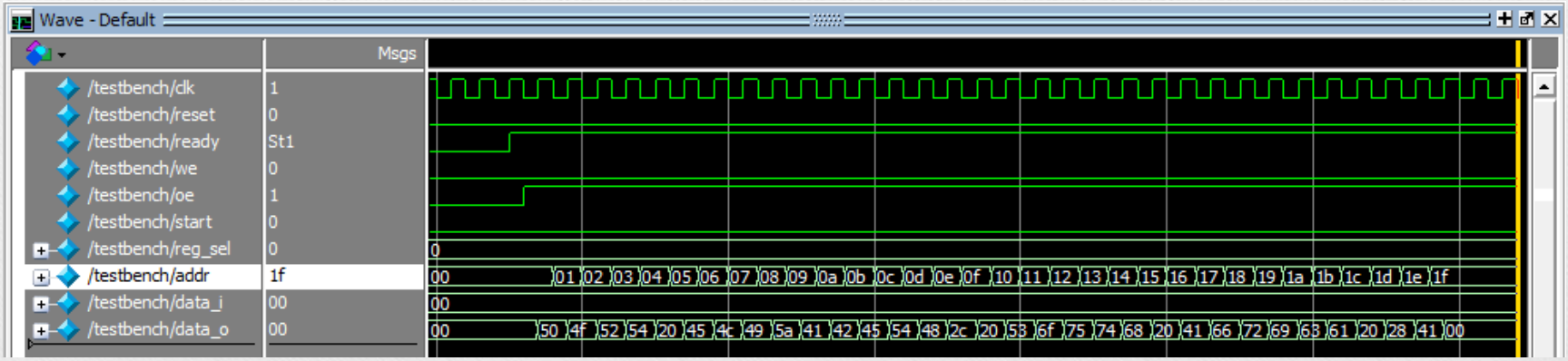
Check the Waveform (1/2)



Check the Waveform (2/2)



Zoom full Zoom Mode



How to see the signals in the design? Just try it!

The End.

Any question?

Reference

1. "DE2-115 User manual" by Terasic.
2. "THDB-HTG User Manual" by Terasic.
3. ModelSim® Tutorial by Mentor Graphics Corporation.
4. "Getting Started with Quartus II Simulation Using the ModelSim-Altera Software User Guide" by Altera.