From Low Power Fundamentals to SOC Low Power Design

Ke-Han Li

Graduate Institute of Electronic Engineering

National Taiwan University

2024/08/13

Outline

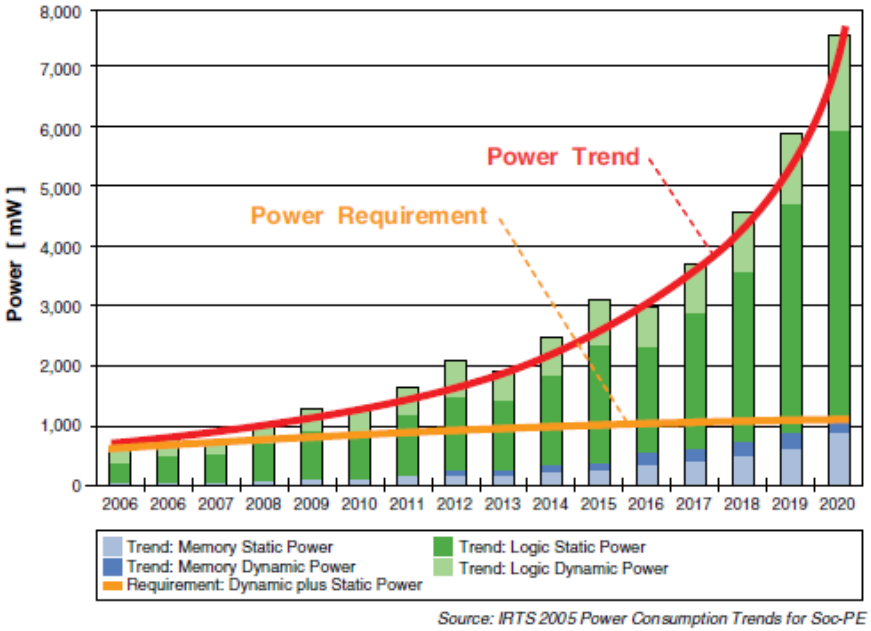
- Motivation
- Power Consumption
- Low Power Design Techniques
- Low Power Design Tools & Flow
- SOC Low Power Design

Outline

- **Motivation**
- Power Consumption
- Low Power Design Techniques
- Low Power Design Tools & Flow
- SOC Low Power Design

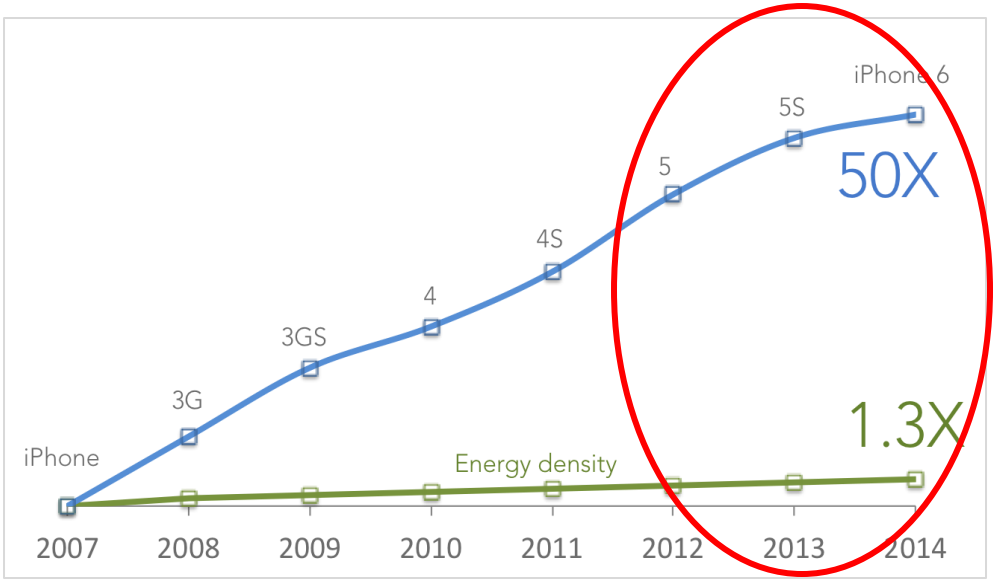
Motivation

CHIP's power increases year by year.



Source: IRTS 2005 Power Consumption Trends for Soc-PE

Battery capacity increases slowly due to physical limitations.



The gap is gradually widening!!!

Outline

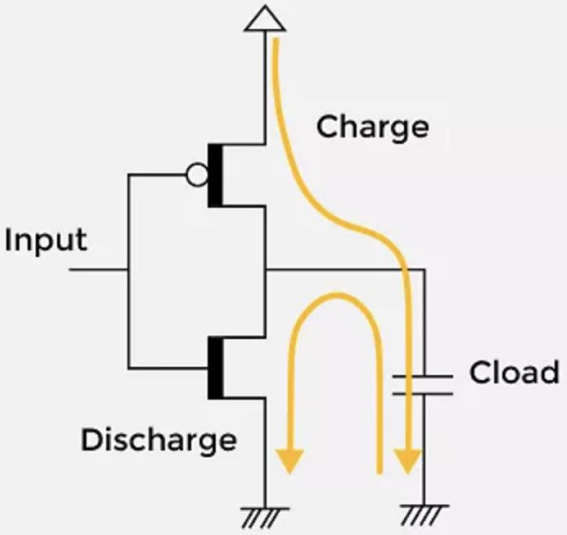
- Motivation
- **Power Consumption**
- Low Power Design Techniques
- Low Power Design Tools & Flow
- SOC Low Power Design

Power Components and Equation

$$P_{Total} = \alpha f C_L V_{DD}^2 + t_{sc} V_{DD} I_{peak} + V_{DD} I_{leakage}$$

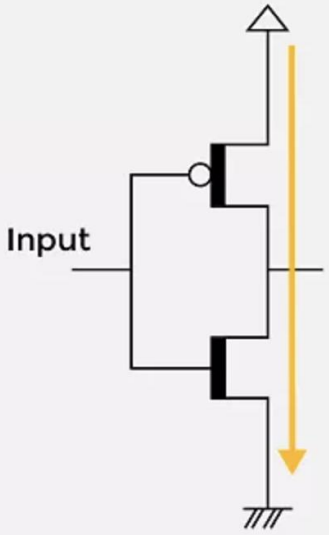
- α = activity factor (0 to 1)
- f = frequency
- t_{sc} = transition time
- C_L = capacitive load
- V_{DD} = supply voltage
- $I_{leakage}$ = leakage current
- I_{peak} = peak current

Input switching to '1' or '0'



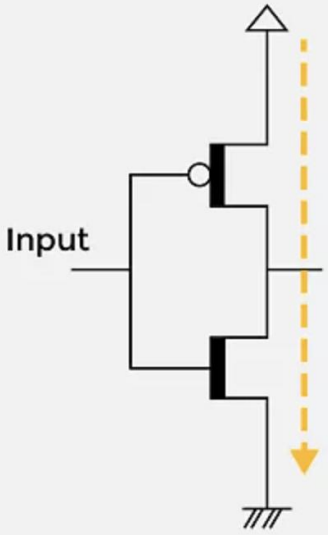
/ Dynamic Power

V<Input<VDD-1



/ Short Circuit Current

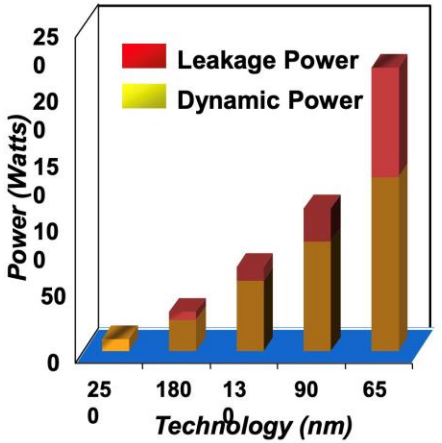
Input : '1' or '0' steady state

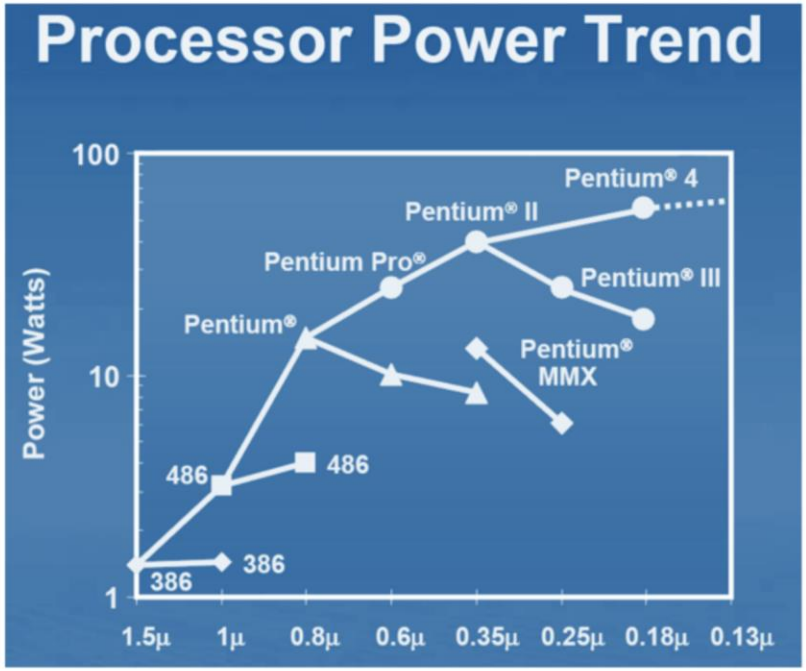


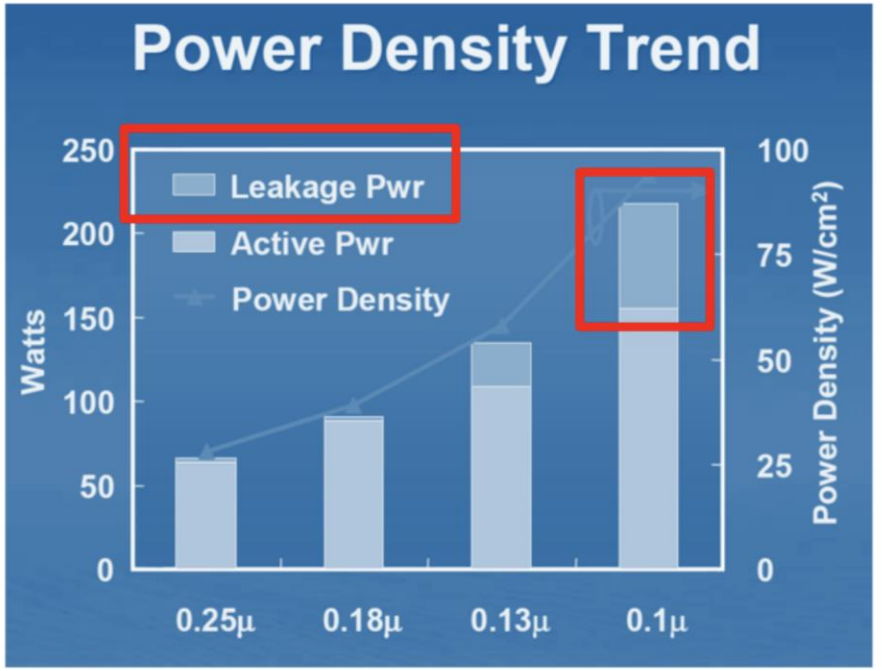
/ Leakage Current

Leakage Power Trend

- Leakage power gradually dominates the total power in advanced technology.







How to Reduce Power?

Dynamic Power | Static Power

$$P_{Total} = \alpha f C_L V_{DD}^2 + t_{sc} V_{DD} I_{peak} + V_{DD} I_{leakage}$$

- **Dynamic Power**
  - Reduce Area*(C_L)*
  - Slow clock & Turn off Clock*(f)*
  - Reduce Voltage*(VDD)*
  - Reduce Switching Activity(α)
- **Static Power**
  - OFF Power*(VDD)*
  - Reduce Voltage*(VDD)*
  - Increase Vt*(I_leak)*

α = activity factor (0 to 1)

f = frequency

t_{sc} = transition time

C_L = capacitive load

V_{DD} = supply voltage

$I_{leakage}$ = leakage current

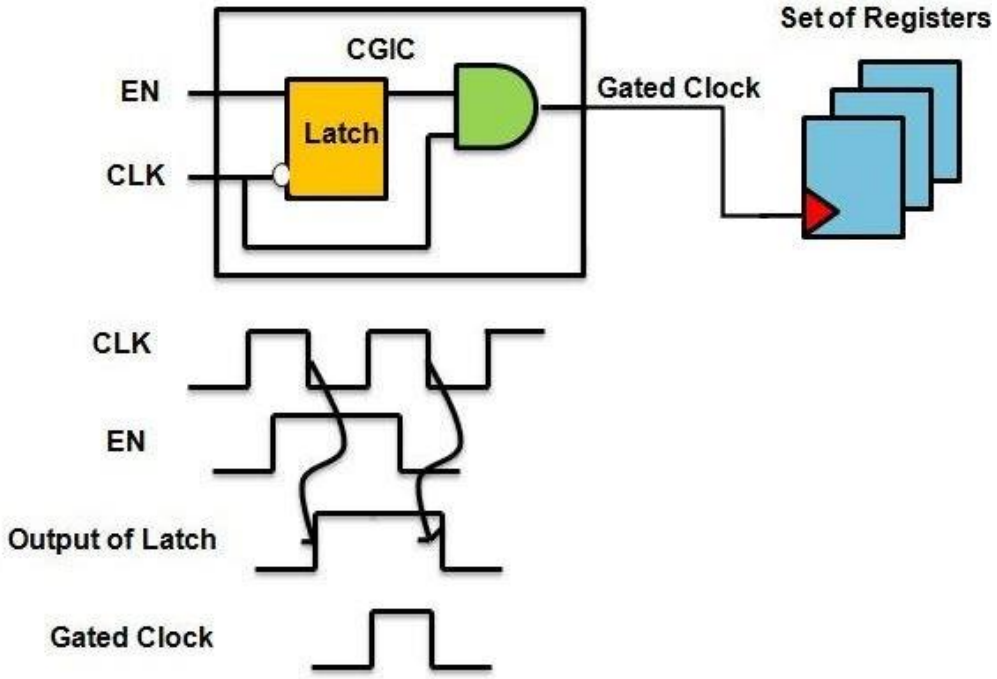
I_{peak} = peak current

Outline

- Motivation
- Power Consumption
- **Low Power Design Techniques**
- Low Power Design Tools & Flow
- SOC Low Power Design

Clock Gating

- Turn off the clock, when not use
- Scope: From module-level(TOOL) to sub-system level(Manual)



Clock Gating (Auto CG)

- If Statement

```
always@(posedge clk) begin
    if (enable) Q <= D_in;
    else Q <= Q;
end
```

- Conditional Assignment

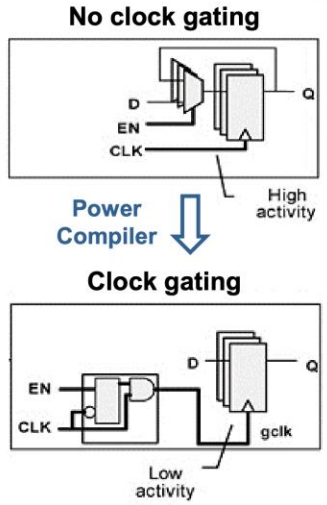
```
always@(posedge clk) begin
    Q <= (enable)? D_in:Q;
end
```

- Clock gating script style 1

```
insert_clock_gating
compile
```

- Clock gating script style 2

```
compile -gate_clock
```



Clock Gating (Manual)

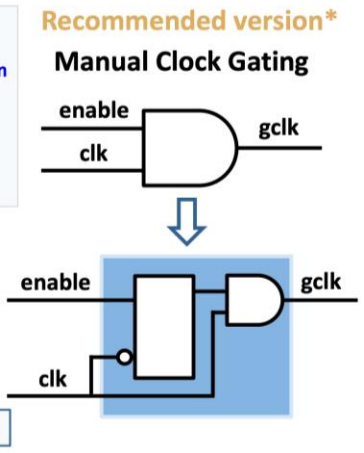
```
Reg [7:0] Data_out;
assign gclk = clk & enable;
always@(posedge gclk or negedge rst_n) begin
    if (!rst_n)
        Data_out <= 8'd0;
    else
        Data_out <= Data_out + 8'd1;
end
```

- Clock gating script

```
replace_clock_gates
compile
```

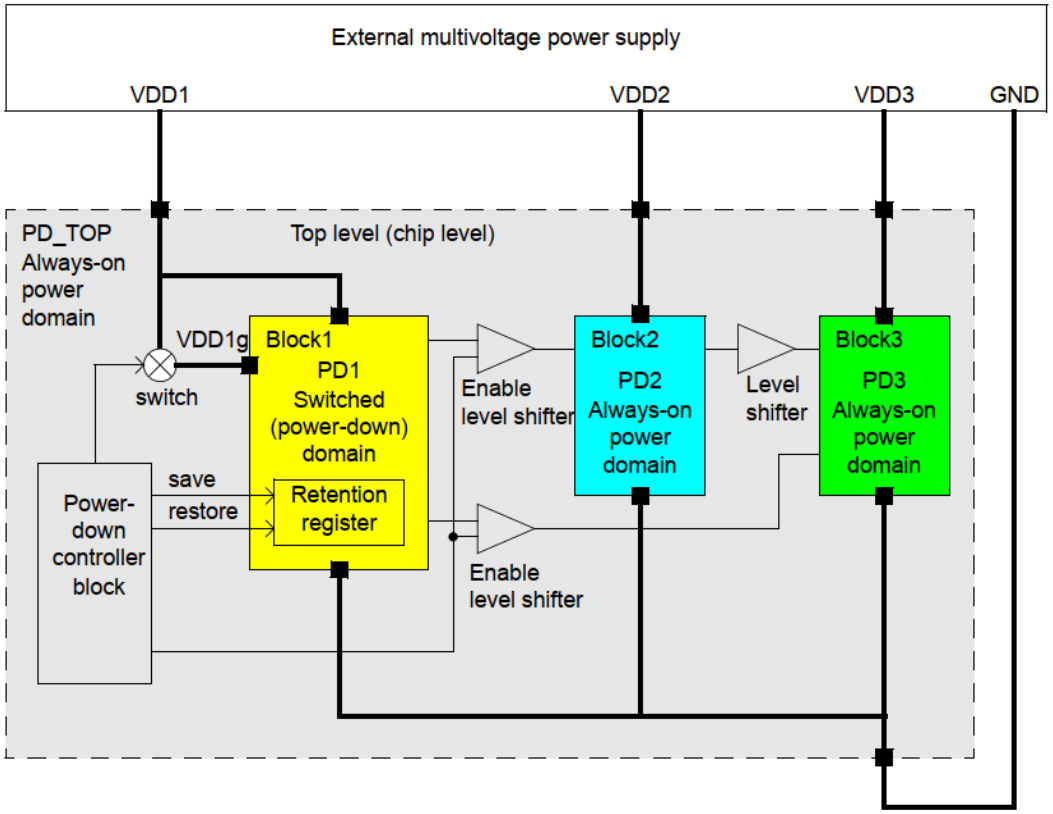
- Report clock gating

```
report_clock_gating -gating_elements
```



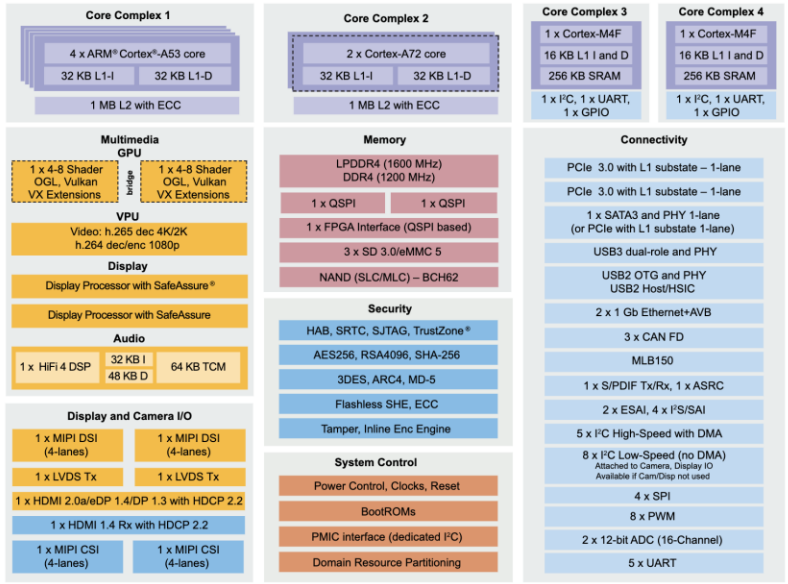
Multi-VDD

- Each sub-system requires the different voltage.



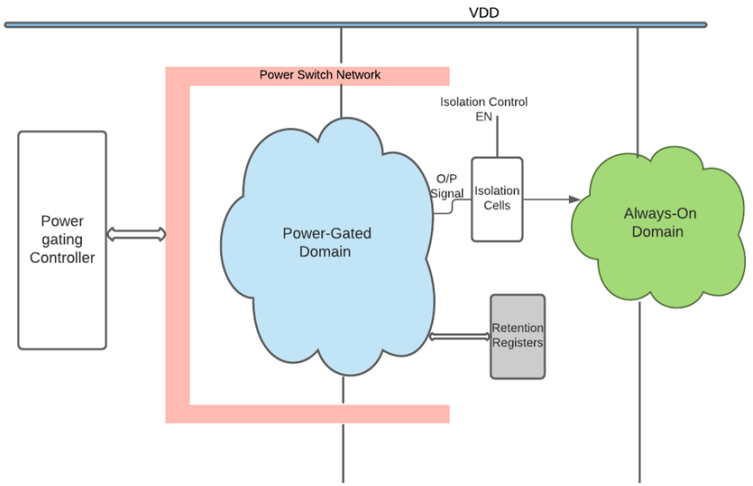
High Performerce(CPU, GPU...) -> High VDD

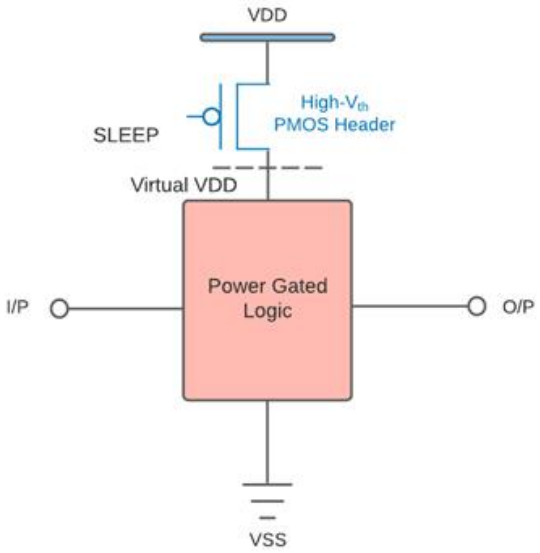
Normal Performance(Sec., Audio...) -> Low VDD

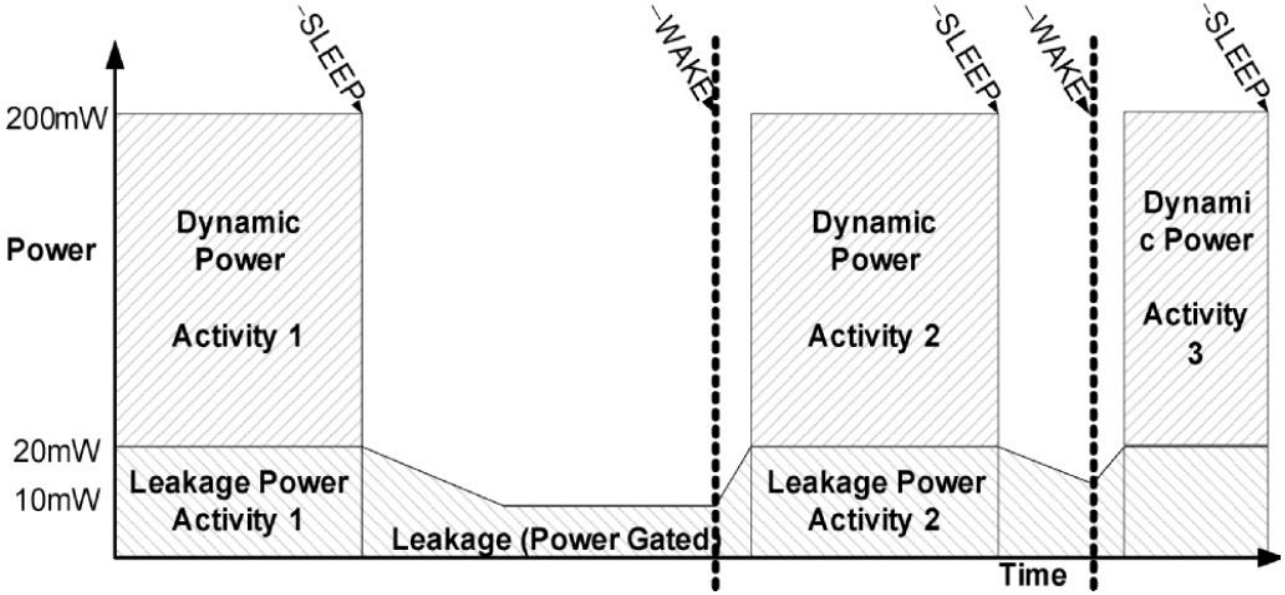


Power Gating

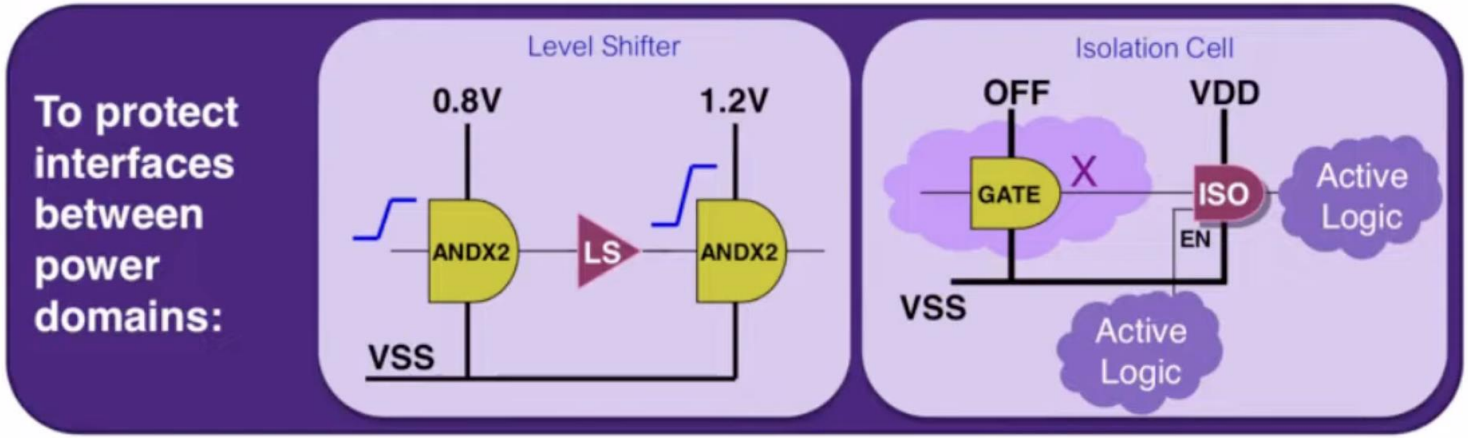
- Turn off the power, when not use
- Required special low power cells

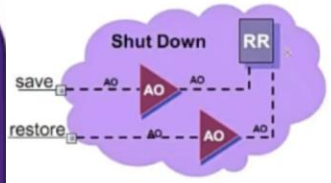


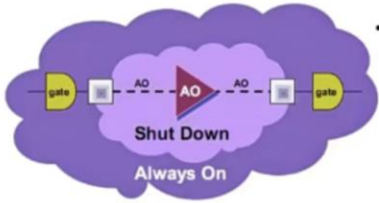




Special Low Power Cell

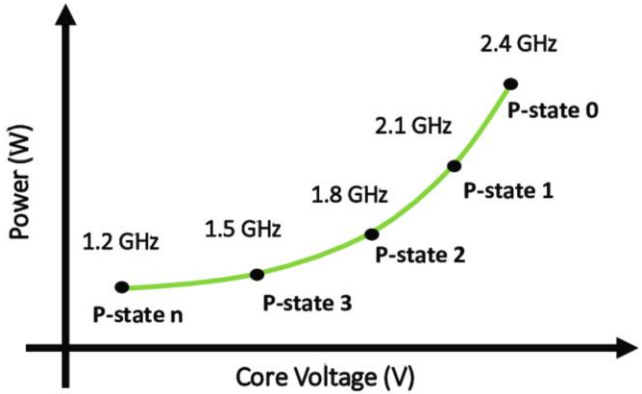






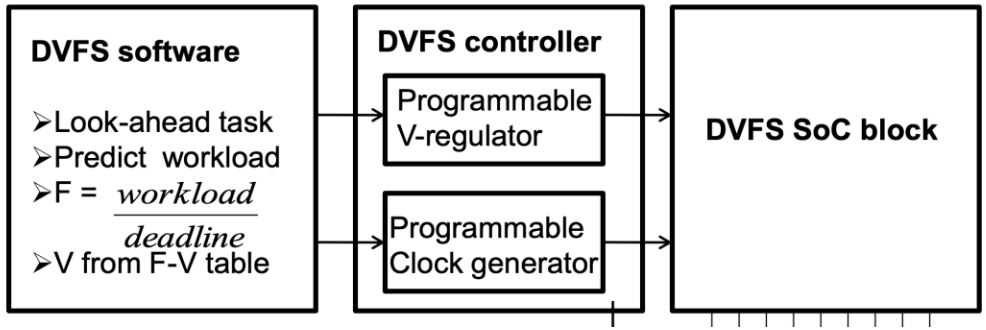
Dynamic Voltage and Frequency Scaling(DVFS)

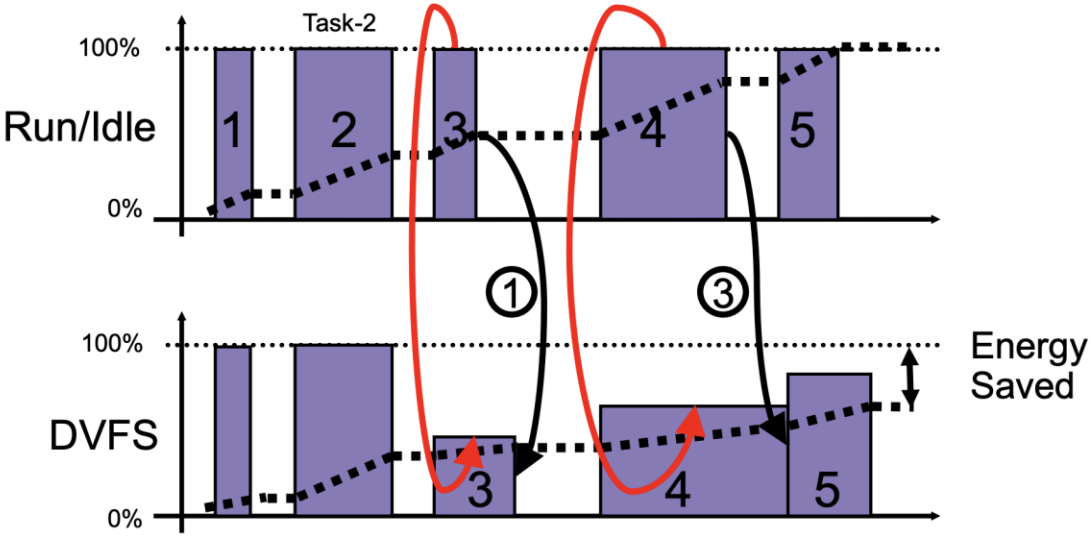
- Adjust V and F to run just fast enough to meet the task



AMD Turion MT-34

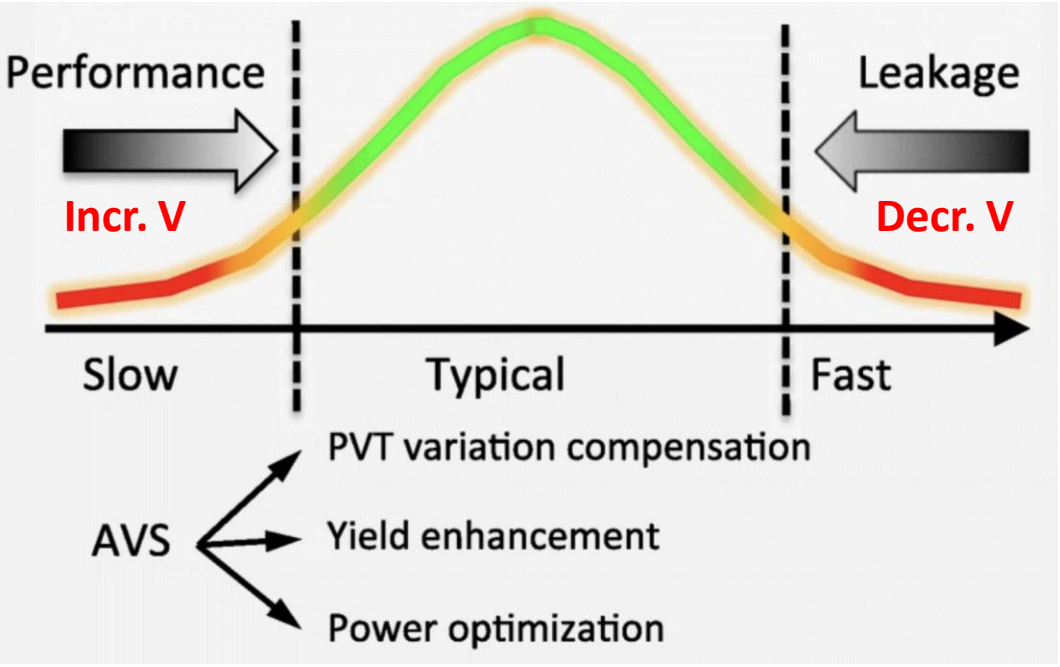
Frequency	Voltage	Power
0.8 GHz	0.90 V	6.25 W
1.0 GHz	1.00 V	9.65 W
1.2 GHz	1.05 V	12.76 W
1.4 GHz	1.10 V	16.34 W
1.6 GHz	1.15 V	20.41 W
1.8 GHz	1.20 V	25.00 W

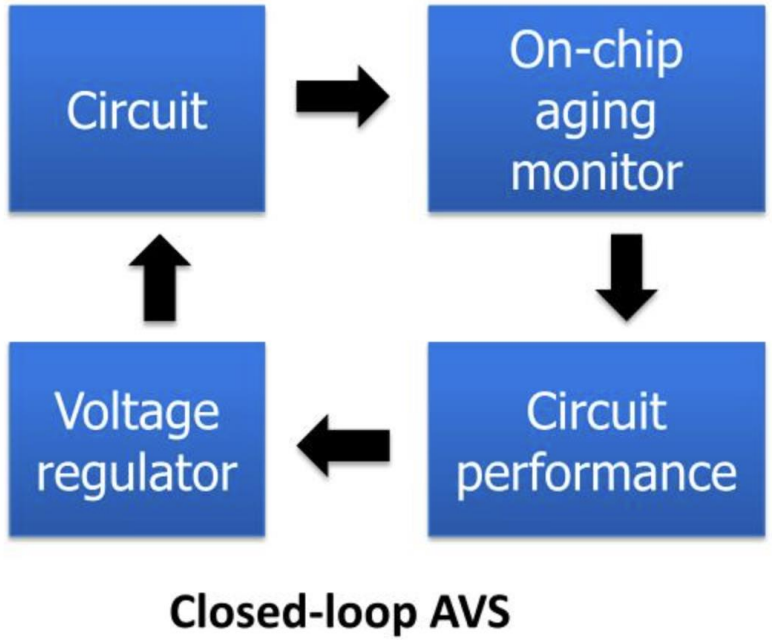




Adaptive voltage frequency scaling (AVS)

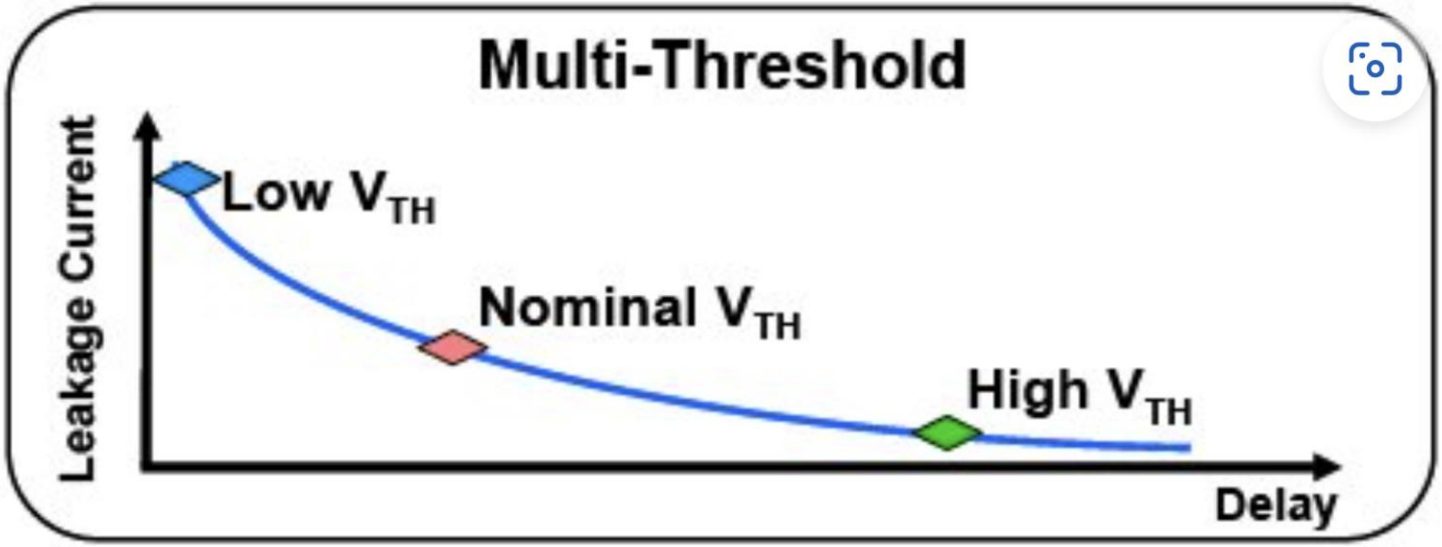
- Adjusts the voltage to match the chip's minimum requirement.
  - based on on-chip performance monitor
- Close-loop system for process and temperature compensation





Multi-Vt Cell

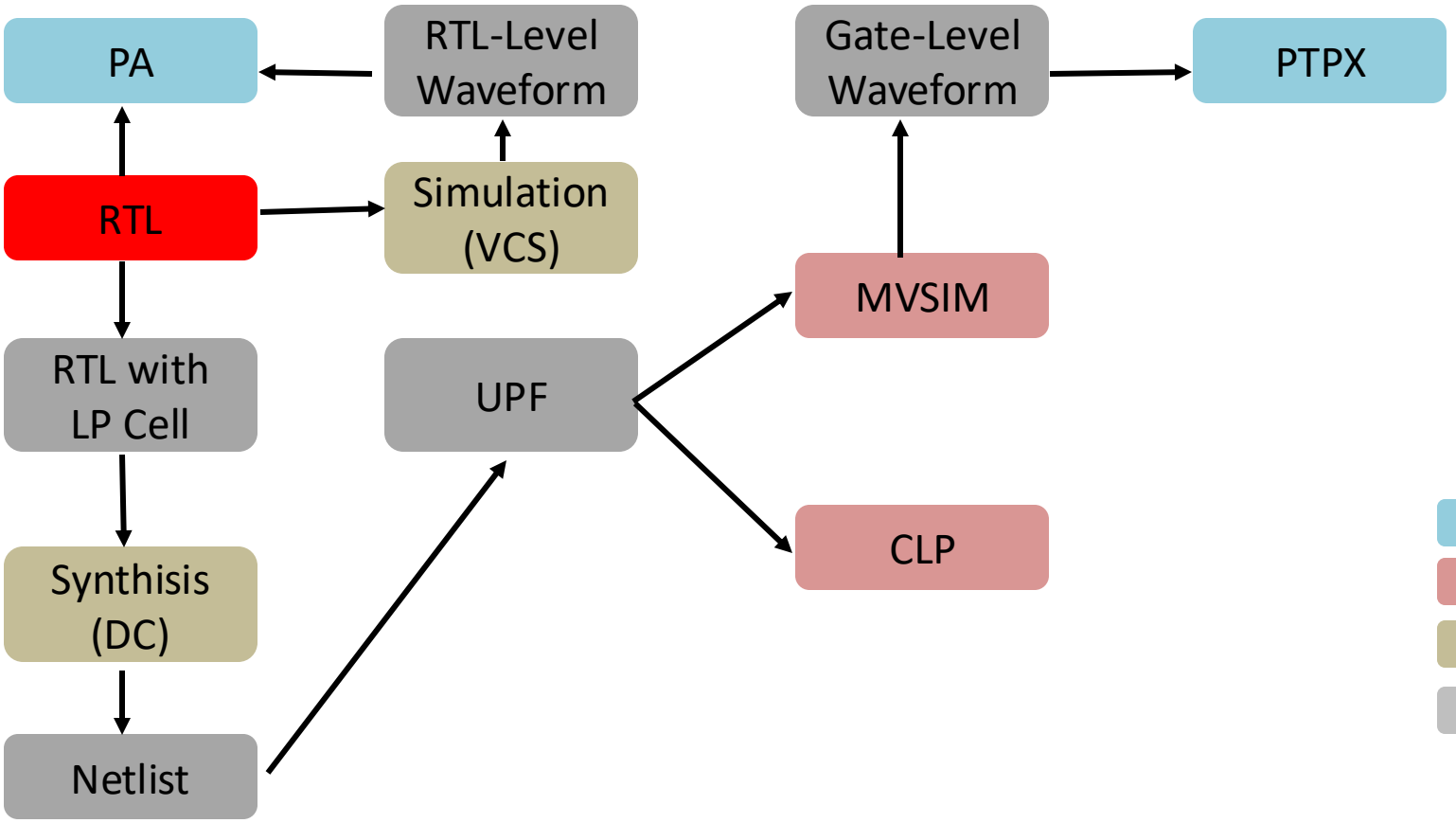
- Low Vt -> Critical Path -> Better Performance
- High Vt -> Non-Critical Path -> Save Power
- Cell selection will be automatically implemented by synthesis tool.



Outline

- Motivation
- Power Consumption
- Low Power Design Techniques
- **Low Power Design Tools & Flow**
- SOC Low Power Design

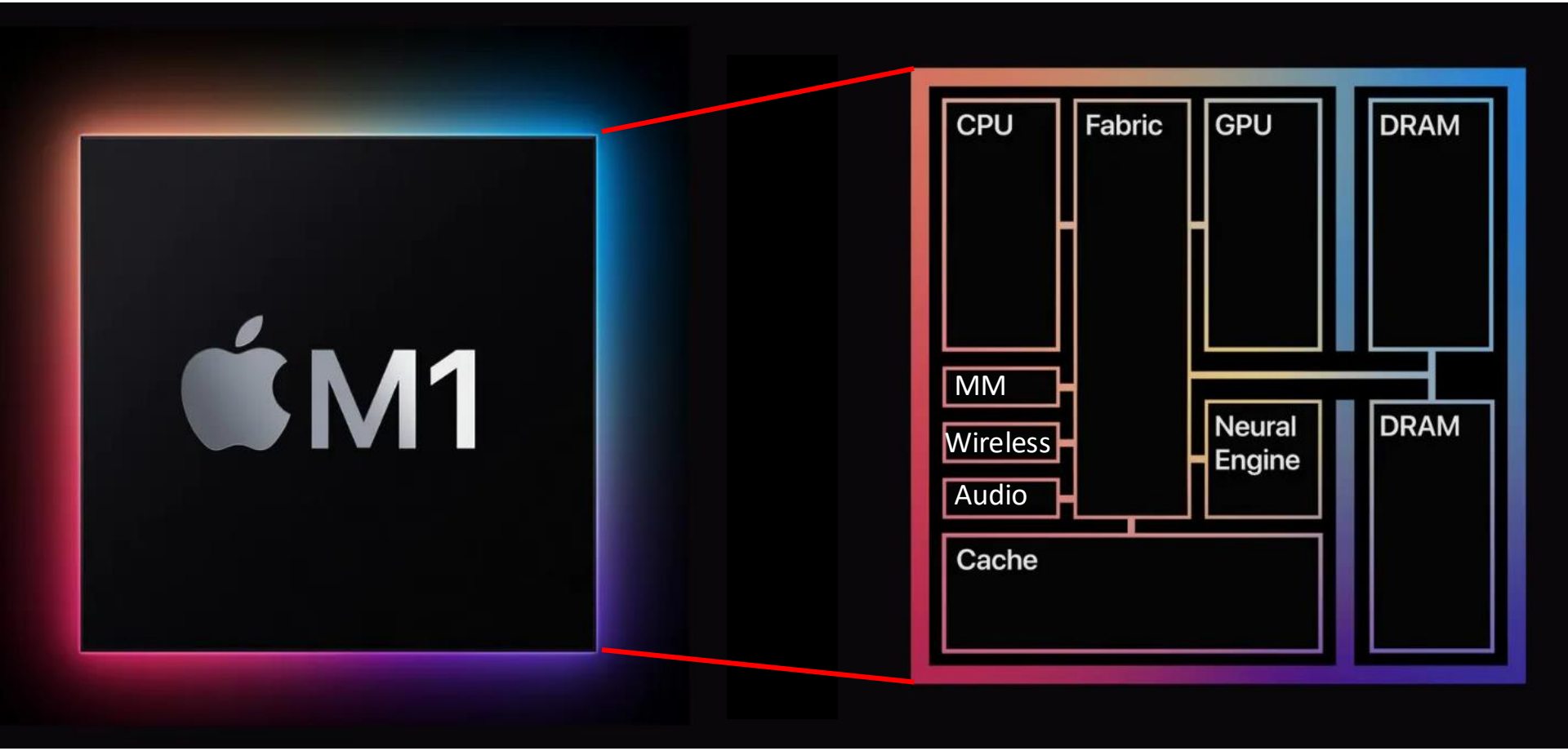
Low Power Design & Verification Flow



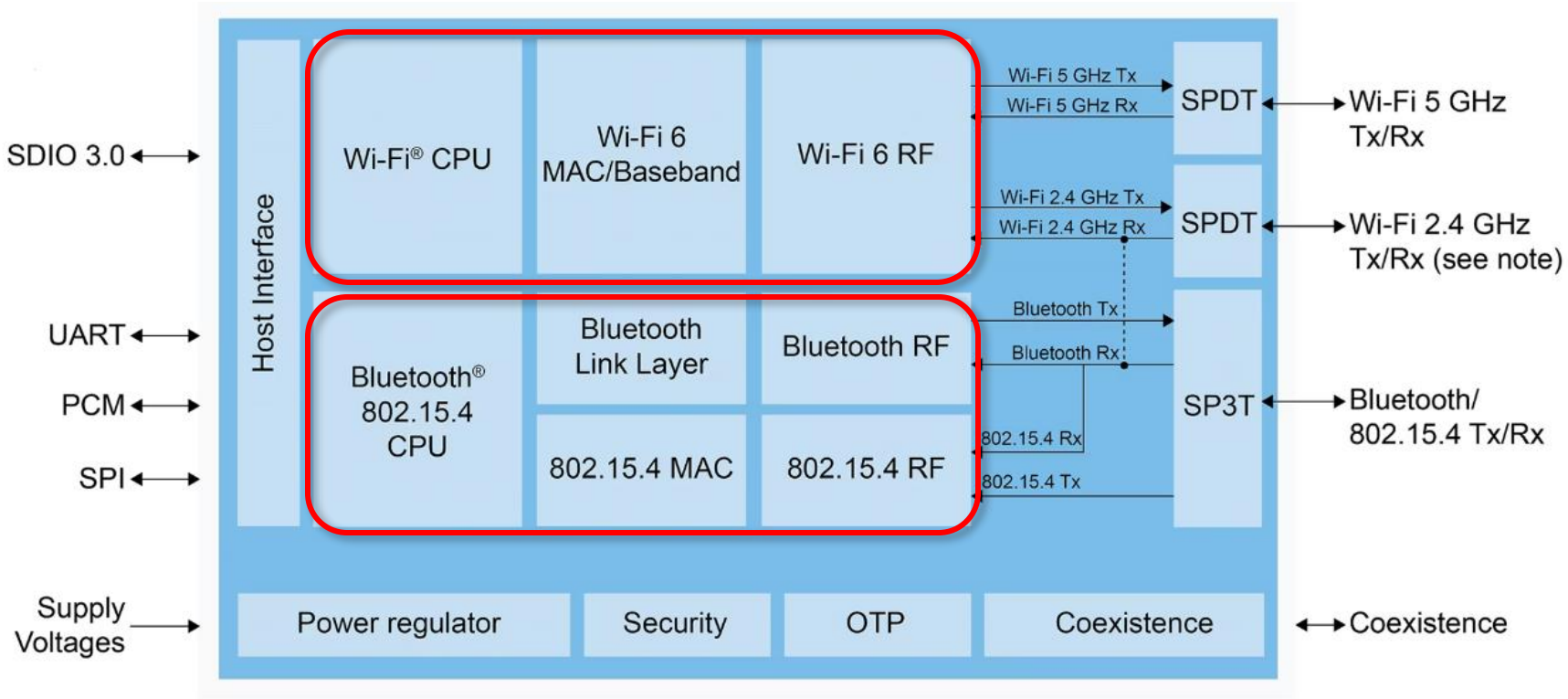
Outline

- Motivation
- Power Consumption
- Low Power Design Techniques
- Low Power Design Tools & Flow
- **SOC Low Power Design**

Apple M1 SOC

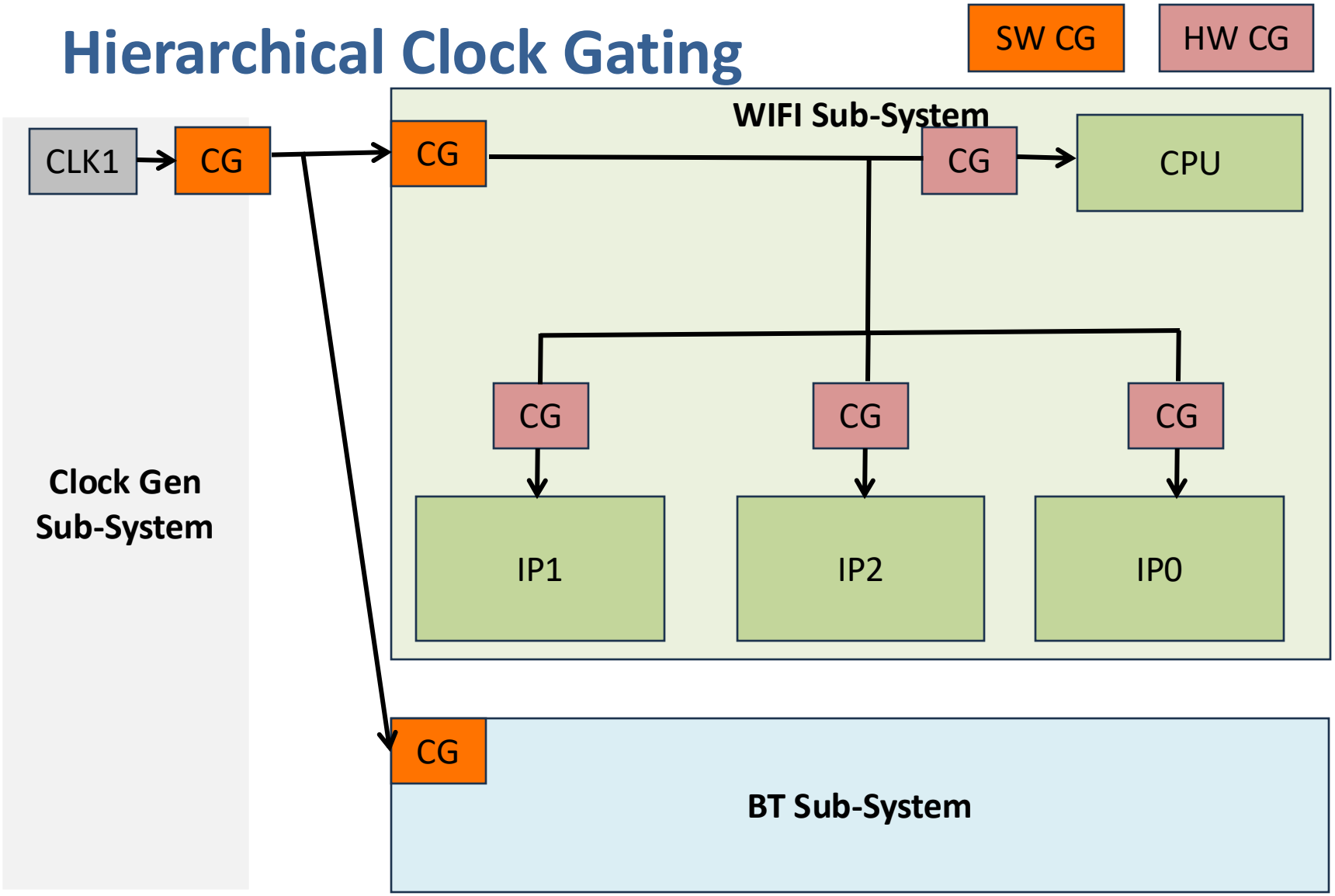

M1
CPU
Fabric
GPU
DRAM
MM
Wireless
Audio
Neural Engine
DRAM
Cache

Wireless Sub-System



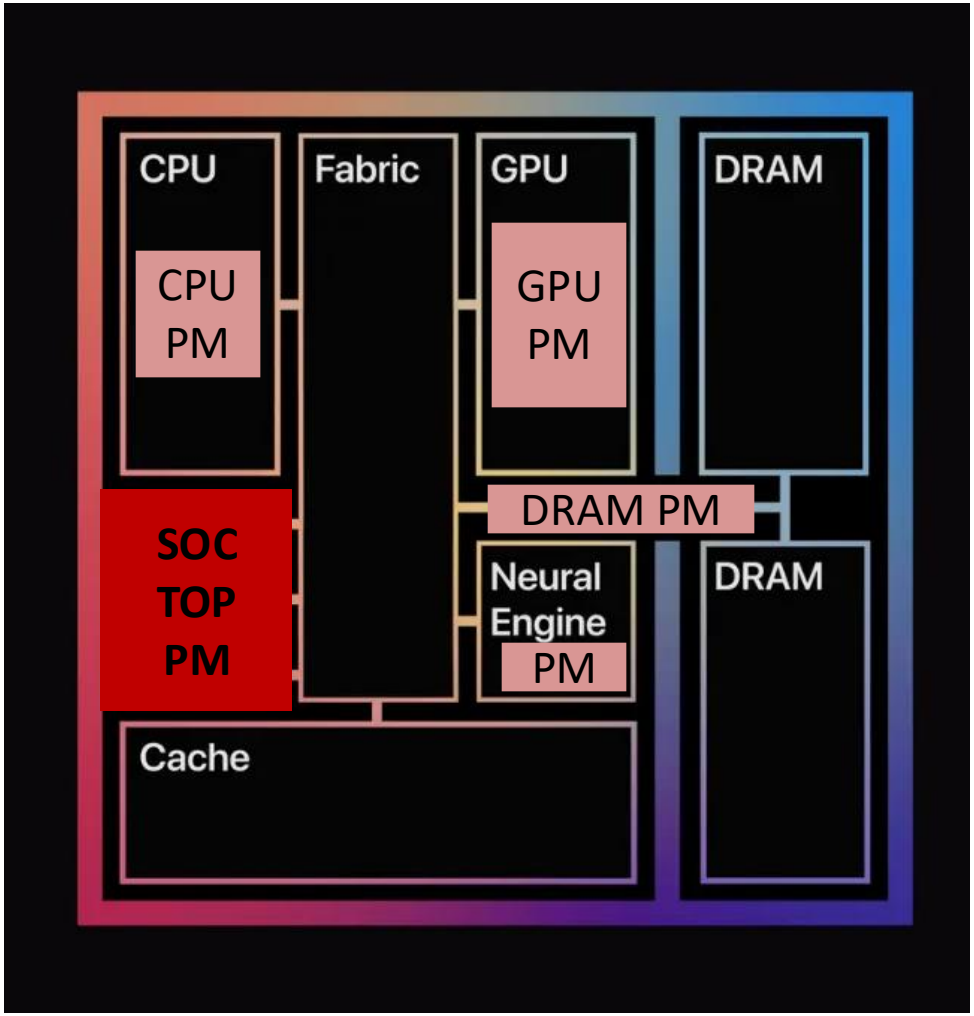
Note: Optional simultaneous receive path between Wi-Fi, Bluetooth, and 802.15.4

Hierarchical Clock Gating



Hierarchical Power Gating

Hierical Low Power Control



References

- What is Low Power Design? – Techniques, Methodology & Tools | Synopsys
- upf low power 1.1 (youtube.com)
- https://zhuanlan.zhihu.com/p/47483274
- The Ultimate Guide to Power Gating - AnySilicon
- Low-Power IC Design: Techniques and Best Practices (ansys.com)
- Galaxy Low Power Solution (synopsys.com)
- Qnovo | I WANT MORE BATTERY CAPACITY IN MY SMARTPHONE

END