DesignWare IP

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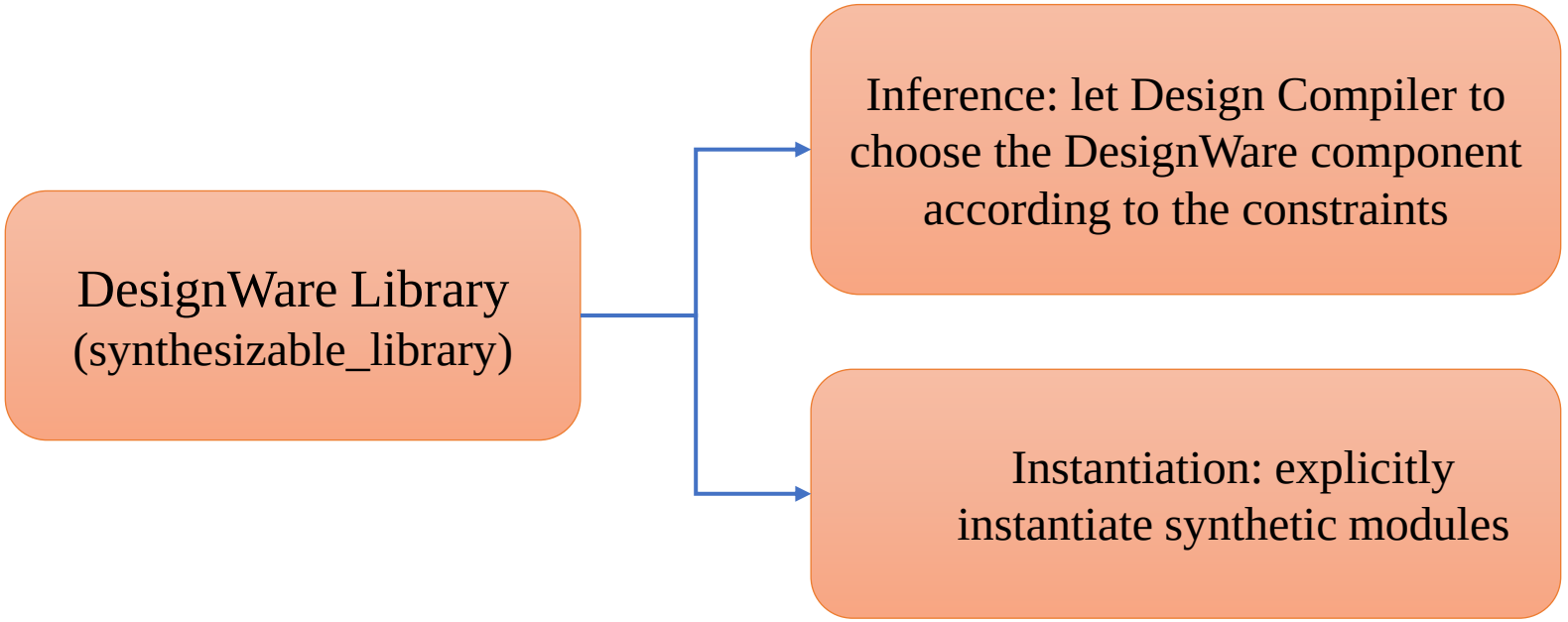
Introduction

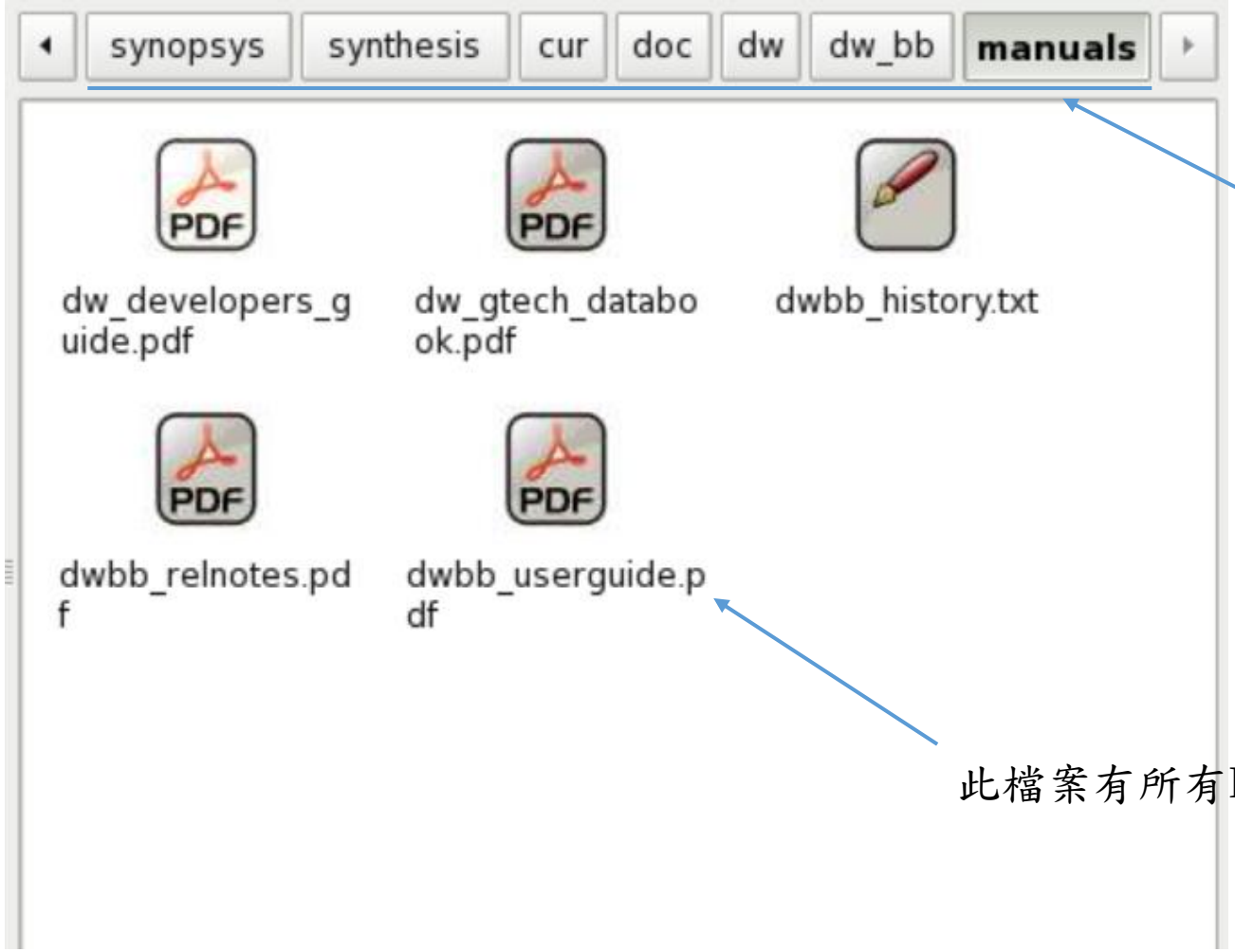
- DesignWare為design compiler附帶的IP元件庫，安裝design compiler時會一並下載
- DesignWare Library分為兩種模式



Introduction

- Inference:使用於可以直接打出來的，Ex. + - * / % (無須額外操作)
- Instantiation:用在如sin, cos, square root等無法直接打出來的(操作方式如後)

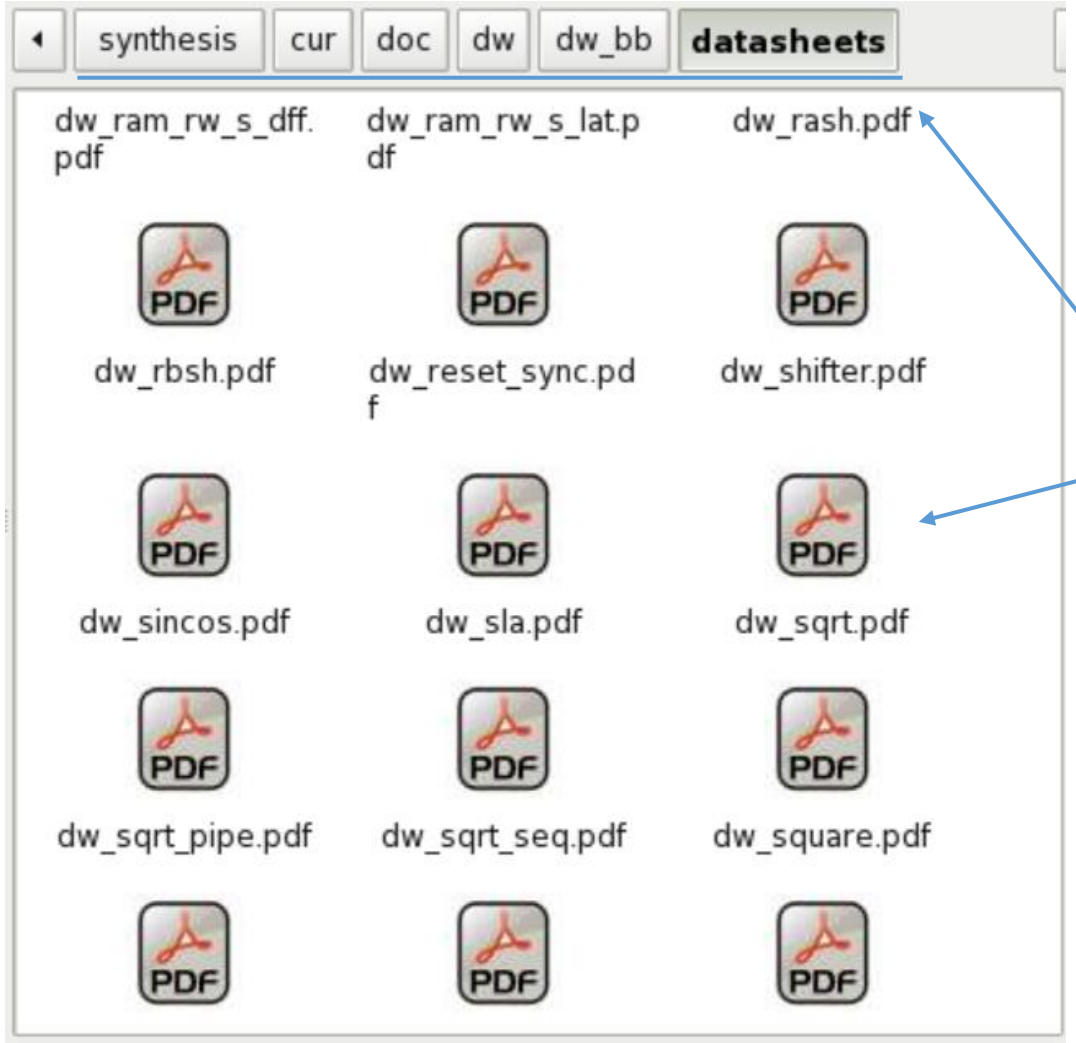
Instantiation DesignWare Component



位置可能有所不同

此檔案有所有DesignWare的IP總覽

Instantiation DesignWare Component



此處可以找到每一個IP的細節描述，接下來會用根號為例

Instantiation DesignWare Component

Table 1-4 Simulation Models

Model	Function
DW02.DW_SQRT_CFG_SIM	Design unit name for VHDL simulation
dw/dw02/src/DW_sqrt_sim.vhd	VHDL simulation model source code
dw/sim_ver/DW_sqrt.v	Verilog simulation model source code

點即進入上一頁ppt中的pdf可以找到相關檔案的存放位置

HDL Usage Through Component Instantiation - Verilog

```
module DW_sqrt_inst (radicand, square_root);
  parameter radicand_width = 8;
  parameter tc_mode        = 0;

  input  [radicand_width-1 : 0]       radicand;
  output [(radicand_width+1)/2-1 : 0] square_root;
  // Please add +incdir+$SYNOPSYS/dw/sim_ver+ to your verilog simulator
  // command line (for simulation).

  // instance of DW_sqrt
  DW_sqrt #(radicand_width, tc_mode)
    U1 (.a(radicand), .root(square_root));
endmodule
```

Pdf內有教如何引入該IP的module到自己的code內

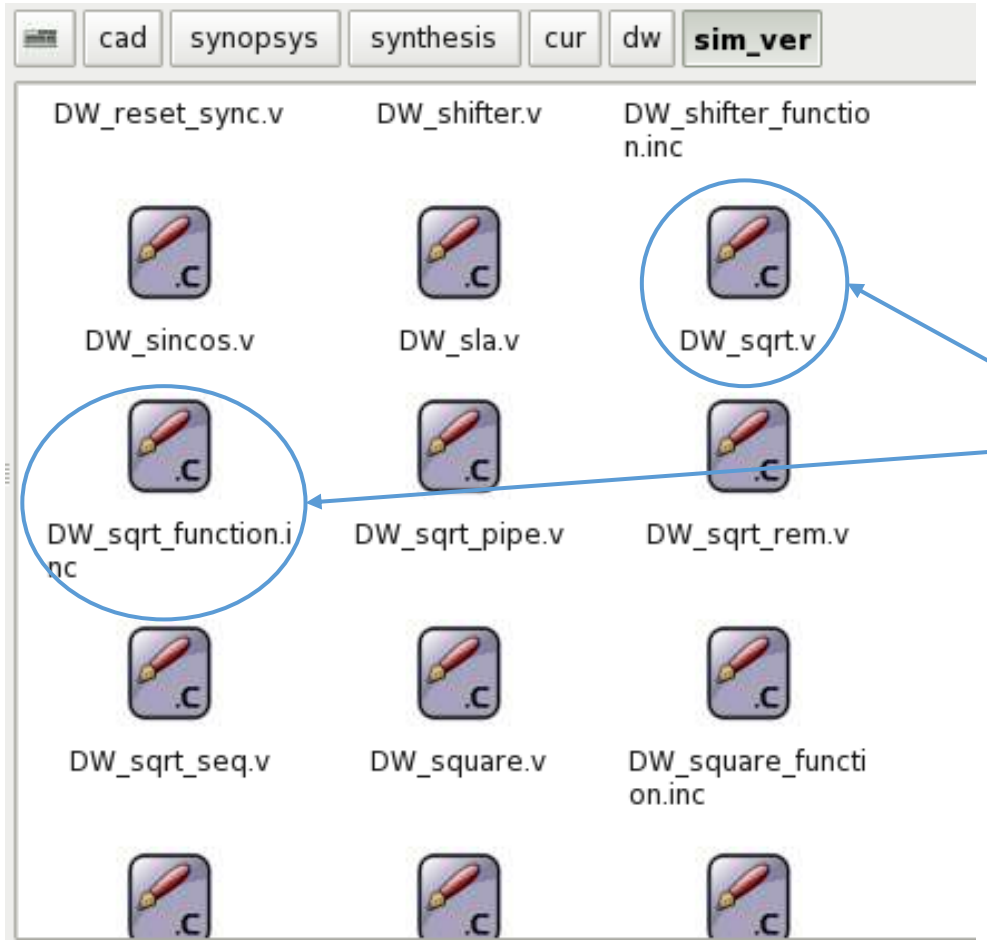
Instantiation DesignWare Component

HDL Usage Through Function Inferencing - Verilog

```
module DW_sqrt_func (radicand, square_root_uns, square_root_tc);

  parameter radicand_width = 8;

  input  [radicand_width-1 : 0]       radicand;
  output [(radicand_width+1)/2-1 : 0] square_root_uns;
  output [(radicand_width+1)/2-1 : 0] square_root_tc;

  // pass the "func_width" parameter to the inference functions
  parameter width = radicand_width;

  // Please add search_path = search_path + {synopsys_root + "/dw/sim_ver"}
  // to your .synopsys_dc.setup file (for synthesis) and add
  // +incdir+$SYNOPSYS/dw/sim_ver+ to your verilog simulator command line
  // (for simulation).
  `include "DW_sqrt_function.inc"

  // function calls for unsigned/signed square root
  assign square_root_uns = DWF_sqrt_uns (radicand);
  assign square_root_tc  = DWF_sqrt_tc (radicand);

endmodule
```

pdf內有該IP的code可以瀏覽，若內部有include某個.inc檔案，則抓取.v檔時也要一並抓取，此.inc位置與.v位置相同

Instantiation DesignWare Component



以上一頁的圖片為例，這兩個檔案都要取得

Simulation

- 可以直接將DesignWare的.v及.inc拉出來加入ncverilog跑RTL simulation
- 另一種方法為使用下面的指令

```
Unix% ncverilg testfixture.v your_design.v
      -y /cad/synopsys/synthesis/cur/dw/sim_ver/ +libext+.v
      +incdir+/cad/synopsys/synthesis/cur/dw/sim_ver/+
```

將所有需要使用的.v檔拉進來

跑RTL simulation才需要加

將所有需要使用的.inc檔拉進來

- 跑design compiler及presim不須額外動作