SoC Verification

Shao-Yi Chien

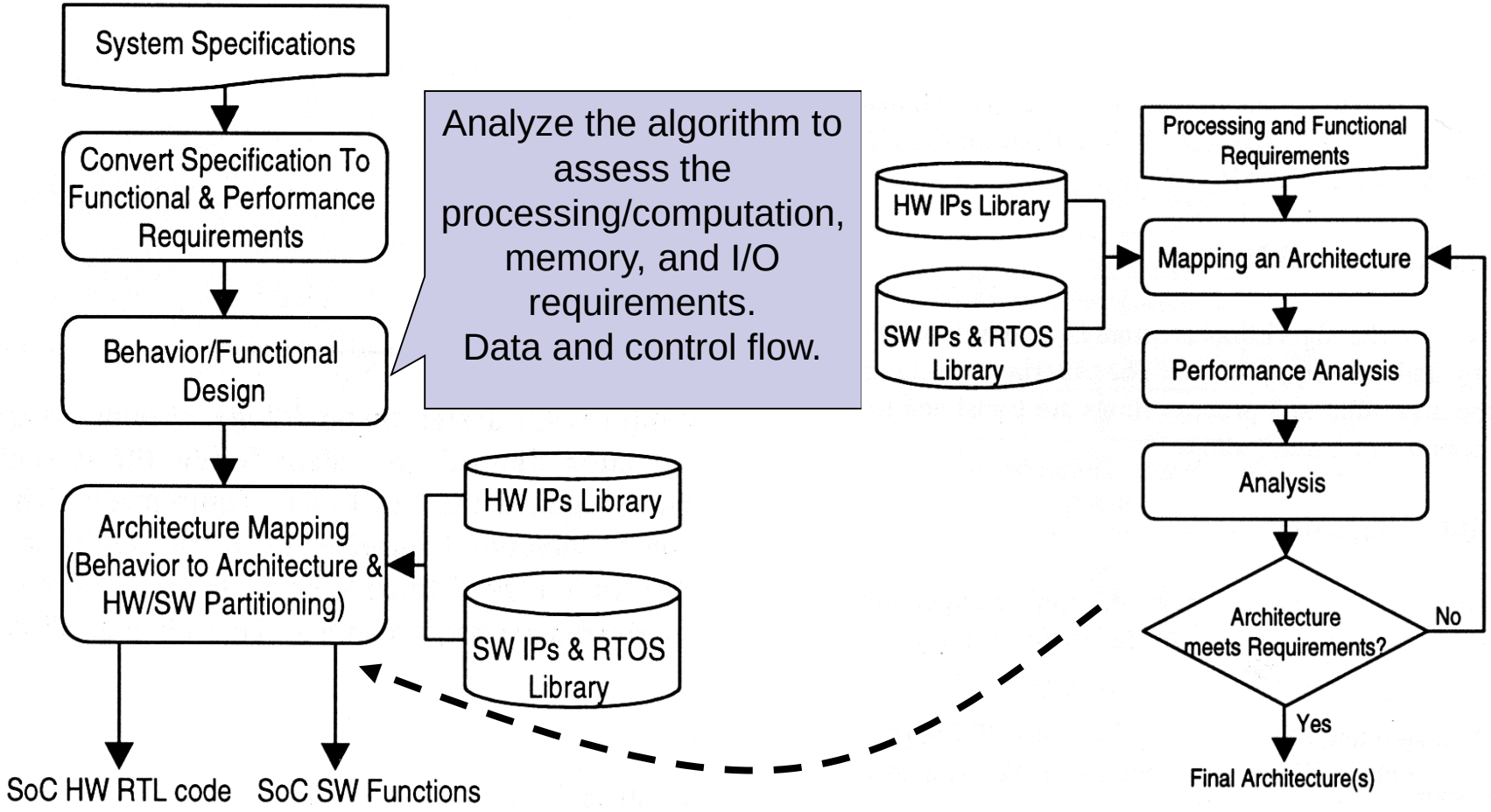
Ref:

1. P. Rashinkar, P. Paterson, and L. Singh, “Chap. 2: System-Level Verification,” *System-on-a-chip Verification*, Kluwer Academic Publishers, 2001.
2. P. Rashinkar, P. Paterson, and L. Singh, “Chap. 6: Hardware/Software Co-verification,” *System-on-a-chip Verification*, Kluwer Academic Publishers, 2001.

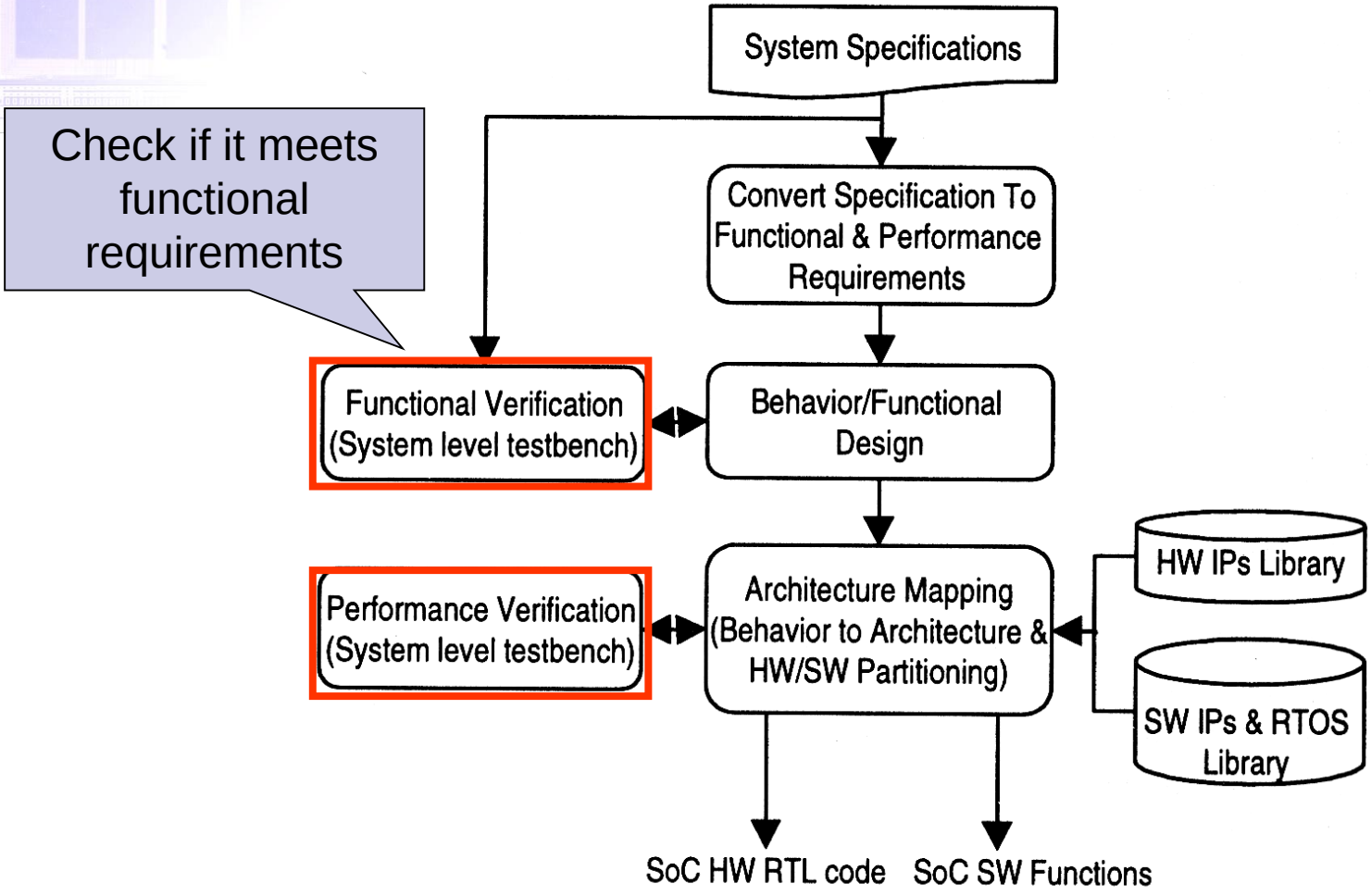
Outline

- System design
- System verification
  - Hardware/software co-verification
  - Rapid prototyping

System Design



System Verification

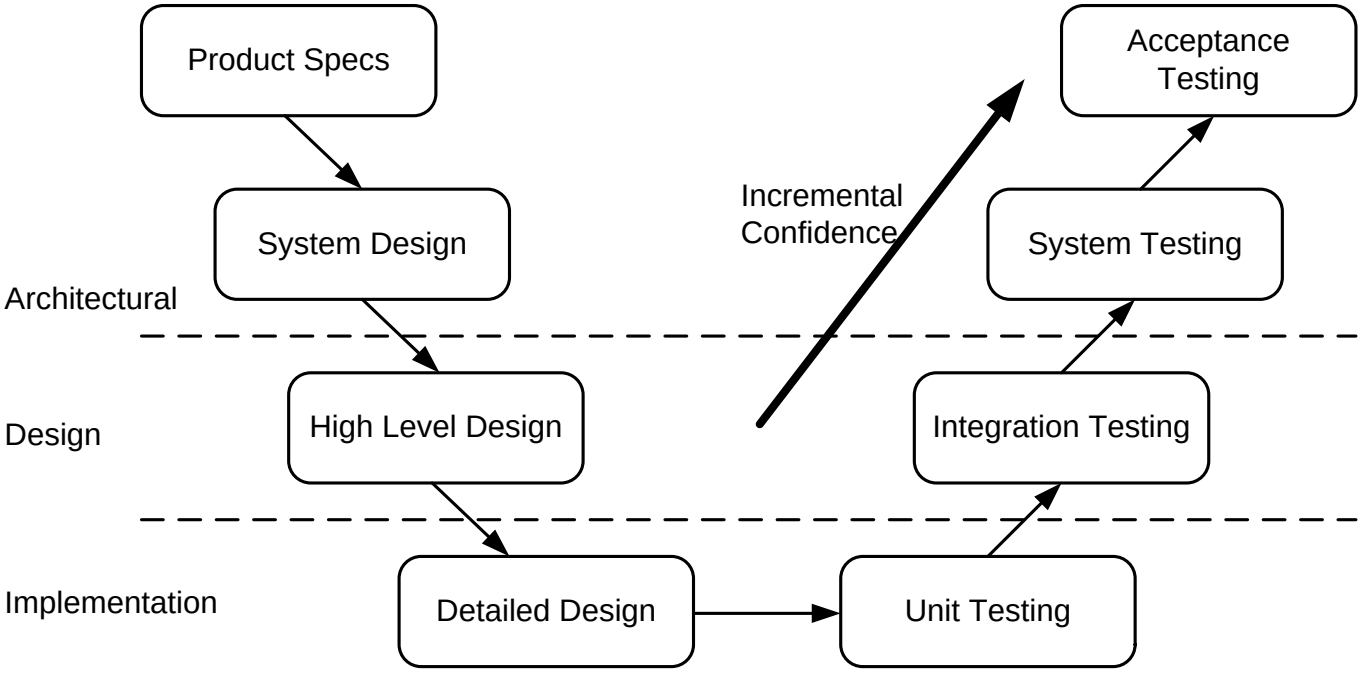


System Verification

- V-shaped model: top-down and bottom-up implementation approach
- Create a system-level testbench
  - System testbench metrics
- Emulation
- Hardware acceleration
- Hardware modeling
- Mixed-level simulation
- Design partitioning

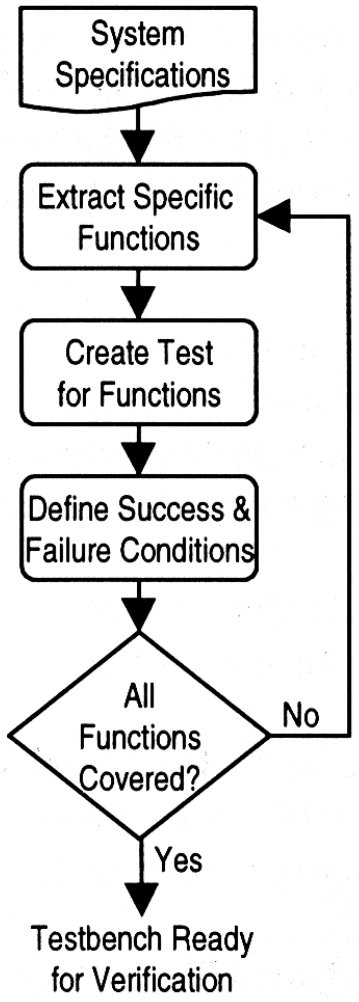
V-Shaped Model

- Top-down and bottom-up implementation approach



Create a System-Level Testbench

- Explicit and implied functionalities
- For example:
  - Data packet (xyz) will appear on port A
  - No illegal bus cycles are generated
  - Memory location (xyz) contains value (AB) on completion of the test
  - Variable (A) goes active during the execution of the test
  - Variable (A) does not go active during the execution of the test
- Pay particular attention to
  - Corner cases
  - Boundary conditions
  - Design discontinuities
  - Error conditions
  - Exception handling



System Testbench Metrics

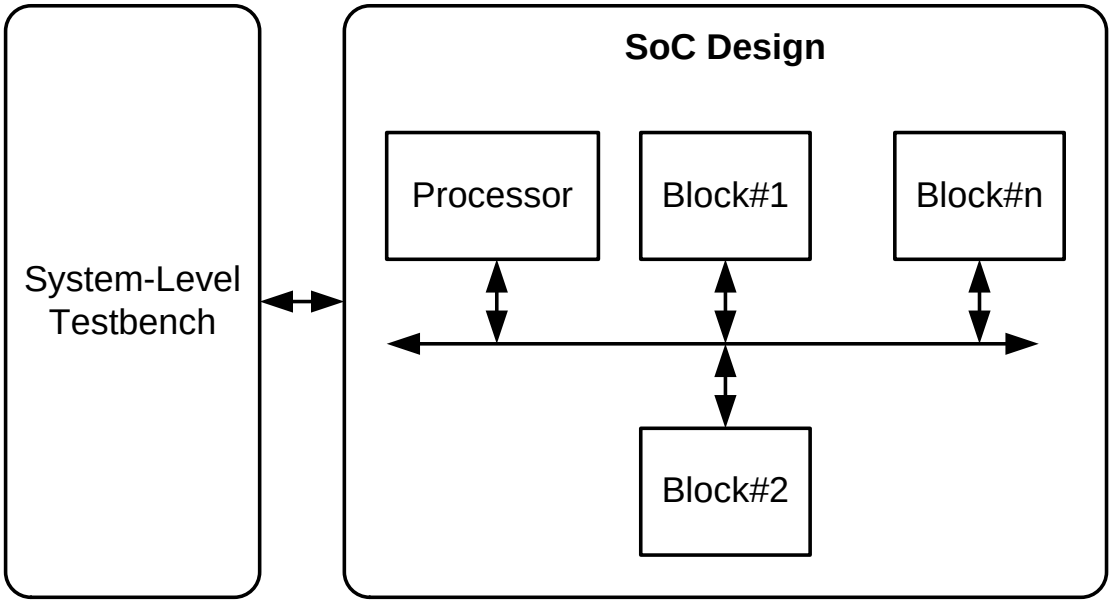
- Whether or not all of the test defined in the verification plan are included
  - A qualitative measure
  - How to define and measure functional coverage is still a problem
- When possible, test all possible combinations of transactions with all possible data sets

Big Challenge for SoC Verification: High Gate Count

- The number of gates on an SoC device increases
- The size of the system-level testbench required to test the SoC exhaustively grows exponentially
- Software simulation cannot keep up with this exponential growth

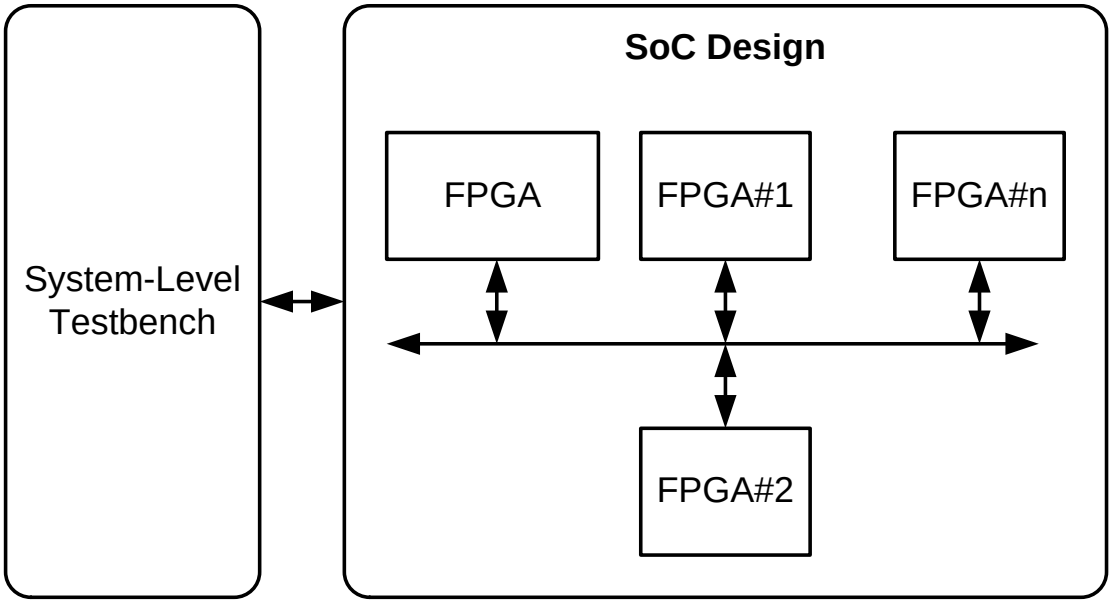
Some Verification Strategies (1)

- Example



Some Verification Strategies (2)

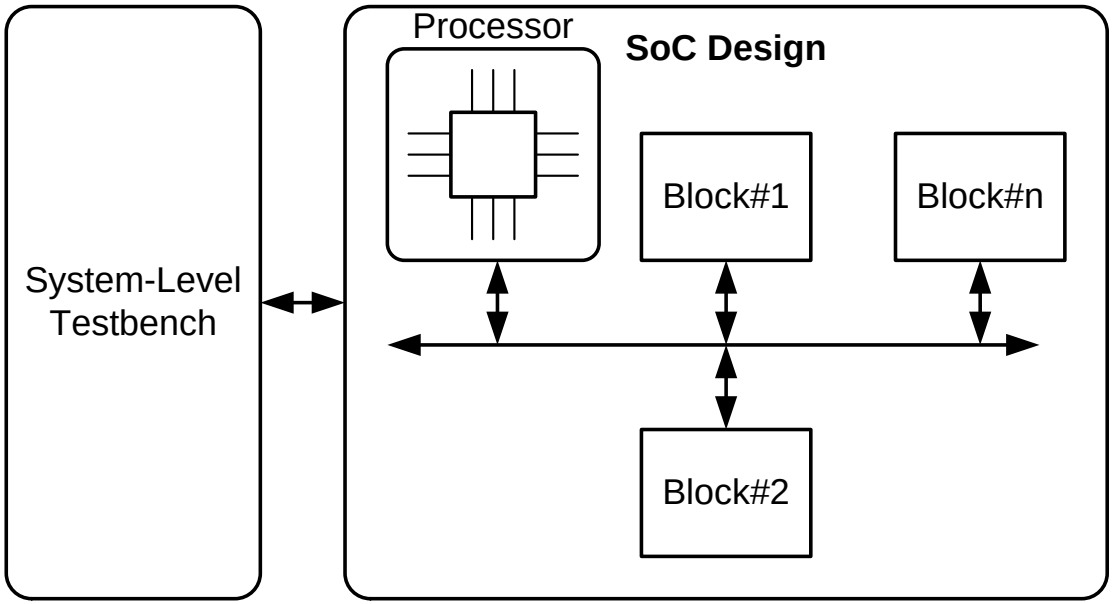
- Emulation



- Hardware accelerator

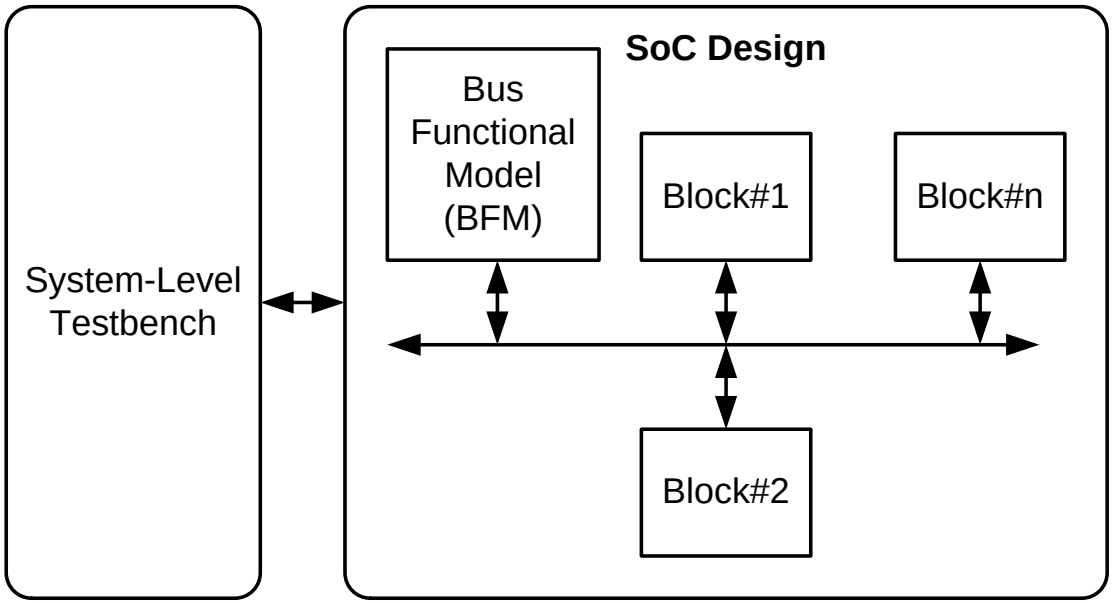
Some Verification Strategies (3)

- Hardware modeling
  - Ex: with a processor bounded core



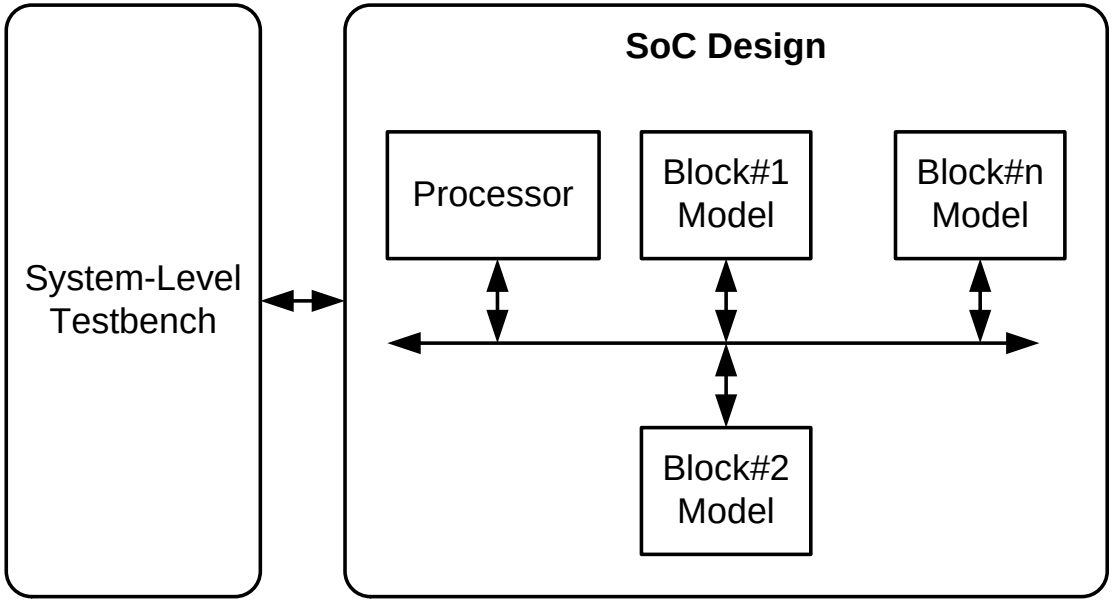
Some Verification Strategies (4)

- Mixed-Level Simulation
  - Single complex block



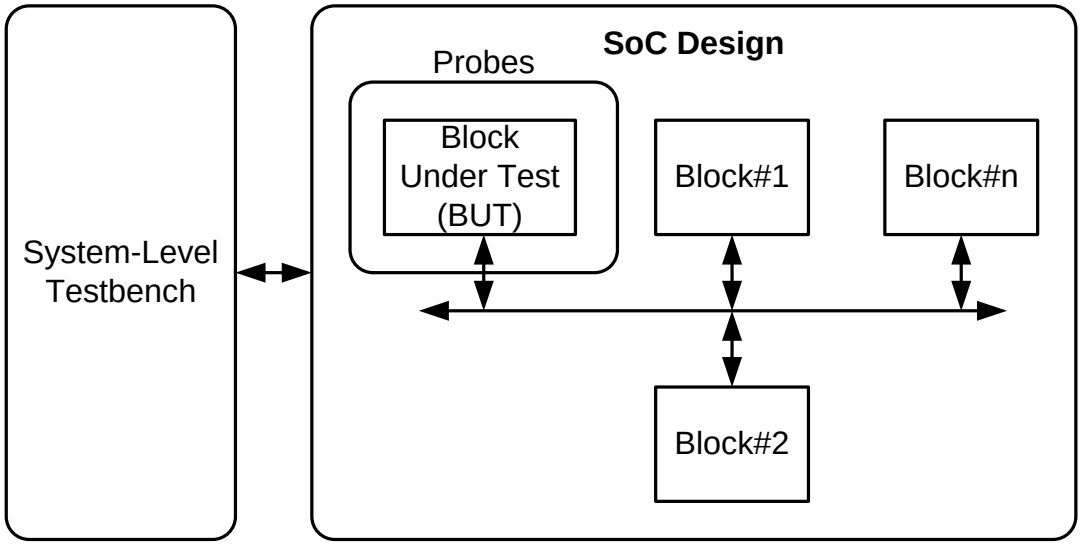
Some Verification Strategies (5)

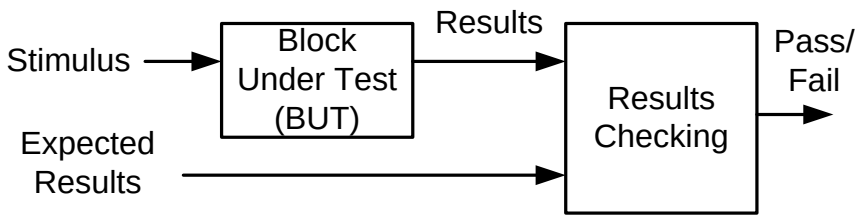
- Mixed-Level Simulation
  - Many complex block: verify one block at a time



Some Verification Strategies (6)

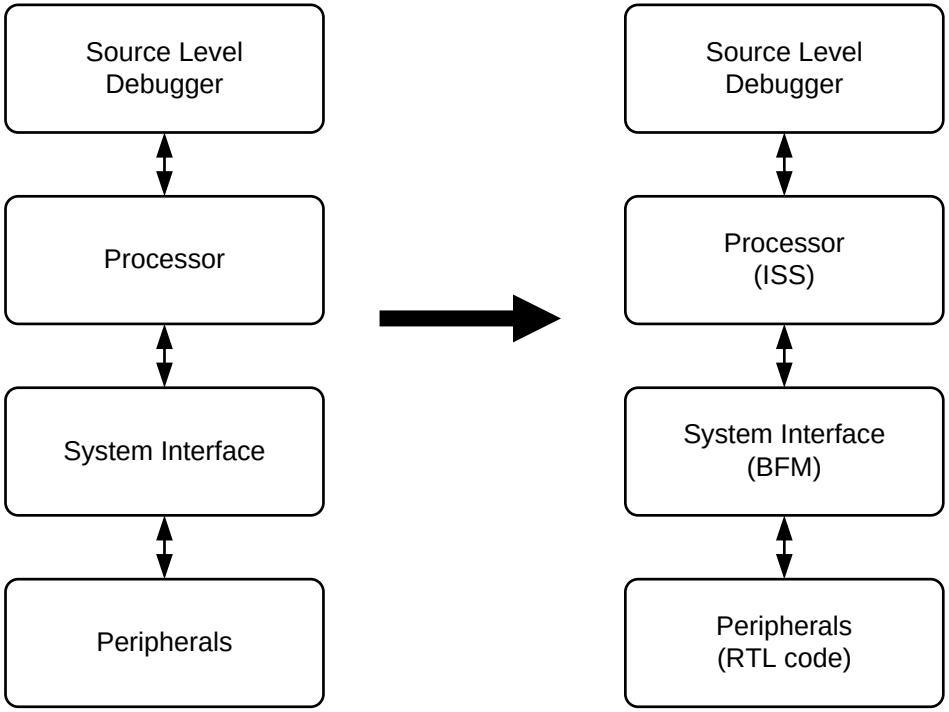
- Design partitioning
  - Can significantly reduce the simulation requirements to verify the entire SoC design





Hardware/Software Co-verification

- HW/SW Co-verification environment



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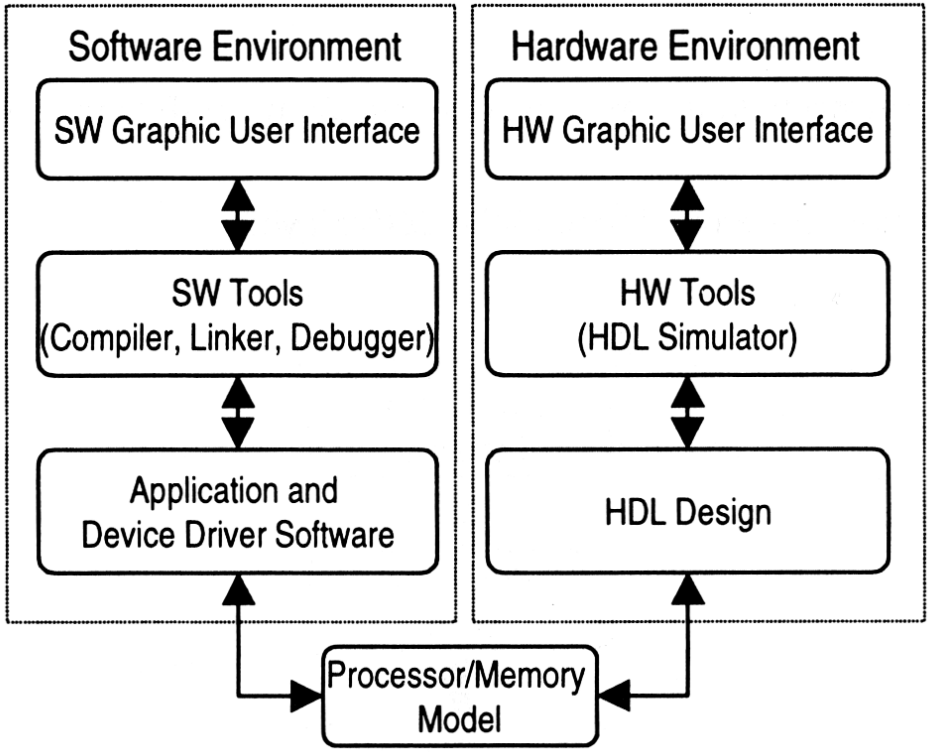
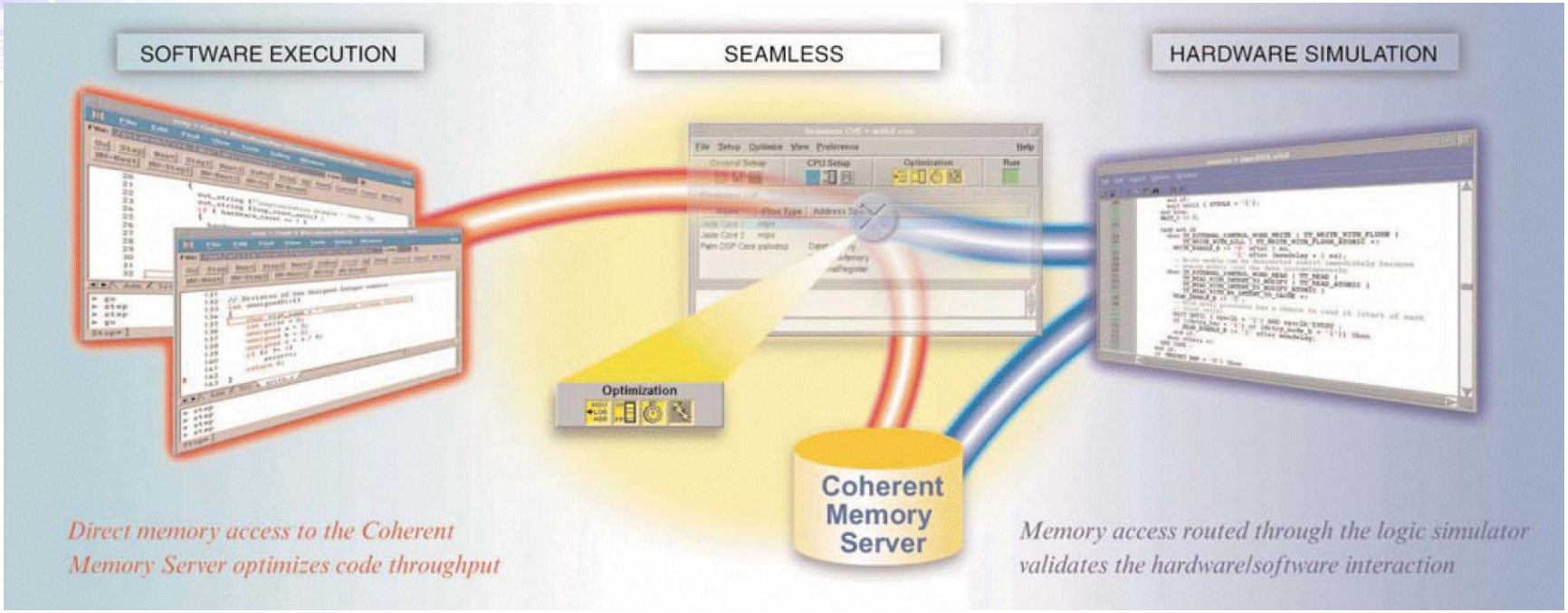


Mentor Graphics Seamless CVE



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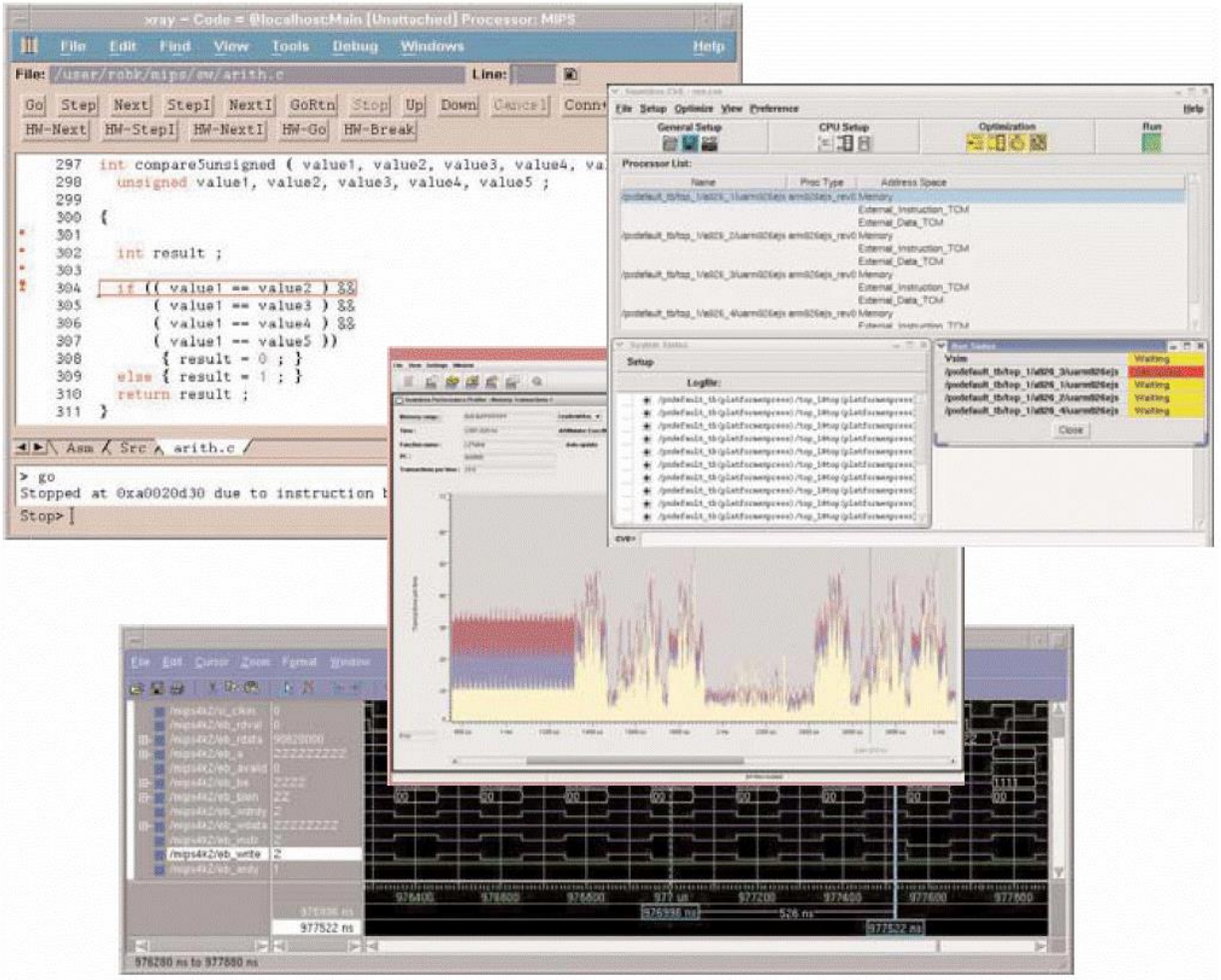
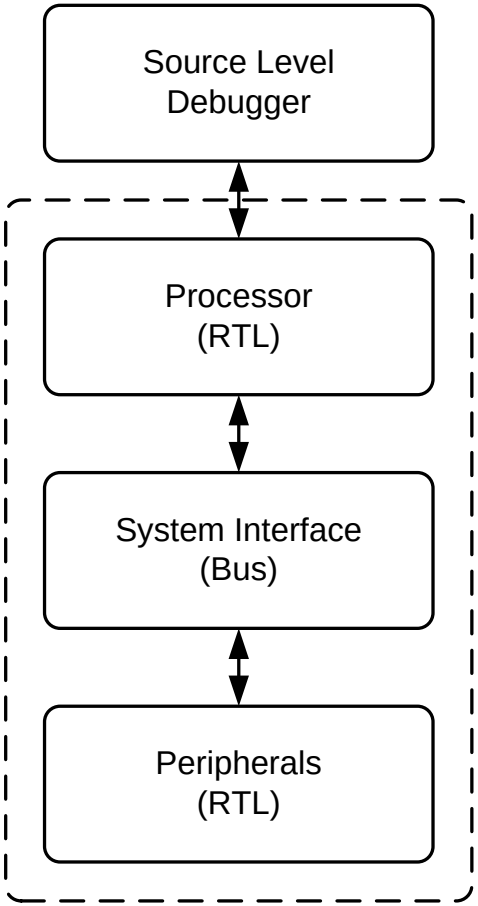


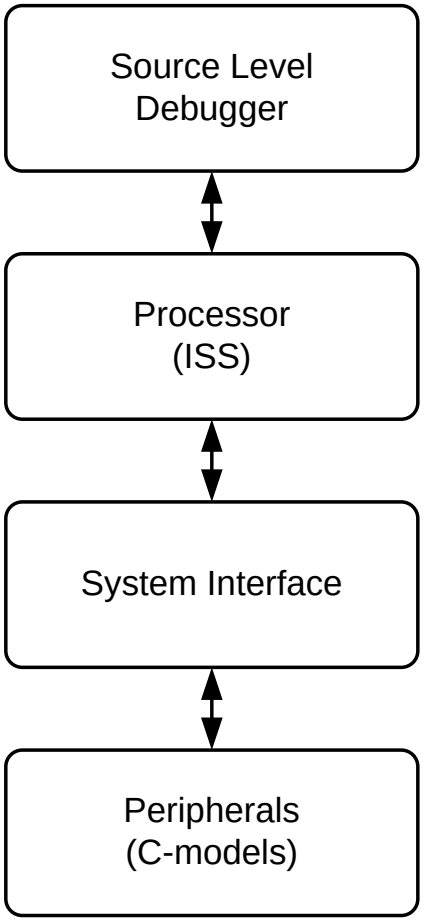
Hardware/Software Co-verification

- Emulation environment



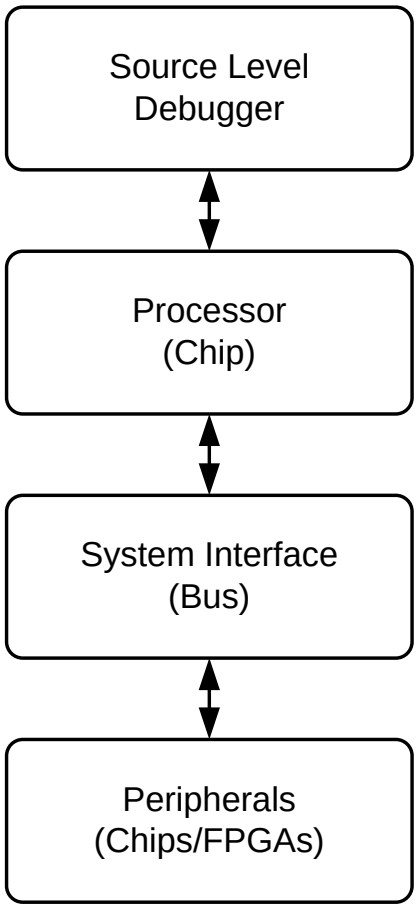
Hardware/Software Co-verification

- Soft prototype environment



Rapid Prototype Systems (RPS)

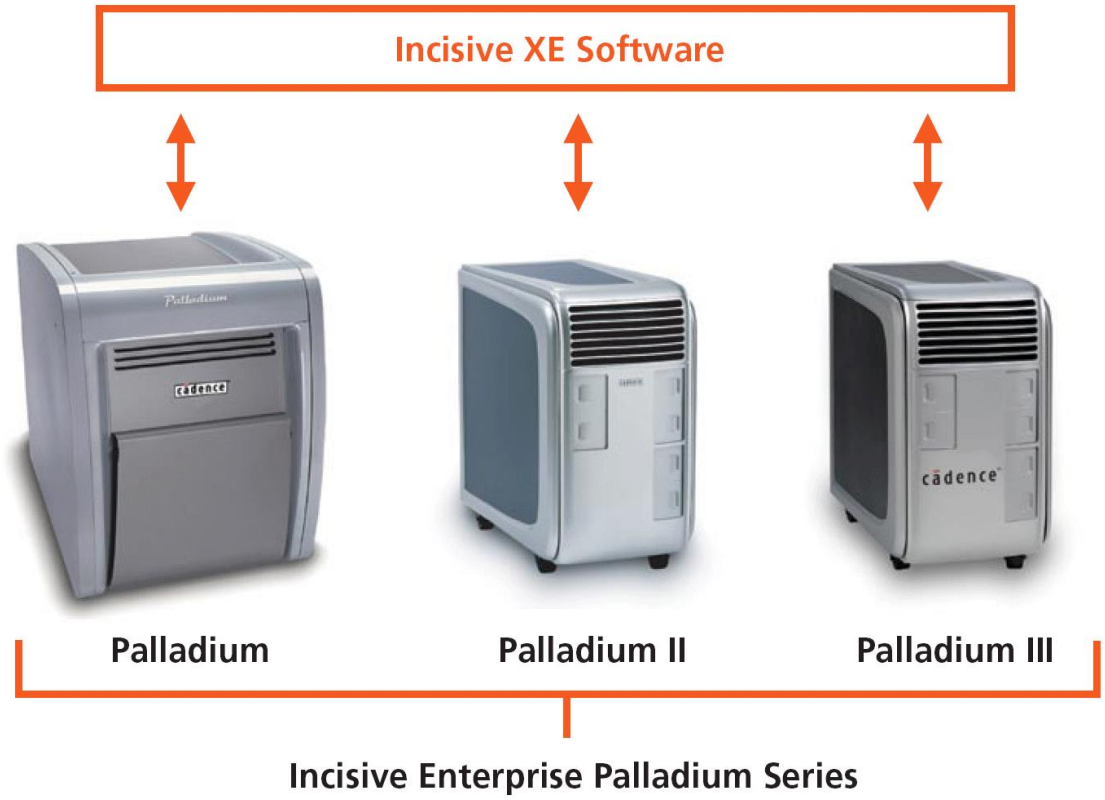
- Rapid prototype environment
  - Emulation
  - Reconfigurable
  - Application specific prototyping



Rapid Prototype Systems (RPS)

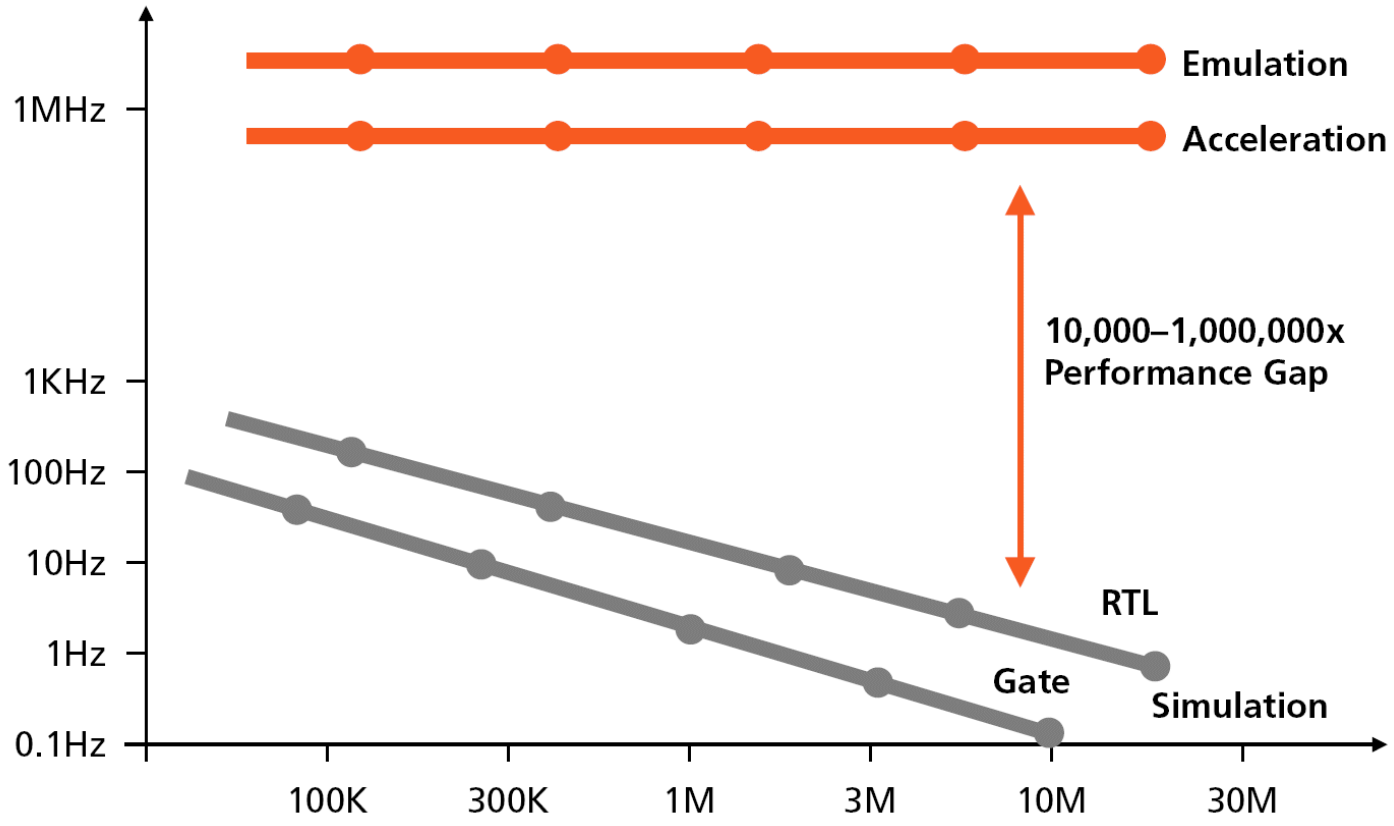
- **Features:**
  - Wide application
  - High performance
    - Possible for real-time
  - Work with AMS devices
  - ECO
    - Fast engineering change order to minor design modification on FPGA
  - Software development
- **Limitations:**
  - Design partition
    - Several FPGAs with limited I/O pins
  - Plug-in modules
  - May need design (RTL code) modification
  - Interconnect delay

Cadence Incisive Palladium (Quickturn)

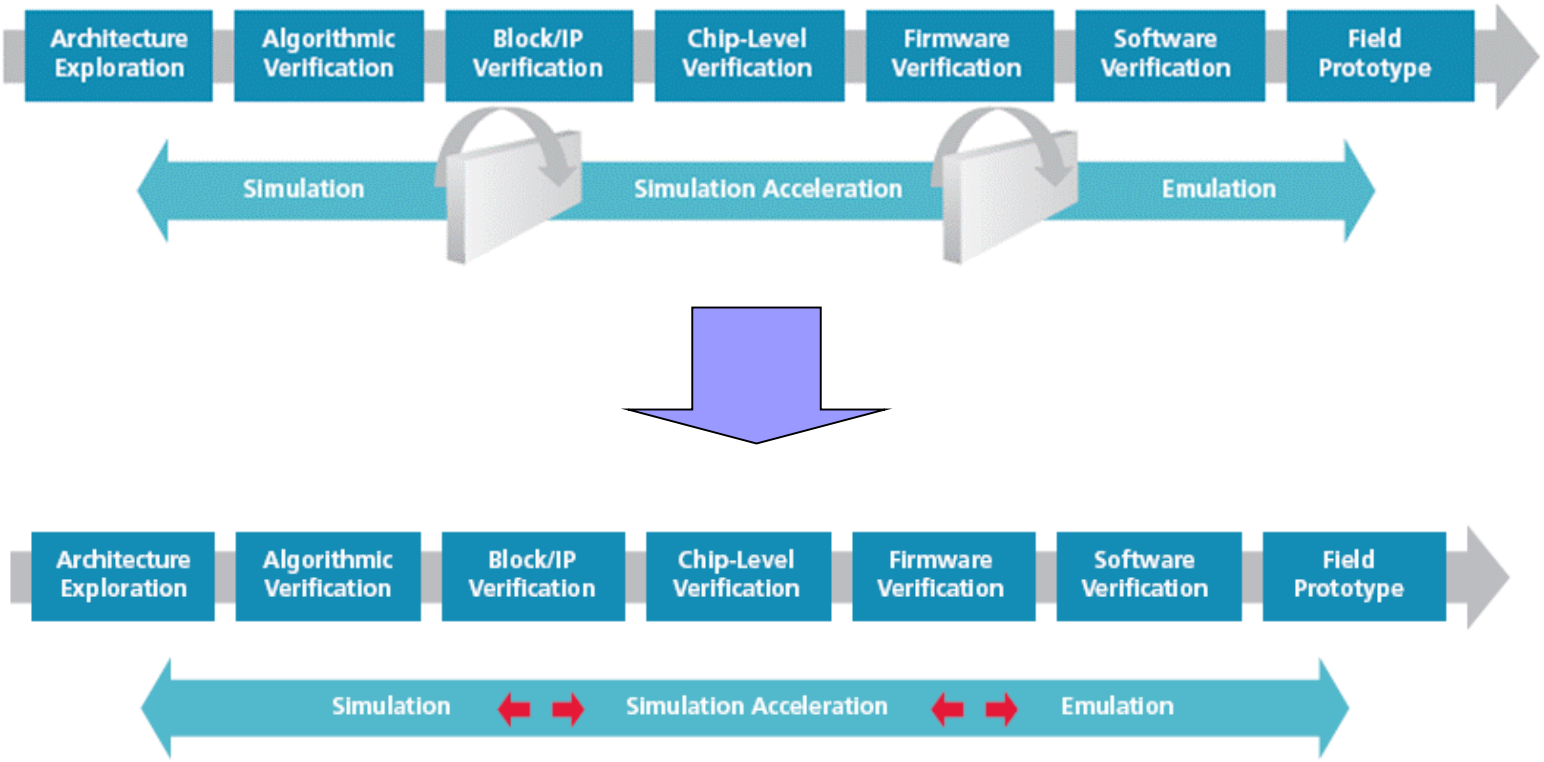


	Palladium	Palladium II	Palladium III
Maximum capacity	Up to 128M gates	Up to 256M gates	Up to 256M gates
Domain capacity	1M gates	1.8M gates	1.8M
Domains per board	8	9	9
Gates per board	8M	16M	16M
Memory per board	4GB	4.6GB	4.6GB
Maximum speed	750KHz	1.5MHz	2MHz

Cadence Incisive Palladium (Quickturn)



Cadence Verification Computing Platform: Palladium XP



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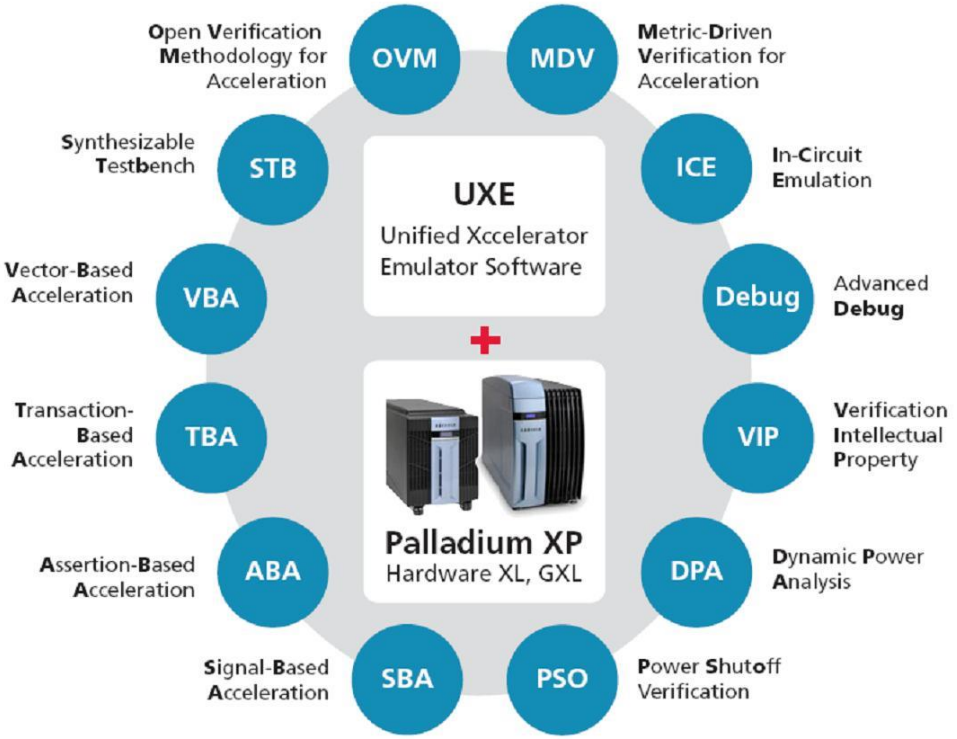


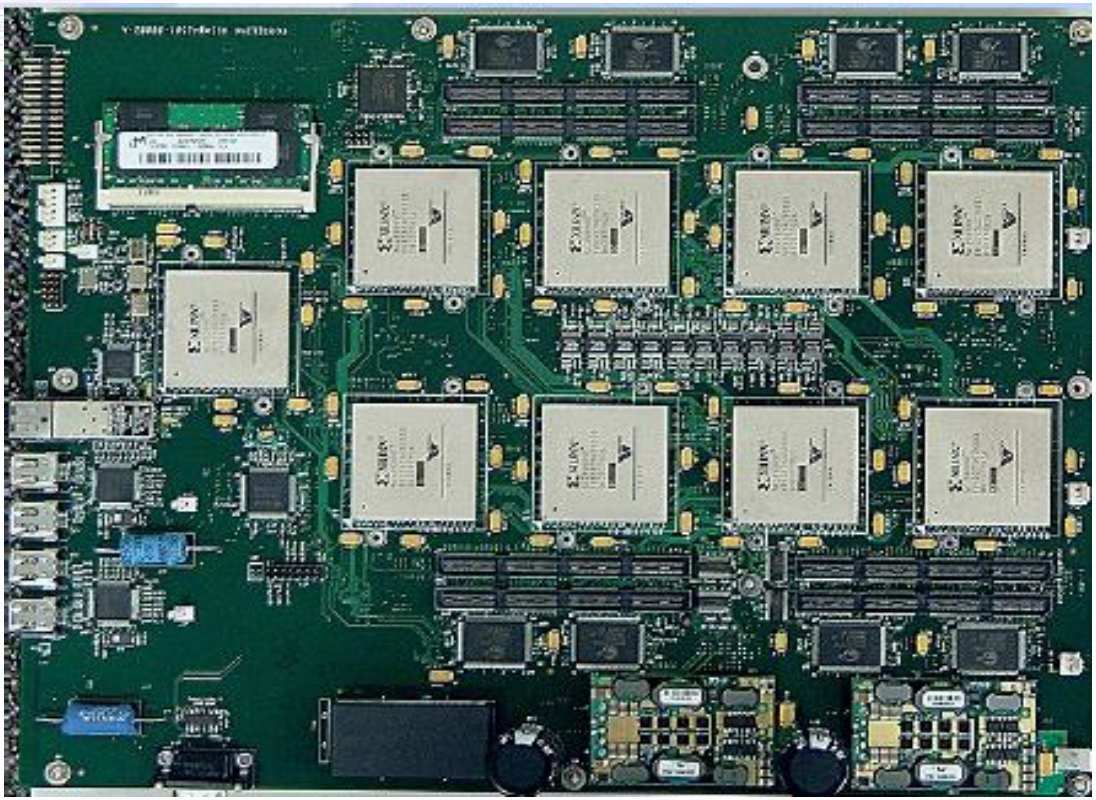
Up to 2 billion gates!

Mentor Graphics VStation (Aptix)

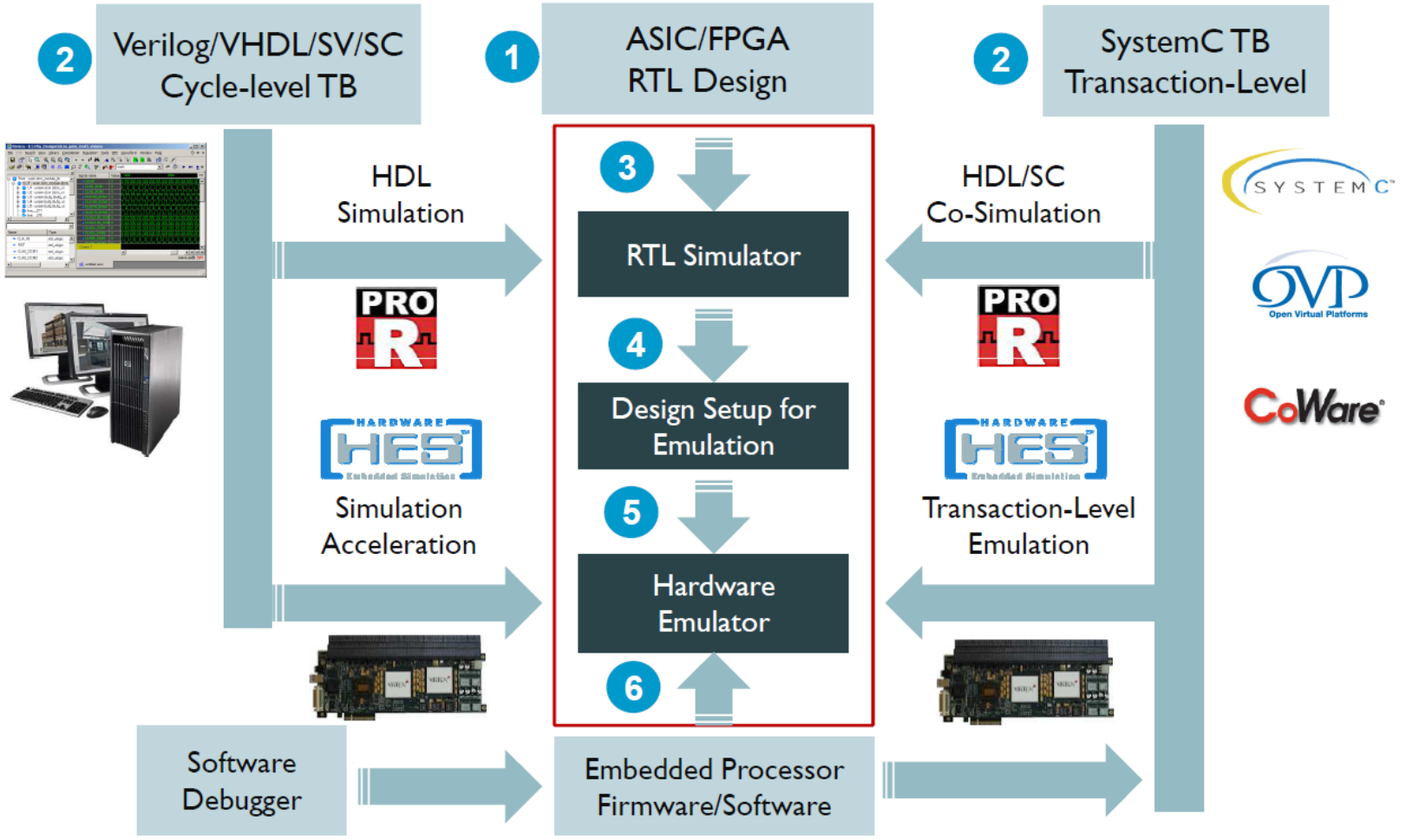
- CIC has one similar equipment!

Veloce2

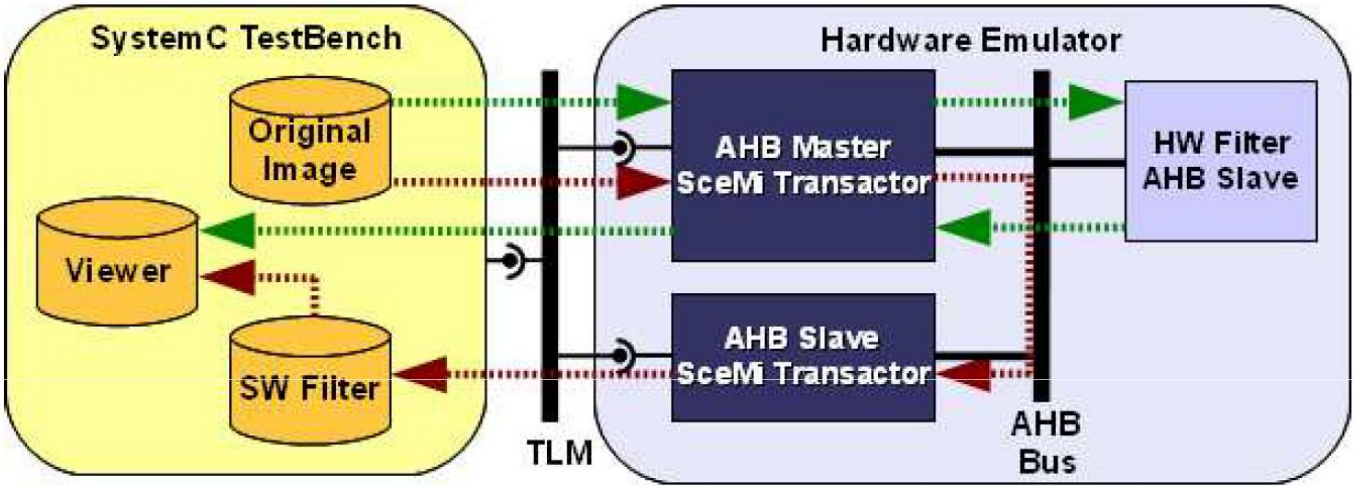
ForteLink Gemini System



ALDEC HES-DVM



ALDEC HES-DVM



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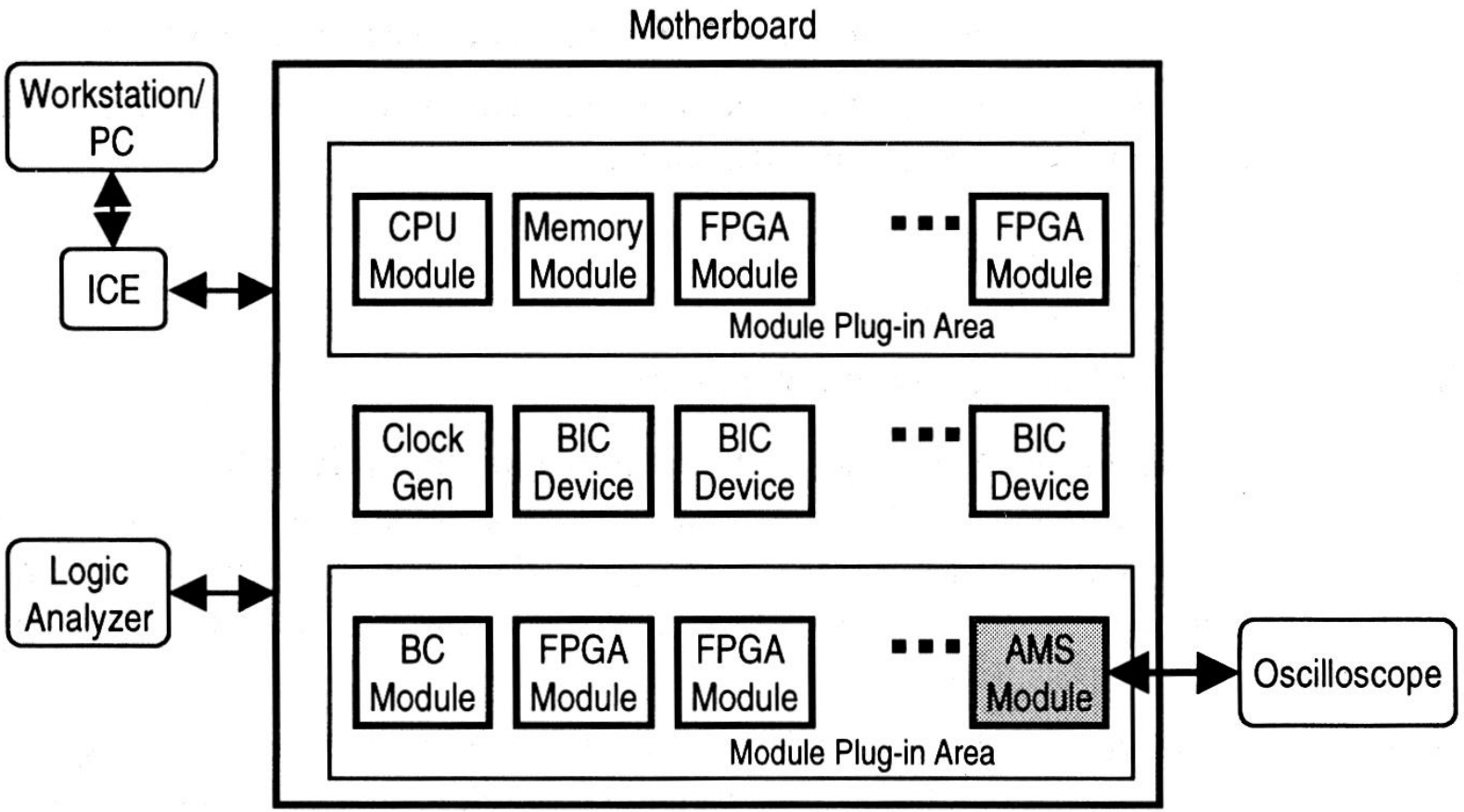
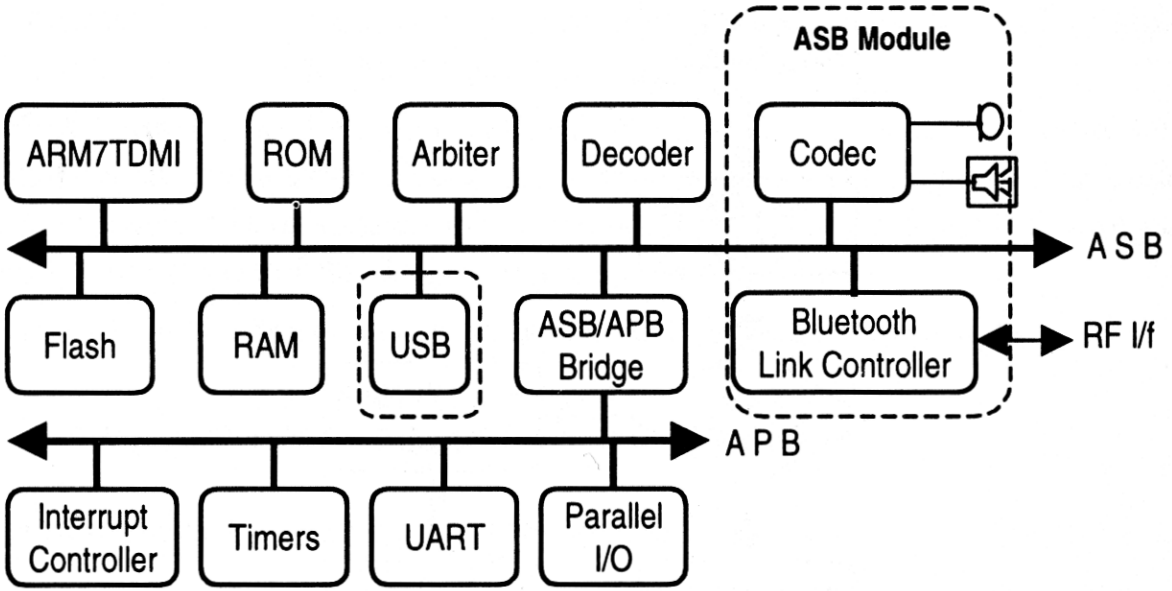
ALDEC
THE DESIGN VERIFICATION COMPANY

Reconfigurable RPS

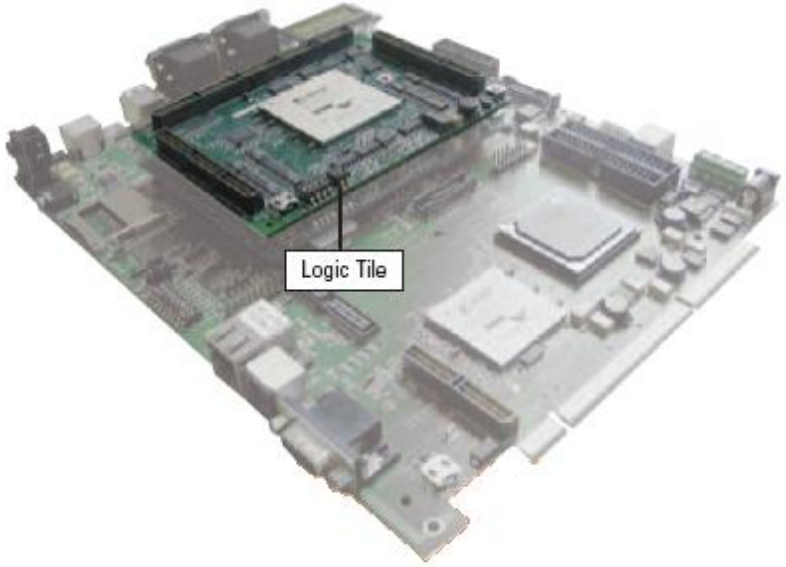


Application-Specific RPS

- Map target design to commercially available components
- Limited expansion and reuse capability
- Usually provide board support packages (BSP)



ARM Versatile



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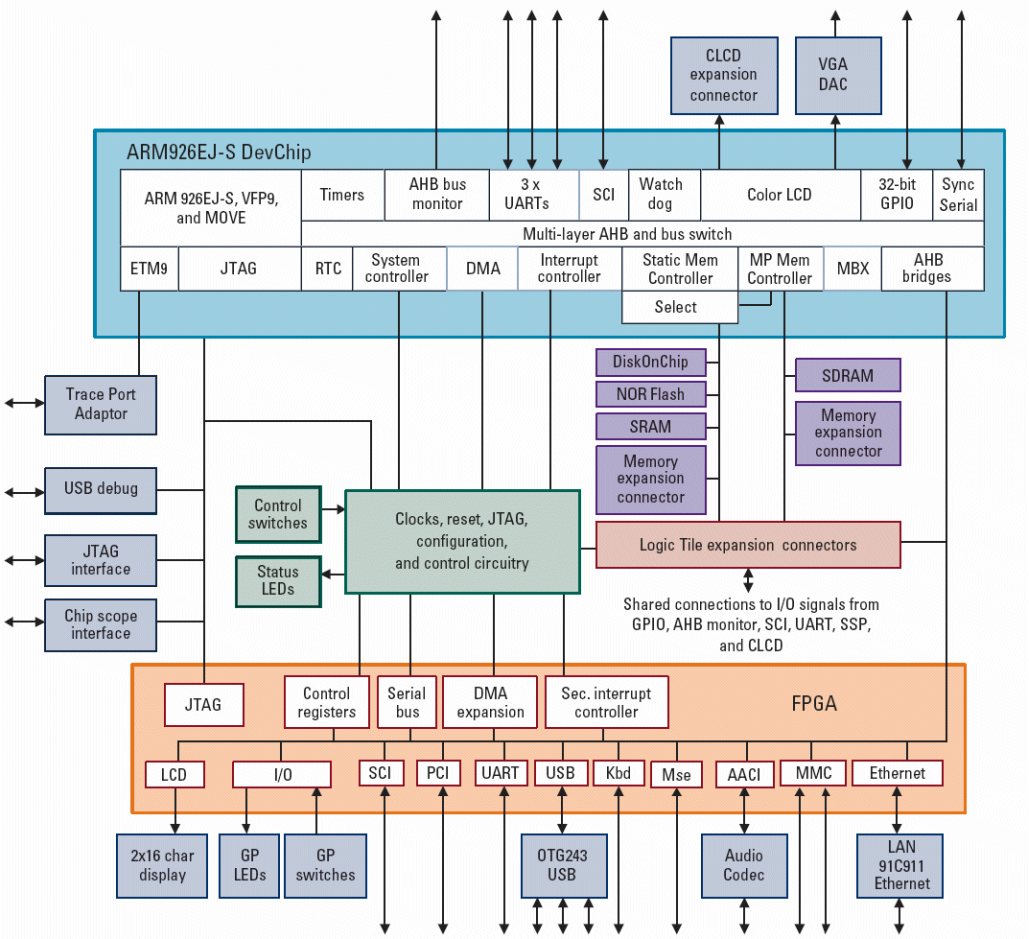
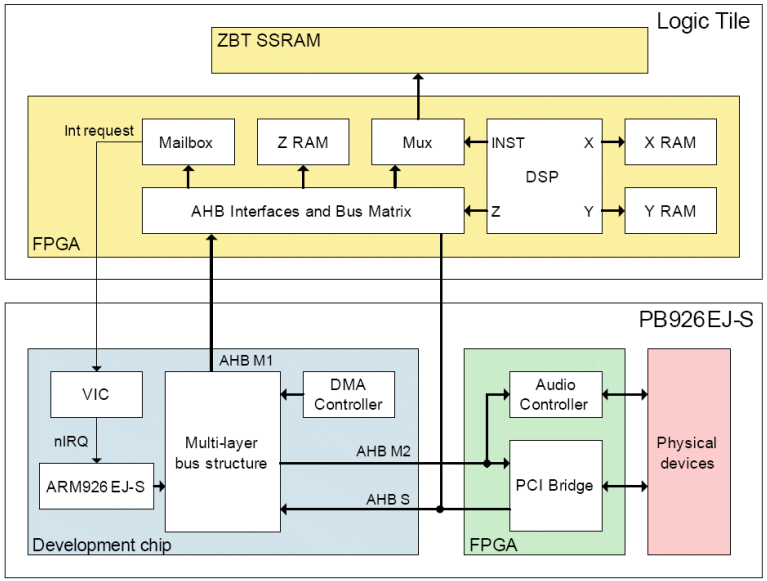
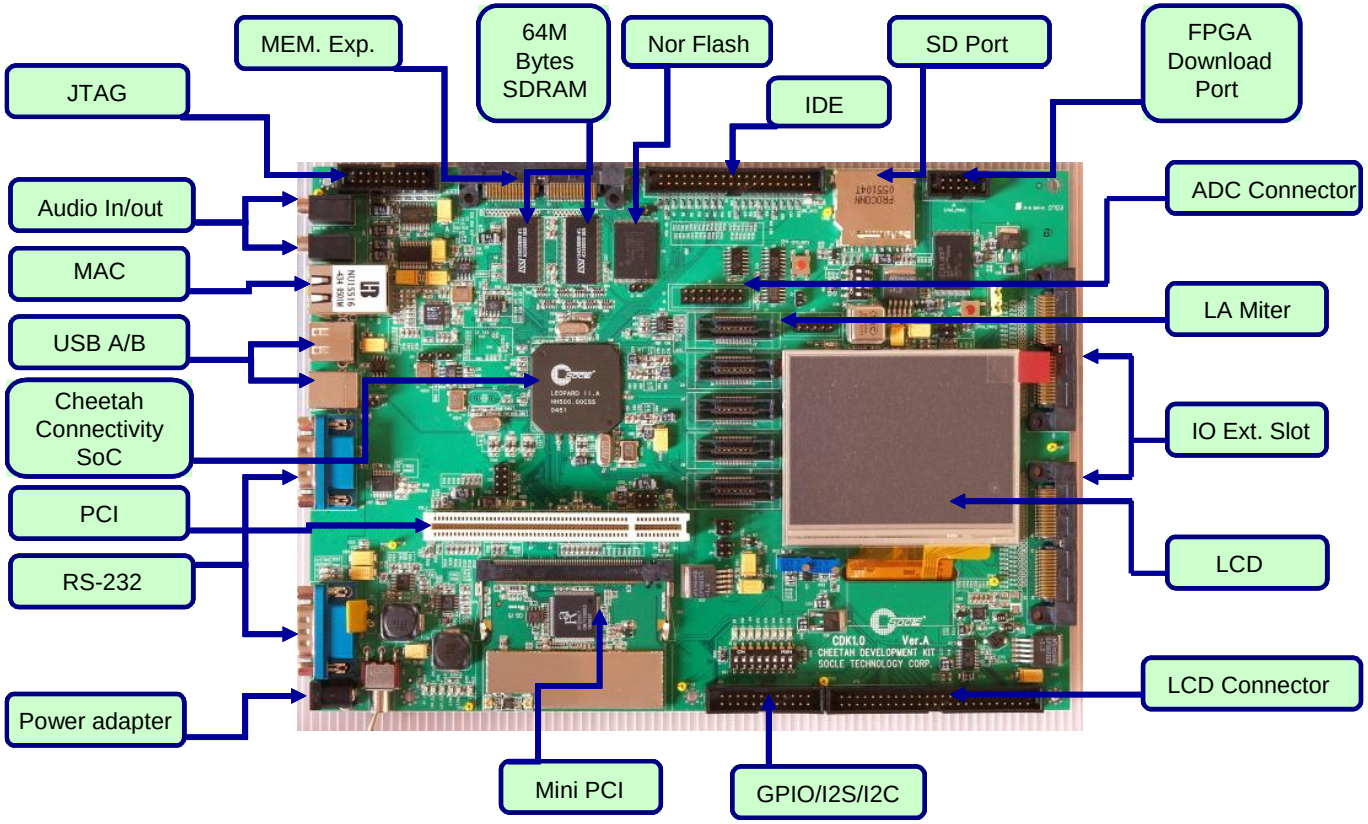


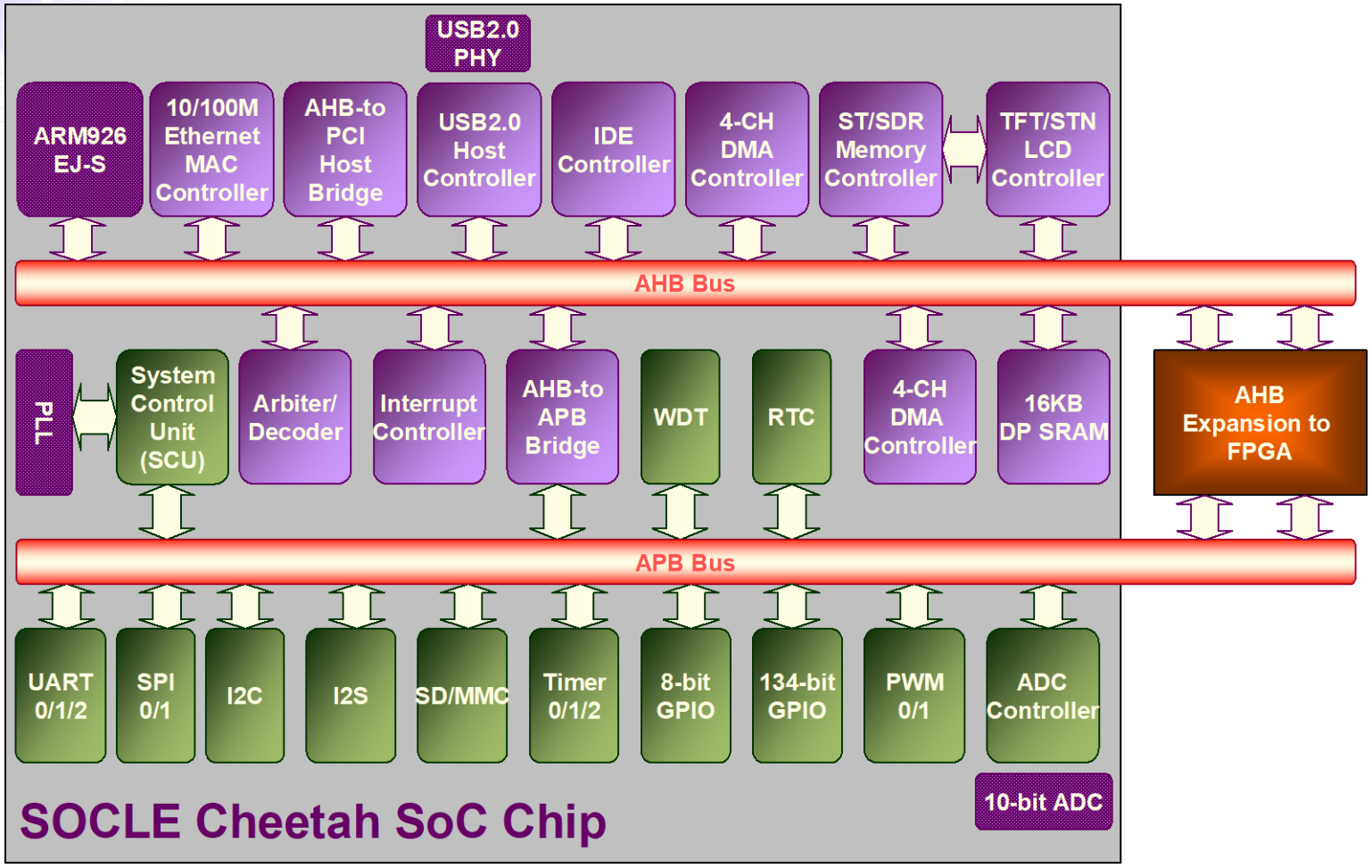


SOCLE SoC Platform

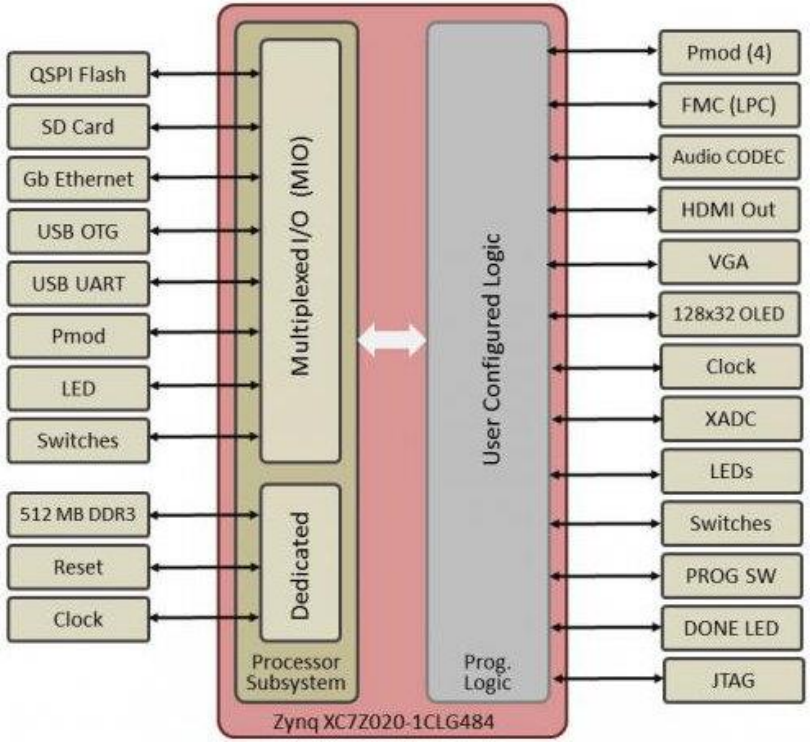
- ARM RISC + FPGA + Peripherals



SOCLE SoC Platform

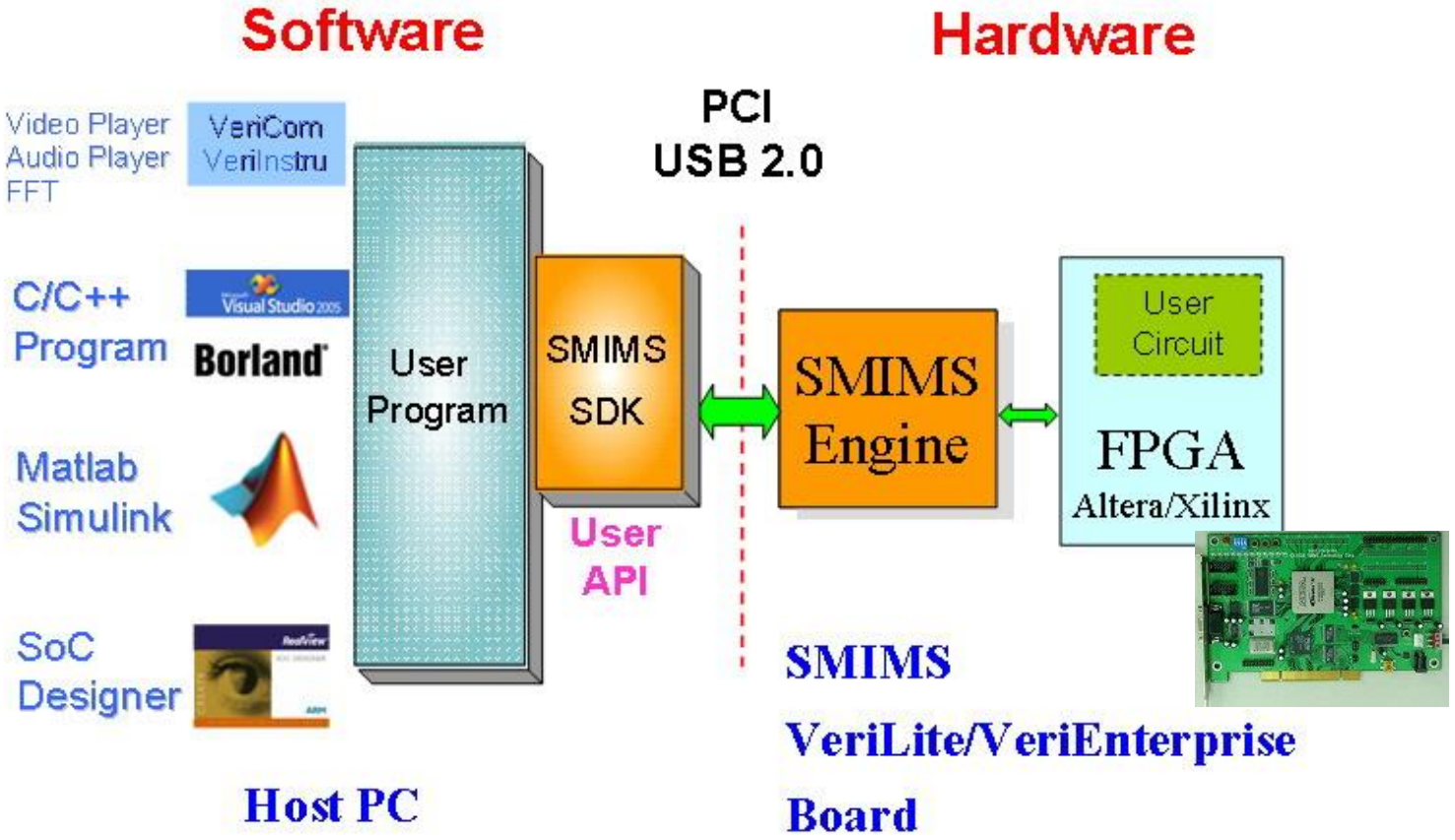


ZedBoard



ZedBoard™

SMIMS PC-Based FPGA Platform for Hardware/Sofware Co-Design and Co-Verification



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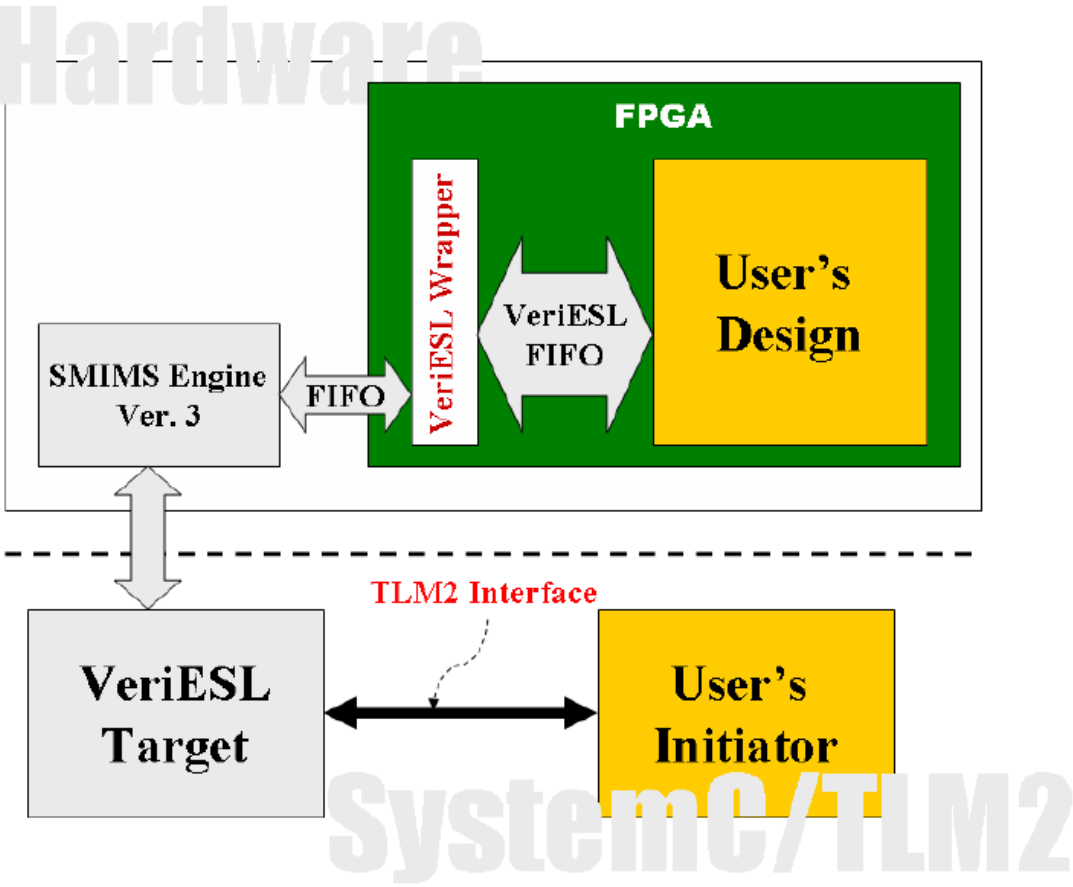

Comparison

Environment	Speed	Debugging	Software	Timing	Cost
Soft/virtual prototype	Medium	Algorithm	Firmware	No	Low
Co-verification	Slow	High	Firmware	Yes	High
Rapid prototype system	Medium →High	Low	Real	Yes	Medium
Emulation	High	Low	Real	Yes	Very high