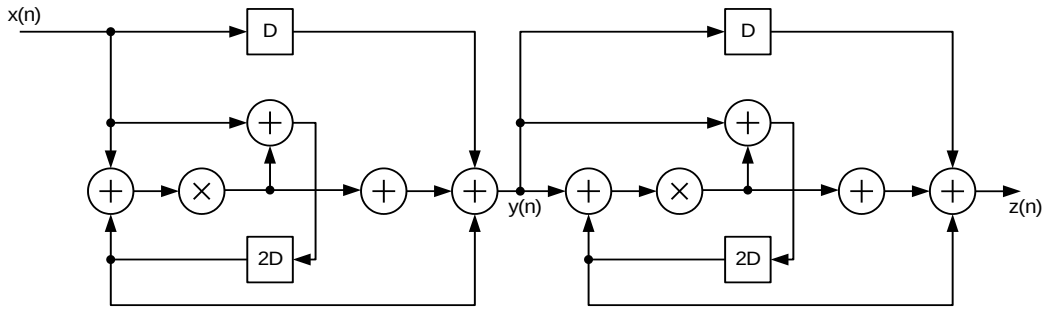
DSP in VLSI Design
Homework (IV)

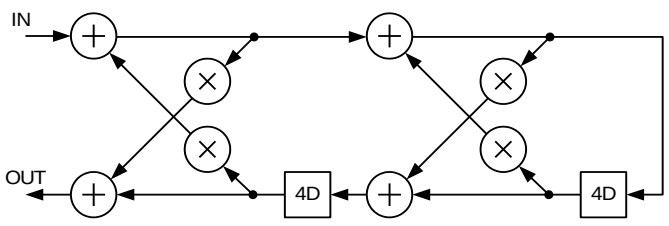
Retiming

Deadline: Oct. 26

1. Consider the wave digital filter shown below. Assume that each multiply operation requires 20 ns and each add operation required 10 ns.
   (a) Calculate the iteration period bound of this filter by inspection.
   (b) Where is the critical path?
   (c) Manually pipeline and/or retime this filter to achieve a critical path equal to the iteration period bound.



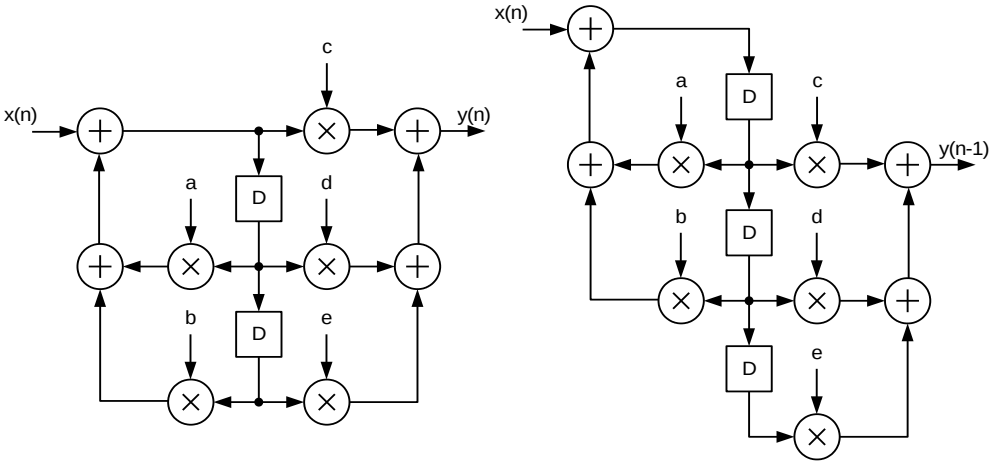
2. Consider the IIR filter DFG shown in below. Assume that addition and multiplication require 1 and 2 u.t., respectively.
   (a) By inspection, calculate the iteration bound.
   (b) Compute the critical path time of the circuit.
   (c) Pipeline and/or retime this system to achieve a critical path of 2 u.t. Do this by inspection (manually).
   (d) Pipeline and/or retime this system to achieve sample period of 1 u.t., where Fine-grain retiming is allowed. Do this by inspection (manually).



3. The two IIR filter DFGs shown below are equivalent.

(a) Prove the two circuits are equivalent.

(b) Transform the left circuit to the right circuit by pipelining and/or retiming.



Please deliver the homework to the TA:

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除非為程式作業，作業盡量繳交紙本格式，不過要交電子檔也沒關係