DSP in VLSI Design
Homework (III)

Pipelining and Parallel Processing

Deadline: Oct. 12

1. Consider a direct-form implementation of the FIR filter

$$y(n) = ax(n) + bx(n-2) + cx(n-3)$$

Assume that the time required for 1 multiply-add operation is T.

(a) Pipeline this filter such that the clock period is approximately T.

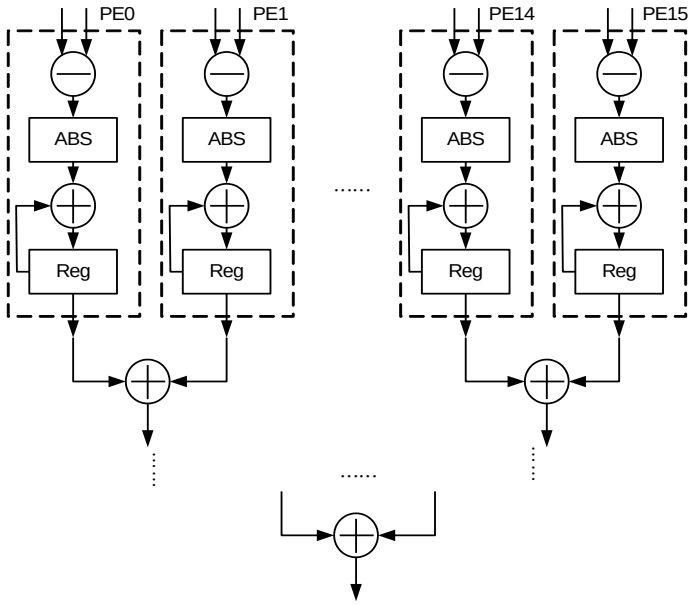
(b) Draw a block filter architecture for a block size of three. Pipeline this block filter such that the clock period is about T. What is the system sample rate?

(c) Pipeline the block filter in part (b) such that the block period is about T/2. Show the appropriate cutsets and label the outputs clearly. What is the system sample rate now? (Hint: you can use fine-grain pipelining.)

2. Consider the core of a systolic array motion estimation architecture shown in the following figure. Assume the computation time of subtractor, absolutor, and adder are 5ns, 7ns, and 6ns, respectively.

(a) Where is the critical path? What is the maximum working frequency of this circuit?

(b) If we want to double the working frequency, please design the associated architecture.



3. Consider the 6-th-order FIR filter

$$y(n) = ax(n) + bx(n-4) + cx(n-6).$$

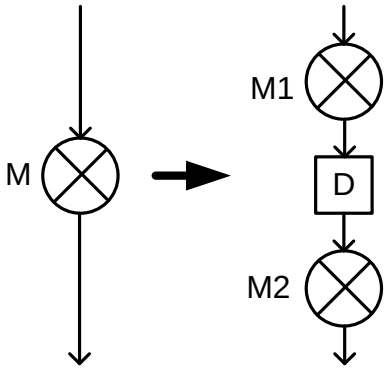
Draw the block diagram of this filter for block size of 3.

4. For the example shown in Page 30 in the handout, with the same sampling period (9 u.t.),

(a) What is the new supply voltage?

(b) What is the power saving percentage?

We then employ fine-grained pipelining technique to further reduce the power consumption, that is, each multiplier is replaced with a pipelined multiplier as follows:



where T_M=8 u.t., T_{M1}=T_{M2}=4 u.t.; C_M=8C_A, C_{M1}=C_{M2}=4C_A

(c) What is the new supply voltage?

(d) What is the power saving percentage?

Please deliver the homework to the TA:

BL-421, 吳柏辰, pcwu@media.ee.ntu.edu.tw

除非為程式作業，作業盡量繳交紙本格式，不過要交電子檔也沒關係