

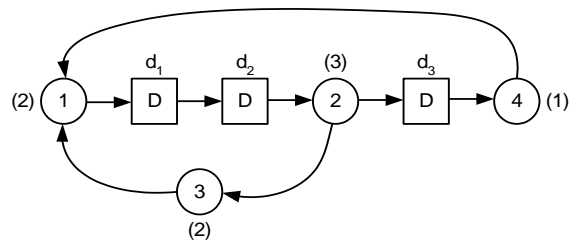
# DSP in VLSI Design

## Homework (V)

### Unfolding

Deadline: April 9

1. In homework (II), you have computed the iteration bound of the following DFG. Please design a new DFG with unfolding to achieve this iteration bound.



2. In homework (III), you have designed a 3-parallel architecture for a direct-form FIR filter,  $y(n) = ax(n) + bx(n-2) + cx(n-3)$ . Please derive the 3-parallel architecture again by using the unfolding technique.

Please deliver the homework to the TA:

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