DSP in VLSI Design
Homework (III)

Pipelining and Parallel Processing

Deadline: March 23, 2010

1. Consider a direct-form implementation of the FIR filter

$$y(n) = ax(n) + bx(n-2) + cx(n-3)$$

Assume that the time required for 1 multiply-add operation is T.

(a) Pipeline this filter such that the clock period is approximately T.

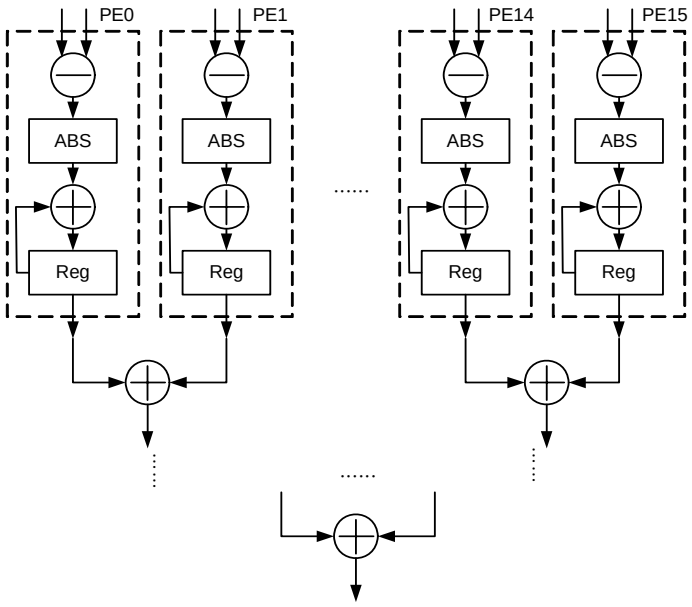
(b) Draw a block filter architecture for a block size of three. Pipeline this block filter such that the clock period is about T. What is the system sample rate?

(c) Pipeline the block filter in part (b) such that the block period is about T/2. Show the appropriate cutsets and label the outputs clearly. What is the system sample rate now? (Hint: you can use fine-grain pipelining.)

2. Consider the core of a systolic array motion estimation architecture shown in the following figure. Assume the computation time of subtractor, absolutor, and adder are 5ns, 7ns, and 6ns, respectively.

(a) Where is the critical path? What is the maximum working frequency of this circuit?

(b) If we want to double the working frequency, please design the associated architecture.



3. Design the 4-parallel (L=4) version of the circuit in page 21.

4. Consider the 6-th-order FIR filter

$$y(n) = ax(n) + bx(n-4) + cx(n-6).$$

Draw the block diagram of this filter for block size of 3.

Please deliver the homework to the TA:

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