DSP in VLSI Design
Homework (VI)

Folding

Deadline: Nov. 4

1. Consider the 6-tap FIR filter

$$y(i) = \sum_{i=0}^{5} h_i x(n-i)$$

implemented using data-broadcast form shown in the following figure. This filter S0={MA5, MA4}, S1={MA3, MA2}, S2={MA1, MA0}.

(a) Design the folded architecture.

(b) Construct a schedule corresponding to the folded architecture and verify that the folded architecture generated the desired filter output samples.

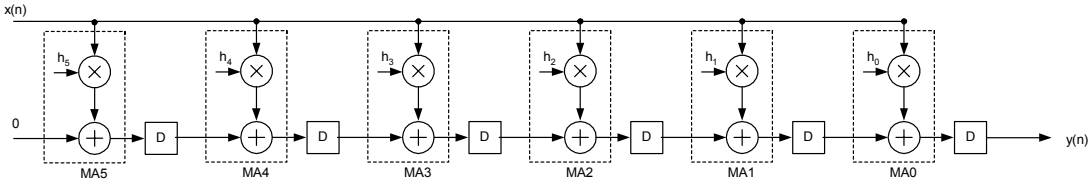

Fig. 1

2. Consider the 4-bit carry propagation adder (CPA) shown in the following figure. Now, we want to derive its bit-serial architecture by using folding technique.

(a) Derive the folding set.

(b) Design the folded architecture.

(c) Construct the schedule to show the architecture can do the same operation as CPA.

(d) Similarly, use the same method to derive 2-digit-serial architecture with the folding set, folded architecture, and schedule.

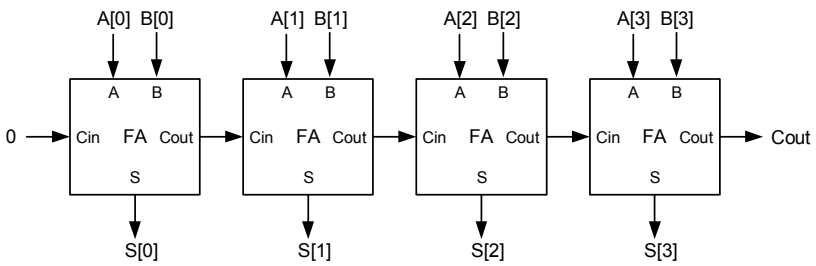

Fig. 2

Please deliver the homework to the TA:
BL-421，陳則瑋dspdesign@media.ee.ntu.edu.tw