About Term Project

About Term Project

- One topic per team
- 1—3 members per team

- You must **employ the design techniques introduced in this class** in the term project
- Two directions: paper survey or implementation
- Paper survey
  - Need **architectural comparison and analysis** of more than one architectures
  - Like the “case study” part of this course
- Implementation
  - **Experimental (implementation) results** are required
- You can combine both directions
- Your topics for thesis is OK

Some Suggested Topics (1)

- Paper survey
  - Briefly introduce the algorithm
  - Report two or more papers on the same topic, analyze it with what you learned in this course

Some Suggested Topics (2)

- Implementation
  - There is no limitation for these topics
  - Design hardware architecture for a specific DSP algorithm
    - FFT, DCT, DWT, ME, …
  - Compared to existing architectures
  - Hardware architecture design methodologies with some examples
  - **The key is hardware architecture design and analysis, not implementation**

Some Suggested Paper List (1/3)

- FFT
  - M. A. Richards, "On hardware implementation of the split-radix FFT," IEEE Transactions on Acoustics, Speech, and Signal Processing, vol. 36, no. 10, pp. 1575--1581, Oct. 1988.
  - I. R. Mactaggart and M. A. Jack, "A single chip radix-2 FFT butterfly architecture using parallel data distributed arithmetic," IEEE Journal of Solid-State Circuits, vol. sc-19, no. 3, pp. 368--373, June 1984.
  - W. A. Perera, "Architectures for multiplierless fast fourier transform hardware implementation in VLSI," IEEE Transactions on Acoustics, Speech, and Signal Processing, vol. ASSP-35, no. 12, pp. 1750--1760, Dec. 1987.
  - Y.-N. Chang and K. K. Parhi, "An efficient pipelined FFT architecture," IEEE Transactions on Circuits and Systems--II: Analog and Digital Signal Processing, vol. 50, no. 6, pp. 322--325, June 2003.
  - E. Bidet, D. Castelain, C. Joanblanq, and P. Senn, "A fast singla-chip implementation of 8192 complex point FFT," IEEE Journal of Solid-State Circuits, vol. 30, no. 3, pp. 300--305, March 1995.
  - M.-K. Lee, K.-W. Shin, and J.-K. Lee, "A VLSI array processor for 16-point FFT," IEEE Journal of Solid-State Circuits, vol. 26, no. 9, pp. 1286--1292, September 1991.
  - C. C. W. Hui, T. J. Ding, J. V. McCanny, and R. F. Woods, "A 64-point fourier transform chip for video motion compensation using phase correlation," IEEE Journal of Solid-State Circuits, vol. 31, no. 11, pp. 1751--1761, Nov. 1996.

Some Suggested Paper List (2/3)

- DCT
  - A. Madisetti and A. N. Willson Jr., "A 100 MHz 2-D 8x8 DCT/IDCT processor for HDTV applications," IEEE Transactions on Circuits and Systems for Video Technology, vol. 5, no. 2, April 1995.
  - D. Slawecki and W. Li, "DCT/IDCT processor for high data rate image coding," IEEE Transactions on Circuits and Systems for Video Technology, vol. 2, no. 2, June 1992.
  - Y.-T. Chang and C.-L. Wang, "New systolic array implementation of the 2-D discrete cosine transform and its inverse," IEEE Transactions on Circuits and Systems for Video Technology, vol. 5, no. 2, April 1995.
- DWT
  - C. Chakrabarti, M. Vishwanath, and R. M. Owens, "Architectures for wavelet transforms: A survey," Journal of VLSI Signal Processing, vol. 14, pp. 171–192, 1996.
  - K. Andra, C. Chakrabarti, and T. Acharya, "A VLSI architecture for lifting-based forward and inverse wavelet transform," IEEE Transactions on Signal Processing, vol. 50, no. 4, pp. 966–977, Apr. 2002.
  - C.-T. Huang, P.-C. Tseng, and L.-G. Chen, "Flipping structure: An efficient VLSI architecture for lifting-based discrete wavelet transform," IEEE Transactions on Signal processing, vol. 52, no. 4, pp. 1080--1089, April 2004.
  - N. D. Zervas, G. P. Anagnostopoulos, V. Spiliotopoulos, Y. Andreopoulos, and C. E. Goutis, "Evaluation of design alternatives for the 2-D-discrete wavelet transform," IEEE Transactions on Circuits and Systems for Video Technology, vol. 11, no. 12, pp. 1246–1262, Dec. 2001.
  - P.-C. Wu and L.-G. Chen, "An efficient architecture for two-dimensional discrete wavelet transform," IEEE Transactions on Circuits and Systems for Video Technology, vol. 11, no. 4, pp. 536–545, Apr. 2001.
  - W. Jiang and A. Ortega, "Lifting factorization-based discrete wavelet transform architecture design," IEEE Transactions on Circuits and Systems for Video Technology, vol. 11, no. 5, pp. 651–657, May 2001.

Some Suggested Paper List (3/3)

- ME
  - K.-M. Yang, M.-T. Sun, L. Wu, "A family of VLSI design for the motion compensation block matching algorithm," IEEE Transactions on Circuits and Systems, vol. 36, no. 10, October 1989.
  - T. Komarek and P. Pirsch, "Array architecture for block matching algorithm," IEEE Transactions on Circuits and Systems, vol. 36, no. 10, October 1989.
  - H. Yo and Y. H. Hu, "A novel modular systolic array architecture for full-search block matching motion estimation," IEEE Transactions on Circuits and Systems for Video Technology, vol. 5, no. 5, October 1995.
  - L. D. Vos and M. Stegherr, "Parameterizable VLSI architectures for the full-search block-matching algorithm," IEEE Transactions on Circuits and Systems, vol. 36, no. 10, October 1989.
  - Y.-S. Jehng, L.-G. Chen, and T.-D. Chiueh, "An efficient and simple VLSI tree architecture for motion estimation algorithms," IEEE Transactions on Signal Processing, vol. 41, no. 2, February 1993.
  - Y.-W. Huang, S.-Y. Chien, B.-Y. Hsieh, and L.-G. Chen, "An efficient and low power architecture design for motion estimation using global elimination algorithm," IEEE International Conference on Acoustics, Speech, and Signal Processing, 2002.
  - W.-M. Chao, C.-W. Hsu, Y.-C. Chang, and L.-G. Chen, "A novel hybrid motion estimator supporting diamond search and fast full search," IEEE International Symposium on Circuits and Systems, 2002.
  - Y.-W. Huang, T.-C. Wang, B.-Y. Hsieh, and L.-G. Chen, "Hardware architecture design for variable block size motion estimation in MPEG-4 AVC/JVT/ITU-T H.264," IEEE International Symposium on Circuits and Systems, 2003.

Reference Journals

- IEEE Transactions on Circuits and Systems for Video Technology
- IEEE Transactions on Circuits and Systems I
- IEEE Transactions on Circuits and Systems II
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems
- IEEE Transactions on Very Large Scale Integration Systems
- Journal of VLSI Signal Processing

Important Dates

- 5/29 proposal with team member list
  - Prepare at most two A4 papers with the following topics:
    - Final project topic & team
    - Motivation
    - Introduction
    - Plan and steps (how to do experiments/implementation)
    - Expected result (which design technique will be employed)
  - Both English and Chinese are allowed
  - Submit the printed manuscript to TA
- 6/12, 6/26 Term project oral presentation